

PRIME

9655™

Features

High-performance 32-bit supermini with up to 8Mb of error correcting, high-speed MOS memory.

Easy-to-use operator interface allows one-step system initialization.

Advanced gate array based processor design.

Advanced Schottky implementation of TTL circuitry.

Pipelined central processor organization allows concurrent processing of two instructions.

16Kb of high-speed cache memory to reduce memory access time.

Up to 128 terminals supported, with up to 255 active processes.

Hardware/microcode implemented instructions for quad precision floating-point operations.

Hardware decimal arithmetic to supplement COBOL performance.

Environmental sensing to detect over-temperature occurrence.

Automatic microverification and parity checking throughout system.

Protection rings and embedded operating system to ensure memory security.

Diagnostic processor with two integrated floppy disks for loading operational and diagnostic microcode.

Full hardware and software compatibility with all 50 Series™ systems.

Efficient, multifunction PRIMOS® operating system plus a wide range of available system and application software.

Description

The 9655 system is a high-performance, interactive supermini ideal for computation, commercial and CAD/CAM/CAE applications in standalone or distributed environments. Hardware and software compatible with the entire line of 50 Series systems, the 9655 includes a 32-bit CPU, an instruction pipeline unit, up to 8Mb of error-correcting MOS memory, burst mode I/O, quad-precision floating point arithmetic, high speed decimal arithmetic, 16Kb cache memory, a sophisticated diagnostic processor, and the PRIMOS[®] operating system.

The 9655 system supports up to 128 terminals in an interactive environment of up to 255 processes. It uses the PRIMOS operating system which supports concurrent interactive and batch processing and is compatible across Prime's entire product line. Like all 50 Series systems, the 9655 can be networked to other Prime[®] systems using PRIMENET[™] communications software and compatible, standard Prime peripherals and controllers.

The standard system is packaged in a 53-inch high, FCC-compliant cabinet that includes a chassis for the CPU and memory, and a chassis for ten I/O controllers. Each chassis has its own power supply. The system includes a two-board processor, diagnostic processor, a power distribution unit, and a cable connector bulkhead for easy reconfiguration of terminal and communications lines. The basic system, including the CPU, 4Mb memory and disk controller uses seven of the available board slots. The remaining slots can be used for additional memory, tape controllers, a line printer controller and other peripheral controllers. Disk, tape and some communication devices must reside in an additional 53-inch high peripheral cabinet.

Prime 50 Series Architectural Features

Compatibility

Prime systems are designed for hardware and software compatibility. Like all 50 Series systems, the 9655 runs under the PRIMOS operating system. The single operating system ensures total software portability across all prime systems. User programs developed on one system will run on all the others without recompilation or modification. In addition, programmers use the same set of commands on all systems. The 9655 is I/O compatible with the entire Prime product line; peripheral controllers can be interchanged between different systems for flexibility and cost-effective upgrade and expansion.

32-bit Architecture

The 9655 uses 32-bit architecture for internal operating efficiency and for large program support. Full 32-bit word length lets more information be processed during each machine cycle than is possible with 16-bit systems. As a result, the system does more work per cycle because it's manipulating a larger amount of data.

The 32-bit word length permits program design without concern for space restrictions. Therefore, very large programs can run on a 9655 processor, programs that might otherwise require a mainframe or very complicated programming.

Virtual Memory Management

Running under the PRIMOS operating system, the 9655 gives each user a virtual address space much larger than physical memory. The mechanisms for virtual memory management are designed for system efficiency and total user transparency. Each user has 512Mb of virtual address space; 64Mb is reserved for private user program space. The rest is for shared libraries and operating system functions.

System functions, such as I/O, are embedded in the virtual address space of each process. This design increases system throughput using ordinary procedure calls, eliminating the need for special system calls. A protection ring mechanism ensures operating system integrity.

Program Environment

Programs for the 9655 system operate in a multi-segment environment that includes a stack segment containing all local variables, a procedure segment containing executable code, and a linkage segment containing statistically allocated variables and linkages to common data. Highly efficient addressing modes provide access to stack and linkage variables. In addition, stack management overhead is minimized by implementing the procedure call mechanism in firmware.

The 9655 stack management mechanisms optimize the efficiency of argument passing, subroutine and procedure calls, arithmetic expressions evaluation, and dynamic allocation of temporary storage. In addition, these mechanisms support re-entrant and recursive procedures.

High-density MOS Memory

Main memory of the 9655, and all Prime processors, features high-density 256K MOS semiconductors for speed and miniaturization benefits. Expandable to 8Mb, the 9655 main memory supports wide-word interleaving to accelerate memory transfers. Error-checking and correction logic monitors memory integrity.

Process Exchange

All Prime processors use an advanced process exchange facility to accelerate performance in multi-user environments. This facility manages context switching, in which the processor transfers control from one process or program to another. Context switching algorithms are implemented in firmware for maximum efficiency and reside in the CPU's micro-programmed control unit.

Register Sets

The 9655 processor has 11 register sets, each containing 32 registers, for a total of 352 32-bit registers. Eight of the register sets are program addressable. One stores the execution state of the currently active process while the other seven store the state of the last seven previously active processes. If one of these processes is the next process to be activated, its state is already loaded, ready for execution. This parallel register set design greatly reduces process exchange overhead in multiuser environments.

The three remaining 32-bit register sets further enhance the processing efficiency of the system. Two sets support the operation of the micro-programmed control unit. The other set contains the 32 direct memory access (DMA) channels.

High-speed Address Buffer

Frequently used virtual-to-physical address translations are stored in the high-speed buffer called the Segment Table Lookaside Buffer (STLB). The STLB's storage capacity on the 9655 is 512 entries. More than 98% of the time, PRIMOS can find the needed physical addresses in the STLB. Access to the STLB is completely overlapped with access to cache for maximum speed.

The 9655 also uses an I/O bus mapping scheme to allow I/O bus transfers to come from (or go to) any location in physical memory. This mapping scheme embodies virtual to physical address translations. The 9655 has an I/O Translation Lookaside Buffer (IOTLB), with 128 entries which allows mapping translations to occur within the hardware of the CPU.

Hardware Integrity Features

The 9655 provides hardware system integrity through comprehensive error detection and reporting mechanisms. Microverification routines, invoked automatically when the system is initialized, test the validity of the CPU and controllers. While the system is running, parity checking ensures data integrity throughout the processor's internal busses, registers and other data paths.

In addition, the 9655 checks the parity of each microcode control word automatically. Main memory error detection and correction detects all double and single-bit errors and corrects single-bit errors. All detected errors are written to the system event log automatically, to help Prime's Customer Service Representatives troubleshoot component problems early.

Protection Rings

A hierarchical multi-ring protection mechanism ensures the security of memory contents. Every program runs at an access privilege level that is hardware enforced. Protection rings prevent processes from accessing unauthorized memory locations.

9655 Special Features

Instruction Pipeline Unit

The Instruction Pipeline Unit improves central processor throughput by prefetching and decoding up to four anticipated instructions. It's an advanced instruction look-ahead buffer that incorporates a two-stage pipelined design. This feature relieves the central processor of instruction preparation overhead by operating in parallel with the 9655 system's Instruction Execution Unit (IEU).

The first stage of the pipeline is an instruction buffer. It is managed by prefetch logic that transfers instructions from cache. The buffer stores up to four instruction words in a first-in, first-out (FIFO) organization.

Concurrently, the second stage of the pipeline prepares instructions for execution by decoding operation codes and by partially resolving effective operand addresses. This two stage pipeline allows the IEU to execute a new instruction immediately. This design speeds the 9655 system's execution by reducing instruction overhead.

Hardware Technology

The 9655 makes extensive use of the latest available gate array and advanced Schottky TTL components. These high-density components offer improved reliability while consuming less power than those previously used.

I/O Transfer Efficiency

For maximum speed, burst-mode transfer mechanisms support DMA data transfers. Burst-mode I/O transfers 64-bits of data at a time over the 5Mb I/O bus. It also enhances the performance of virtual memory management by increasing the speed of disk-to-main memory page transfers.

Cache Memory

Cache memory greatly reduces the 9655 system's effective memory access time by storing frequently used instructions and data in fast buffer memory within the central processor. The high-speed components and efficient circuit design provide a cache access time of only 80 nanoseconds. With a 16Kb capacity and a 95% hit rate, cache memory gives the 9655 an effective main memory access time of only 132 nanoseconds. In addition, an efficient "write through" algorithm eliminates bus delays during main memory writes by letting information be written through cache.

Quad Precision Floating Point and Commercial Instructions

The 9655 instruction set is a superset of the instructions used on other members of the 50 Series product line. Quad precision floating point is available on the 9655 (also available with the 2655,TM 9750,TM and 9955TM processors). In this format, the fraction (mantissa) has been expanded to 96-bits from the 48-bits available with double-precision floating point. The floating point logic manipulates the mantissa and the exponent in parallel to reduce execution time. The extra accuracy of quad precision floating point will be invaluable in certain scientific and mathematical applications that need extra digits for precision. Prime's FORTRAN compiler (F77) has been enhanced to support quad precision floating point. Other 50 Series systems, without the instruction set enhancements, can emulate quad precision floating point by automatic invocation of software routines. This preserves program compatibility between the 9655 and other 50 Series systems.

Instruction Set

The Prime instruction set takes advantage of the 9655 system's 52-bit data paths and 32-bit internal architecture, and the expanded number of registers in the system to achieve maximum performance. Designed to increase speed in commercial high-level language execution, the 9655 instruction set features optimized machine instructions for decimal and character string operations. In addition, frequently used Prime INFORMATIONTM instructions have been implemented in microcode to enhance performance.

The more than 550 instructions enhance operating system communication, data handling, and process coordination. Highly flexible address formation techniques let all instructions use any one of four user-accessible base registers and 32-bit indirect words in any combination. This lets all memory reference instructions access the entire virtual address space.

Because the 9655 instruction set is compatible with the standard 50 Series instruction set, user programs written for any Prime system can run on the 9655 without modification. This also means applications written and compiled on the 9655 will run on other members of the 50 Series family without modification.

Diagnostic Processor

The 9655 diagnostic processor performs a variety of system integrity, administrative and monitoring functions. The diagnostic processor controls the two floppy disks used for operational and diagnostic microcode loading. The Status Panel, with operator switches and indicators, interfaces to the diagnostic processor, as does the operator's console.

The diagnostic processor controls the automatic system startup feature. With a single push of a button, the multi-user PRIMOS operating system is brought up on the 9655. Time of day and date are provided to PRIMOS (at the appropriate point) from a battery-operated clock on the diagnostic processor, which is trickle-charged when the 9655 is running. The clock will keep time for up to one month when the 9655 has no power.

Environmental Sensing

By monitoring the system airflow and temperature sensors, the diagnostic processor can detect problems with the computer room air conditioning, or an internal cooling problem. The PRIMOS operating system then notifies the operator's console of any malfunctions, so corrective action can be taken before any damage is done.

Local and Remote Diagnostics

The diagnostic processor also provides the ability for local and remote diagnostics. This provides fast, effective trouble-shooting for identifying a hardware problem and for performing comprehensive system diagnostics.

By depressing a "Remote Enable" button on the control panel, the local system operator or administrator initiates remote access. A second button places the remote terminal in monitoring mode, and gives the remote terminal the ability to control the system as if it were the local system console. A Customer Service Representative, when in control mode, can completely run the system from a remote terminal, including tasks such as bootloading and on-line operations.

Two indicators display the state of the remote communications link; one indicates a remote user has been given the ability to dial into the system and monitor operations; the second indicates whether a remote access is in progress, and flashes when the remote user has been given control of the system.

Microcode Diagnostics

Like all other members of the 50 Series product line, the 9655 has a microprogrammed central processor. But where the older members of the 50 Series have their microcode held in unalterable read-only memories, the control store for the 9655 is built from random access memory. Two diskette drives are supplied as an integral part of the 9655. Memory is automatically loaded from one diskette upon application of power to the 9655. The other diskette is used for loading diagnostic microcode. A portion of the diagnostic microcode is automatically loaded into the control store, and run, during 9655 system startup. Following successful verification of the integrity of the central processor and memory interface, the operational microcode replaces the diagnostic microcode in the control store. Should verification fail, the Prime Customer Service Representative can run a second level of diagnostic microcode on the 9655. This second level diagnostic microcode is very extensive and will overlay the control store up to five times. This will pinpoint any problem to a specific area of the central processor and/or memory interface.

Software

The PRIMOS operating system supports both interactive and batch processing on all 50 Series systems. The operating system supports re-entrant procedures, letting many users share a single copy of a software module.

A wide range of high-level, industry-standard languages run on Prime systems. Available languages include FORTRAN 77, ANSI 74 COBOL, Pascal, PL/I Subset G, C, BASIC and RPG II. The Prime Macro Assembler, the Source-Level Debugger, and EMACS, the extendable screen editor, support these standard languages.

Prime offers a comprehensive family of data management products. Central to these are MIDASPLUS™ and PRISAM™ indexed sequential access managers, and CODASYL-compliant Prime DBMS. Complementing these data managers are: FORMS for screen management, the PRIME/POWER+ product for query and reporting on MIDASPLUS and PRIMOS files, and the DISCOVER™ product for query and reporting on PRISAM and Prime DBMS files.

Other Prime software offerings include PRIMEWAY™ development and transaction management system, Prime INFORMATION software, a fourth generation, relationally-based data management product, and the Prime Office Automation System (Prime OAS).

For CAD/CAM/CAE applications, Prime offers the PRIME MEDUSA™ design and drafting package; the Product Design Graphics System™ (PDGS)™, GNC™ Graphical Numerical Control, and the SAMMIE™ ergonomic design software packages. In addition, a large library of application packages is available from the Prime Users Library Service (PULSE) and from the Joint Marketing Agreements (JMA) that we have with third-party software houses.

Networking

The 9655 is ideal for networking and distributed processing environments. PRIMENET networking software lets Prime computers communicate among themselves, with terminals, and with other manufacturers' systems. Using PRIMENET facilities, up to 63 remote users can remotely log into another system. These users can share files among systems, and develop distributed applications. For local area networks, the 9655 can be attached in a high-speed network, via the RINGNET™ system, with any other 50 Series system. The ring provides inter-system communication via a coaxial cable or fiber optics for Prime systems using PRIMENET software and a PRIMENET node controller.

The 9655 supports all Prime communications hardware controllers. Available communications hardware options include IBM BISYNC for HASP and 2780/3780; High-Level Data Link Control (HLDC) protocol for X.25 packet-switching networks; Control Data 200UT; UNIVAC 1004; Honeywell GRTS; ICL 7020; and XBM.

Prime's Distributed Processing Terminal Executive (DPTX) lets the 9655 emulate and support 3271/3277 Display Systems.

The PRIME/SNA™ product family allows Prime systems to coexist with networks based on IBM's system network architecture, SNA.

Peripherals

The 9655 supports a wide range of peripheral products for mass storage, interactive data entry/retrieval, and hardcopy output. Peripherals are upwardly compatible across the Prime product line for easy, economical system upgrade.

The 9655 can support all Prime disk devices in the product line including the 315Mb and 675Mb Winchester disk subsystems.

The 9655 has the ability to store up to 10 billion bytes of data on-line using magnetic disk subsystems. Magnetic tape products include a 50-ips, 6250-bpi GCR unit with up to eight tape drives available per system, a 75-ips, 800/1600-bpi tape unit, streaming tape drive, or cartridge tape unit.

A variety of printing devices – band printers, matrix printer, letter-quality printers and matrix plotters – are supported by the 9655. The system's printer interface can be a serial asynchronous communications line or a parallel interface device used with the unit record controller. Video and hardcopy terminals are also available. The 9655 can support up to 128 terminals for local and remote input.

Regulation and Power

The 9655 has been certified to meet U.S. Safety and Noise Emission Regulations – U.L. and FCC EMI – as well as Canadian safety regulations. The system can be configured for North American and European ac power sources. Support for an uninterruptible power supply (UPS) is standard on the 9655.

Specifications

System

Main Memory:	Up to 8Mb
Cache Memory:	16Kb
Effective Memory	
Access Time:	132 nanoseconds
Virtual Address Space:	512Mb
Terminals	
Supported:	Up to 128
Disk Storage:	Up to 10 gigabytes

Environmental

Noise Level:	Less than 65 DBA
Operating	15-32° C
Temperature:	(59-90 ° F)
Operating	30-80%
Humidity:	(non-condensing)
Operating	
Altitude:	0-3.5Km (0-12,000 ft.)
Heat Dissipation:	5700 BTU/HR
	1425 Kcal

Physical

Height:	135cm (53")
Width:	68cm (26.5")
Depth:	89cm (35")

Power

Electrical	104-127 Volts (60Hz),
Requirements:	208-254 (50 Hz)
Electrical	
Consumption:	2.5 KVA

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