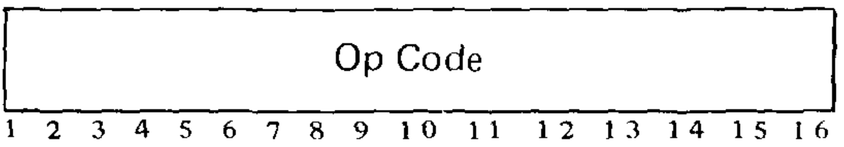
Prime Computer Instruction Summary

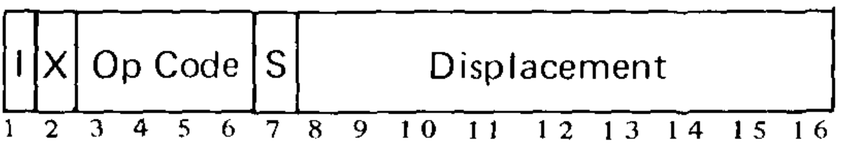
A summary of machine language instructions for Prime 100, 200 and 300 central processors.

Instruction Formats

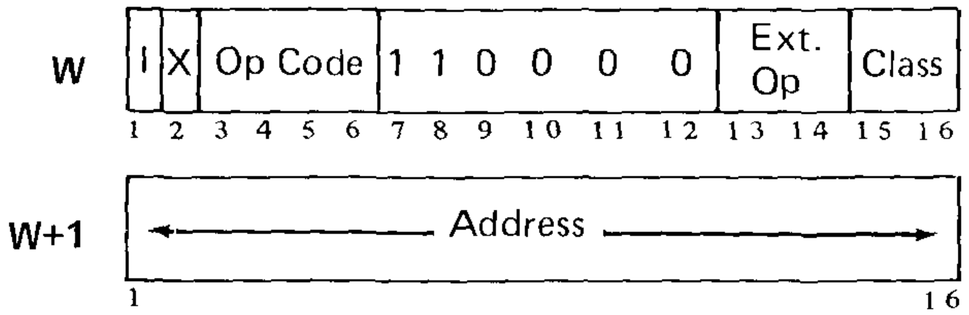
GENERIC (G)



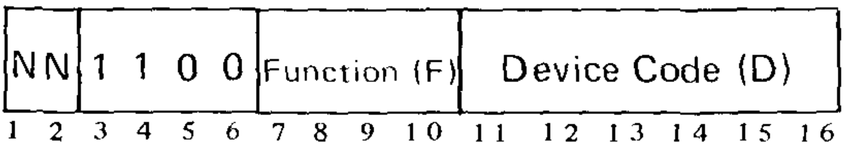
MEMORY REFERENCE (MR)



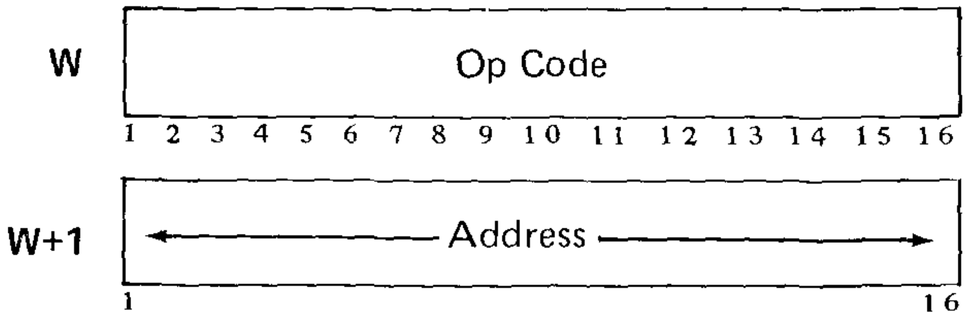
EXTENDED MEMORY REFERENCE (XMR)



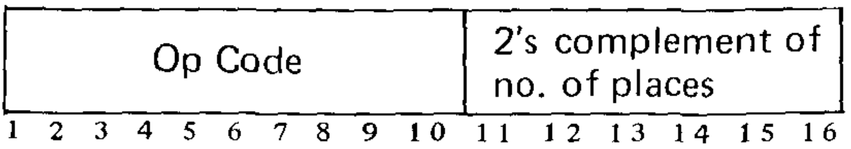
INPUT/OUTPUT (I/O)



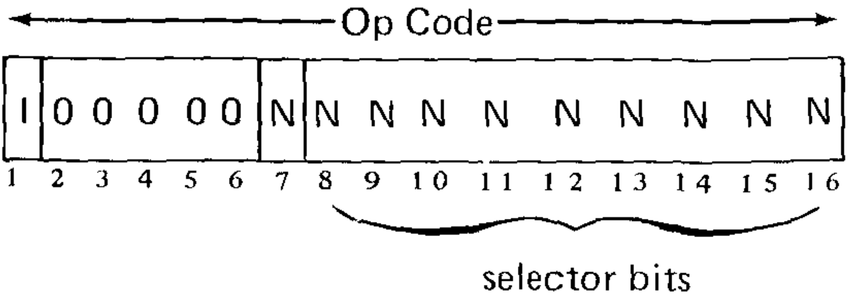
VIRTUAL MEMORY (XG)



SHIFT (SH)

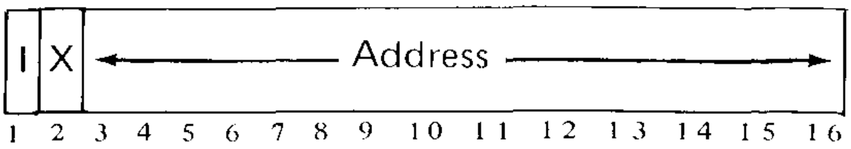


GENERIC SKIP GROUP (G)

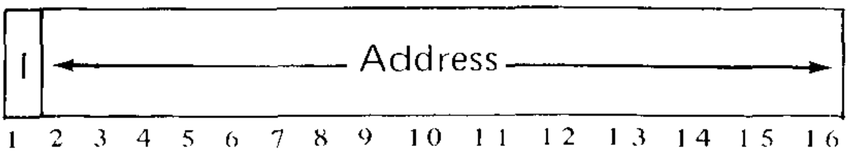


Address & Data Formats

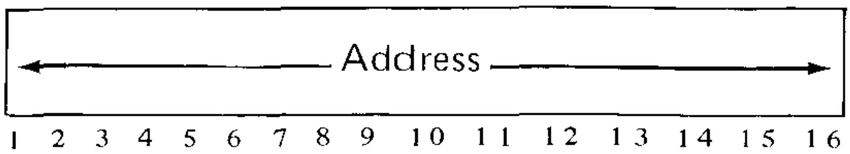
INDIRECT ADDRESS 16S Mode



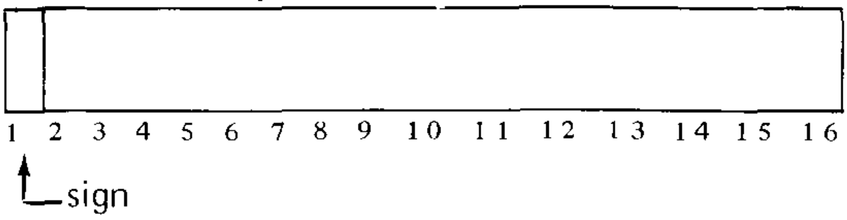
INDIRECT ADDRESS 32S or 32R Mode



INDIRECT ADDRESS 64R Mode

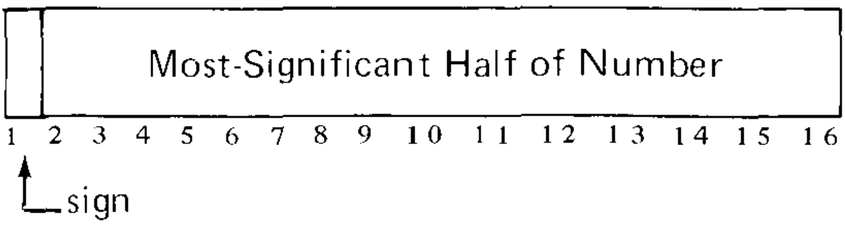


FIXED-POINT, SINGLE-PRECISION DATA

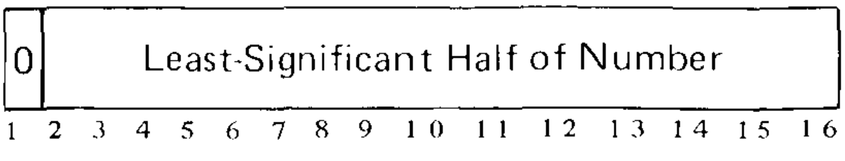


FIXED-POINT, DOUBLE-PRECISION DATA

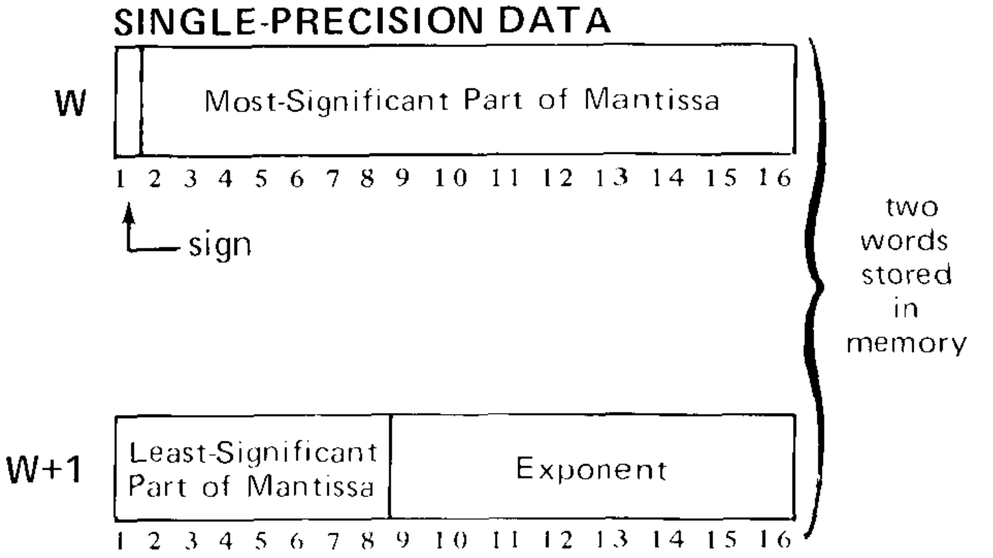
W



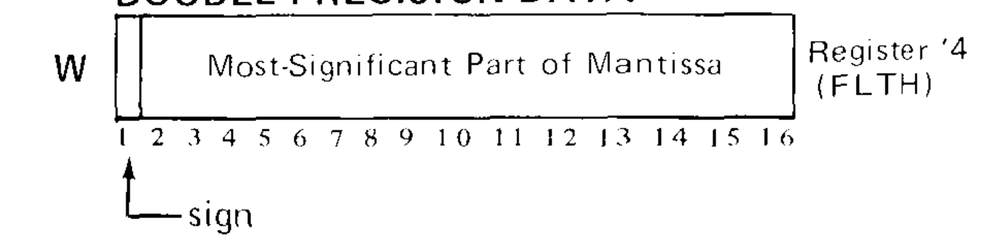
W+1

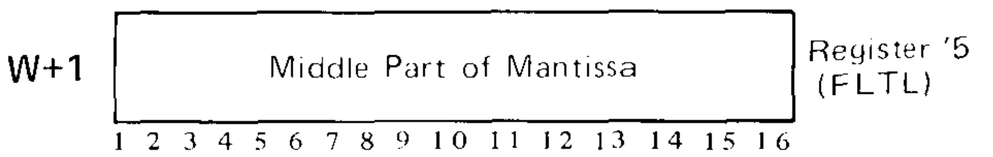


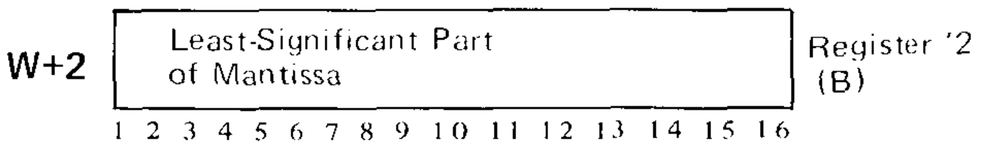
FLOATING POINT, SINGLE-PRECISION DATA

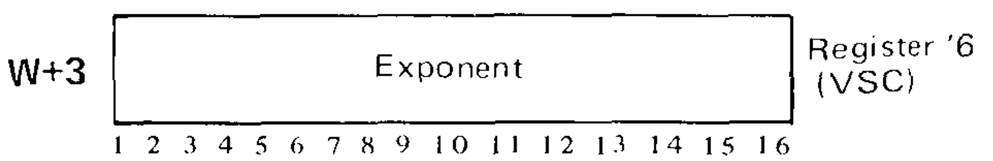


FLOATING POINT, DOUBLE-PRECISION DATA









NOTES:
1. Registers '4, '5, '2, '6 = DFAC (Double Floating Accumulator).
2. Registers '4, '5, '6 = FAC (Floating Accumulator).
3. For Single Precision FP, Register '2 is not used and the least-significant part of the mantissa is loaded into Register '5.

Mnemonic Op Codes

MNEMONIC	OCTAL	FUNCTION
A1A	141206	Add One to A
A2A	140304	Add Two to A
ACA	141216	Add C to A
ADD	06	Add to A
ALL	0414	A Left Logical
ALR	0416	A Left Rotate
ALS	0415	A Left Shift
ANA	03	And With A
A0A	141206	Add One to A
ARL	0404	A Right Logical
ARR	0406	A Right Rotate
ARS	0405	A Right Shift
CAI	000411	Clear Active Interrupt
CAL	141050	Clear A Left Byte
CAR	141044	Clear A Right Byte
CAS	11	Compare & Skip
CAZ	140214	Compare A With Zero & Skip
CEA	000111	Compute Effective Address
CHS	140024	Change Sign
CMA	140401	Complement A
CRA	140040	Clear A
CRB	140014	Clear B
CREP	10 02	Call Recursive Procedure
CRL	140010	Clear Long
CSA	140320	Copy Sign Of A
DAD	06	Double Precision Add
DBL	000007	Enter Dbl Prec Mode
DFAD	06 02	Dbl Prec Floating Add
DFCM	140574	Dbl Prec Floating Complement
DFCS	11 02	Dbl Prec Floating Compare & Skip
DFDV	17 02	Dbl Prec Floating Divide
DFLD	02 02	Dbl Prec Floating Load
DFMP	16 02	Dbl Prec Floating Multiply
DFSB	07 02	Dbl Prec Floating Subtract
DFST	04 02	Dbl Prec Floating Store
DIV	17	Divide
DLD	02	Double Load
DRX	140210	Decrement Replace Index & Skip
DSB	07	Double Precision Subtract
DST	04	Double Store
E16S	000011	Enter 16K Sectored Mode
E32R	001013	Enter 32K Relative Mode
E32S	000013	Enter 32K Sectored Mode
E64R	001011	Enter 64K Relative Mode
EAA	01 01	Effective Address to A Register
EMCM	000503	Enter Machine Check Mode
ENB	000401	Enable Interrupt
ENTR	01 03	Enter Recursive Procedure
EPMJ	000217	Enter Page Mode & Jump
EPMX	000237	Enter Page Mode & Jump to XCS

ERA	05	Exclusive Or to A
ERMJ	000701	Enter Restricted Mode & Jump
ERMX	000721	Enter Restricted Mode & Jump to XCS
ESIM	000415	Enter Std Interrupt Mode
EVIM	000417	Enter Vectored Interrupt Mode
EVMJ	000703	Enter Virtual Mode & Jump
EVMX	000723	Enter Virtual Mode & Jump to XCS
FAD	06 01	Floating Add
FCM	140530	Floating Complement
FCS	11 01	Floating Compare & Skip
FDV	17 01	Floating Divide
FLD	02 01	Floating Load
FLOT	140550	Float (A & B) as Integer Normalized
FLX	15 01	Load Floating Index
FMP	16 01	Floating Multiply
FRAC	140570	Fix as Fraction
FRN	140534	Round-Up
FSB	07 01	Floating Subtract
FSGT	140515	Floating Skip if >0
FSLE	140514	Floating Skip if $<=0$
FSMI	140512	Floating Skip if Minus
FSNZ	140511	Floating Skip if Not 0
FSPL	140513	Floating Skip if Plus
FST	04 01	Floating Store
FSZE	140510	Floating Skip if 0
HLT	000000	Halt
IAB	000201	Interchange A & B
ICA	141340	Interchange Bytes of A
ICL	141140	Interchange Bytes of A & Clear Left Byte
ICR	141240	Interchange Bytes of A & Clear Right Byte
IMA	13	Interchange Memory & A
INA	54	Input to A From I/O
INH	001001	Inhibit Interrupt
INK	000043	Input Keys to A
INT	140554	Fix as Integer
IRS	12	Increment Memory Replace & Skip
IRX	140114	Increment Replace Index & Skip
ISI	000511	Input Serial Interface
JDX	15 02	Jump & Decrement X
JEQ	02 03	Jump if Equal to 0
JGE	07 03	Jump if $>=0$
JGT	05 03	Jump if >0
JIX	15 03	Jump & Increment X
JLE	04 03	Jump if $<=0$
JLT	06 03	Jump if <0
JMP	01	Unconditional Jump
JNE	03 03	Jump if $\neq 0$
JST	10	Jump to Subroutine
JSX	35 03	Jump & Store Return in X
LDA	02	Load A
LDX	35	Load Index (not indexed)
LEQ	140413	Convert A=0 to True
LF	140416	Convert A to False
LGE	140414	Convert A $>=0$ to True

LGL	0414	A Left Logical
LGR	0404	A Right Logical
LGT	140415	Convert A > 0 to True
LLE	140411	Convert A < = 0 to True
LLL	0410	Long Left Logical
LLR	0412	Long Left Rotate
LLS	0411	Long Left Shift
LLT	140410	Convert A < 0 to True
LMCM	000501	Leave Machine Check Mode
LNE	140412	Convert A ≠ 0 to True
LPMJ	000215	Leave Page Mode & Jump
LPMX	000235	Leave Page Mode & Jump to XCS
LRL	0400	Long Right Logical
LRR	0402	Long Right Rotate
LRS	0401	Long Right Shift
LT	140417	Convert A to True
MPY	16	Multiply
NOP	101000	Skip on None (NOP)
NOP	000001	No Operation
NRM	000101	Normalize
OCP	14	Output Control Pulse
OSI	000515	Output Serial Interface
OTA	74	Output A to I/O
OTK	000405	Output A to Status Keys
PID	000211	Position For Integer Divide
PIM	000205	Position Following Integer Multiply
RCB	140200	Reset C-Bit
RMC	000021	Reset Machine Check Flag
RTN	000105	Return From Recursive Procedure
S1A	140110	Subtract One From A
S2A	140310	Subtract Two From A
SAR N	100260+ (N-1)	Skip On A Bit N Reset
SAS N	101260+ (N-1)	Skip On A Bit N Set
SCA	000041	Load Shift Counter Into A
SCB	140600	Set C-Bit
SGL	000005	Enter Single Precision Mode
SGT	100220	Skip if A Greater Than Zero
SKP	100000	Skip Unconditionally
SKS	34	Skip if I/O Device Condition Set
SLE	101220	Skip on A < = Zero
SLN	101100	Skip on Least Sig. Bit Not 0
SLZ	100100	Skip if Least Sig. Bit Zero
SMCR	100200	Skip if Machine Check Reset
SMCS	101200	Skip if Machine Check Set
SMI	101400	Skip on A Minus
SMK	170020	Set Int Enable Flags According to Mask in A
SNR N	100240+ (N-1)	Skip On Sense Switch N Reset
SNS N	101240+ (N-1)	Skip On Sense Switch N Set
SNZ	101040	Skip if A Not Zero
SOA	140110	Subtract One From A

SPL	100400	Skip on A Plus
SR1	100020	Skip if SS1 Reset
SR2	100010	Skip if SS2 Reset
SR3	100004	Skip if SS3 Reset
SR4	100002	Skip if SS4 Reset
SRC	100001	Skip if C-Bit Reset
SS1	101020	Skip if SS1 Set
SS2	101010	Skip if SS2 Set
SS3	101004	Skip if SS3 Set
SS4	101002	Skip if SS4 Set
SSC	101001	Skip if C-Bit Set
SSM	140500	Set Sign Minus
SSP	140100	Set Sign Plus
SSR	100036	Skip if All Sense Switches (1-4) Reset
SSS	101036	Skip if Any Sense Switch (1-4) Set
STA	04	Store A
STX	15	Store Index (not indexed)
SUB	07	Subtract From A
SVC	000505	Supervisor Call
SZE	100040	Skip if A Zero
TCA	140407	Two's Complement A
VIRY	000311	Execute Verification Routine
XCA	140104	Transfer A To B & Clear A
XCB	140204	Transfer B To A & Clear B
XEC	01 02	Execute Effective Address Contents As Next Inst.

Key To Abbreviations & Symbols

A	A Register
An	A Register, bit n
An . . . Am	A Register, bits n to m (also shown as An-m)
B	B Register
Bn	B Register, bit n
C	Carry Bit (C-Bit)
DFAC	Double Precision Floating Accumulator (registers '04, '05, '02 and '06)
(DFAC)	Contents of Double Precision Floating Accumulator
EA	Effective Address
[EA]	Contents of Effective Address
F	I/O Function Code
FAC	Floating Accumulator (registers '04, '05 and '06)
(FAC)	Contents of Floating Accumulator
FP	Floating Point
G	Generic Instruction
XG	Generic Instruction, 2-Word Format
HSA	High Speed Arithmetic
I/O	Input/Output Instruction
LSB	Least Significant Bit
MR	Memory Reference Instruction

XMR	Memory Reference, 2-Word Format
MSB	Most Significant Bit
OV	Overflow
P	Program Counter
P300	Prime 300 Instruction Set
Loc '6	Shift Counter '6
S	Standard
SH	Shifting Instructions
SS	Sense Switch
X	Index Register
( )	Contents of Hardware Register
[ ]	Contents of Memory Location
→	Replaces
##	CPU must be in Double Precision Mode
*	Multiplication
/	Division
$	Hexadecimal Number Follows
'	Octal Number Follows

Prime Instruction Set

Mnemonic	OP Code	Function	Type	Availability
ADDRESS MODE SELECTION				
E16S	000011	Enter 16K Sectored Mode	G	S
E32S	000013	Enter 32K Sectored Mode	G	S
E32R	001013	Enter 32K Relative Mode	G	S
E64R	001011	Enter 64K Relative Mode	G	S
CONTROL				
CEA	000111	EA → A	G	S
EMCM	000503	Enter Machine Check Mode	G	S
HLT	000000	Halt Computer Operation	G	S
LMCM	000501	Leave Machine Check Mode	G	S
NOP	000001	No Operation	G	S
RCB	140200	Reset C-Bit	G	S
RMC	000021	Reset Machine Check Flag	G	S
SCB	140600	Set C-Bit	G	S
SVC	000505	Supervisor Call	G	S
LOAD & STORE INSTRUCTIONS				
IMA	13	[EA] → (A) & (A) → [EA]	MR	S
LDA	02	[EA] → A	MR	S
LDX	35	[EA] → X (not indexed)	MR	S
STA	04	(A) → EA	MR	S
STX	15	(X) → EA (not indexed)	MR	S
JUMP INSTRUCTIONS				
JMP	01	Unconditional Jump, [EA] → P	MR	S
JST	10	P+1 → EA; P 3-16 → EA 3-16 in 16S mode; P 2-16 → EA 2-16 in 32S or 32R mode; P 1-16 → EA 1-16 in 64R mode; other EA bits not affected; next instruction at EA+1	MR	S
SKIP INSTRUCTIONS				
DRX	140210	(X)-1 → X, if result = 0 skip next instruction	G	S
IRS	12	[EA] + 1 → EA, if result = 0 skip next instruction	MR	S
IRX	140114	(X) + 1 → X, if result = 0 skip next instruction	G	S
SAR N	100260 + (N-1)	Skip on A Bit N Reset	G	S
SAS N	101260 + (N-1)	Skip on A Bit N Set	G	S
SGT	100220	Skip Next Inst. if A > 0	G	S
SLE	101220	Skip Next Inst. if A < = 0	G	S
SMCR	100200	Skip Next Instruction If Machine Check is Reset	G	S
SMCS	101200	Skip Next Inst. if Machine Check is Set	G	S

SNR N	100240 + (N-1)	Skip on SS N Reset	G	S
SNS N	101240 + (N-1)	Skip on SS N Set	G	S

SKIP GROUP

		Selector Bits	Bit 7	Skip On Condition		
NOP	101000		1	Skip on None (NOP)	G	S
SEQ	100040	11	0	Skip on A = 0	G	S
SGE	100400	8	0	Skip on A >= 0	G	S
SKP	100000		0	Skip Unconditionally	G	S
SLE	101220	8	1	Skip on A <=0		
SLN	101100	10	1	Skip on LSB Non Zero (A16 = 1)	G	S
SLZ	100100	10	0	Skip on LSB Zero (A16 = 0)	G	S
SMI	101400	8	1	Skip on A Minus (A1 = 1)	G	S
SNZ	101040	11	1	Skip on A Nonzero	G	S
SPL	100400	8	0	Skip on A Plus (A1 = 0)	G	S
SR1	100020	12	0	Skip on SS1 Reset	G	S
SR2	100010	13	0	Skip on SS2 Reset	G	S
SR3	100004	14	0	Skip on SS3 Reset	G	S
SR4	100002	15	0	Skip on SS4 Reset	G	S
SRC	100001	16	1	Skip on C-Bit Reset	G	S
SS1	101020	12	1	Skip on SS1 Set	G	S
SS2	101010	13	1	Skip on SS2 Set	G	S
SS3	101004	14	1	Skip on SS3 Set	G	S
SS4	101002	15	1	Skip on SS4 Set	G	S
SSC	100001	16	0	Skip on C-Bit Reset	G	S
SSR	100036	12-15	0	Skip on All SS (1-4) Reset	G	S
SSS	101036	12-15	1	Skip on Any SS (1-4) Set	G	S
SZE	100040	11	0	Skip on A = 0	G	S

COMPARE

CAS	11	If (A) > [EA] execute next Instruction, if (A)=[EA] skip next inst, if (A) < [EA] skip next two instructions.	MR	S
CAZ	140214	If (A) >0 execute instruction, if (A) = 0 skip next instruction, if (A) <0 skip next two inst.	MR	S

REGISTER OPERATE

CRA	140040	Clear A, 0 → A	G	S
CRB	140014	Clear B, 0 → B	G	S
CRL	140010	Clear Long, 0 → A & B	G	S
IAB	000201	(A) → (B) & (B) → (A)	G	S
XCA	140104	(A) → B, 0 → A	G	S
SCB	140204	(B) → A, 0 → B	G	S

BYTE MANIPULATION

CAL	141050	0 → A 1-8, A 9-16 unchanged	G	S
CAR	141044	0 → A 9-16, A 1-8 unchanged	G	S
ICA	141340	A 1-8 → A 9-16, A 9-16 → A 1-8	G	S
ICL	141140	A 1-8 → A 9-16, 0 → A 1-8	G	S
ICR	141240	A 9-16 → A 1-8, 0 → A 9-16	G	S

SHIFT INSTRUCTIONS

ALL	0414	[C] ← [A1 . . . A16] ← 0	SH	S
ALR	0416	[A1 . . . A16] → [C]	SH	S
ALS	0415	[A1] ← [A2 . . . A16] ← 0 OV → [C]	SH	S
ARL	0404	0 → [A1 . . . A16] → [C]	SH	S
ARR	0406	[C] → [A1 . . . A16]	SH	S
ARS	0405	[A1] → [A2 . . . A16] → [C]	SH	S
LGL	0414	[C] ← [A1 . . . A16] ← 0	SH	S
LGR	0404	0 → [A1 . . . A16] → [C]	SH	S
LLL	0410	[C] ← [A1 . . . A16] ← [B1 . . . B16] ← 0	SH	S
LLR	0412	[A1 . . . A16 B1 . . . B16] → [C]	SH	S
LLS	0411	[A1] ← [A2. . . A16 B1 B2. . . B16] B16 ← 0, OV → [C]	SH	S
LRL	0400	0 → [A1 . . . A16] → [B1 . . . B16] → [C]	SH	S
LRR	0402	[C] → [A1 . . . A16 B1 . . . B16]	SH	S
LRS	0401	[A1] → [A2 . . . A16 B1 B2 . . . B16] B16 → [C]	SH	S

LOGICAL

ANA	03	And with A, (A) & [EA] → A	MR	S
CMA	140401	Complement A	G	S
ERA	05	Exclusive Or to A, (A) Exclusive Or [EA] → A	MR	S

LOGICIZE

LEQ	140413	If A=0 then 1 → A, else 0 → A	G	S
LF	140416	False, 0 → A	G	S
LGE	140414	If A >=0 then 1 → A, else 0 → A	G	S
LGT	140415	If A >0 then 1 → A, else 0 → A	G	S
LLE	140411	If A <=0 then 1 → A, else 0 → A	G	S
LLT	140410	If A <0 then 1 → A, else 0 → A	G	S
LNE	140412	If A not = 0 then 1 → A, else 0 → A	G	S
LT	140417	True, 1 → A	G	S

SINGLE PRECISION FIXED POINT ARITHMETIC

ACA	141216	(C) + (A) → A, OV → C	G	S
ADD	06	Add, [EA] + (A) → A, OV → C	MR	S
AOA	141206	(A)+1 → A, OV → C	G	S
A1A	141206	see AOA	G	S
A2A	140304	(A)+2 → A, OV → C	G	S

CHS	140024	Change Sign	G	S
CSA	140320	A1 → C, 0 → A1	G	S
SOA	140110	(A)-1 → A, OV → C	G	S
SSM	140500	1 → A1	G	S
SSP	140100	0 → A1	G	S
SUB	07	Subtract, (A)-[EA] → A, OV → C	MR	S
S1A	140110	See SOA	G	S
S2A	140310	(A)-2 → A, OV → C	G	S
TCA	140407	0-(A) → A, OV → C	G	S

SGL-DBL PRECISION MODE CHANGE

DBL	000007	Enter Double Prec Mode	G	S
SGL	000005	Return to Single Prec Mode	G	S

DOUBLE PRECISION FIXED POINT ARITHMETIC

DAD	06	[EA, EA+1] + (A,B) → A1 . . . A16,B2 . . . B16 0 → B1 OV → C	G	S
DIV	17	(A,B)/[EA] → A, remain → B improper divide status → C	MR	HSA
DSB	07	(A & B) - [EA & EA+1] → A1 . . . A16 & B2 . . . B16; 0 → B1	MR	S
MPY	16	(A)*[EA] → A&B, OV → C	MR	HSA
PID	000211	A2 . . . A16 → B2 . . . B16, 0 → A1, B1 → A2 . . . A16	G	HSA
PIM	000205	B2 . . . B16 → A2 . . . A16, 0 → A1	G	HSA

NOTE: Processor must be in double precision mode for DAD and DSB to execute.

DOUBLE PREC FIXED PT LOAD AND STORE

DLD	02	[EA] → A, [EA] + 1 → B	MR	S
DST	04	(A) → EA, (B) → EA + 1	MR	S

NOTE: Processor must be in double precision mode for DLD and DST to execute.

SINGLE PRECISION FLOATING PT ARITHMETIC

FAD	06 01	(FAC)+[EA] → FAC, OV → C	XMR	FP
FCM	140530	Complement, -(FAC) → FAC, OV → C	G	FP
FDV	17 01	(FAC)/[EA] → FAC, OV → C	XMR	FP
FMP	16 01	(FAC)*[EA] → FAC, OV → C	XMR	FP
FRN	140534	24 MSB of mantissa+(0.5*LSB) → 24 MSB of mantissa. OV → C	G	FP
FSB	07 01	(FAC)-[EA] → FAC, OV → C	XMR	FP

SINGLE PREC FLOATING LOAD STORE AND SKIPS

FCS	11 01	If (FAC) > [EA] execute next inst., if (FAC) = [EA] skip next inst., if (FAC) < [EA] skip next two instructions	XMR	FP
FLD	02 01	Floating Load, [EA] → FAC	XMR	FP
FLOT	140550	(A & B) as an integer → FAC normalized	G	FP

FRAC	140570	Fractional part of (FAC) → A & B, scaled with binary point between A1 & A2, OV → C	G	FP
FSGT	140515	If ('04) > 0 skip next inst.	G	FP
FSLE	140514	If ('04) ≤ 0 skip next inst.	G	FP
FSMI	140512	If ('04) < 0 skip next inst.	G	FP
FSNZ	140511	If ('04) not = 0 skip next inst.	G	FP
FSPL	140513	If ('04) ≥ 0 skip next inst.	G	FP
FST	04 01	Floating Store (FAC) → EA	XMR	FP
FSZE	140510	If ('04) = 0 skip next inst.	G	FP
INT	140554	Integer Part Of (FAC) → A & B, OV → C	G	FP

NOTE: for single precision floating pt overflow or exceptions, vector through '74
Loc '11 = $100 for exponent
Loc '11 = $101 for divide by 0
Loc '11 = $102 for store, loc '12 = EA
Loc '11 = $103 for int exception

DOUBLE PRECISION FLOATING PT ARITHMETIC

DFAD	06 02	(DFAC)+[EA]→DFAC, OV → C	XMR	FP
DFCM	140574	(DFAC)=0-(DFAC), OV → C	G	FP
DFDV	17 02	(DFAC)/[EA] → DFAC, OV → C	XMR	FP
DFMP	16 02	(DFAC)*[EA] → DFAC, OV → C	XMR	FP
DFSB	07 02	(DFAC)-[EA] → DFAC, OV → C	XMR	FP

DBL PRECISION FLOATING PT LOAD, STORE AND SKIP

DFCS	11 02	If (DFAC) < 0 execute next instruction, if (DFAC) = 0 skip next instruction, if (DFAC) > 0 skip next two instructions	XMR	FP
DFLD	02 02	[EA] → DFAC	XMR	FP
DFST	04 02	(DFAC) → EA	XMR	FP

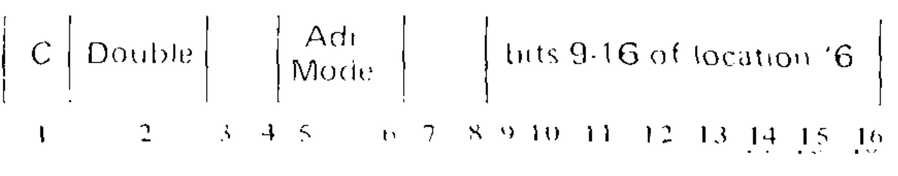
NOTE: For double precision floating pt overflow or exception,
vector through '74
Loc '11 = $200 for exponent
Loc '11 = $201 for divide by 0

NORMALIZE

NRM	000101	|A1|┌┤A2...A16|B1|B2...B16| → 0 Until A2 not = A1, number of shifts → reg '06	G	HSA
SCA	000041	('06 9-16) → A 9-16, 0 → A 1-8	G	S

STATUS KEYS

INK	000043	Status Keys → A, where A=	MR	S



Bits 5-6	Adr. Mode
00	16S
01	32S
10	64R
11	32R

OTK	000405	Output Keys, A 1-6 → Keys, A 9-16 → '6 9-16, 0 → '6 1-8	MR	S

PROGRAMMED INPUT/OUTPUT

INA	54	If device D ready, input info as specified by function F and skip next inst. If ready state irrelevent, perform function F on device D and go to next inst. If device not ready, do not perform function F on device D, but execute next inst. (INA to device 20 never skips).	I/O	S
OCP	14	Output control pulse for function F to device D	I/O	S
OTA	74	If device D is ready, send (A) to device D for purpose specified by F. Handle ready status as in INA. OTA to device 20 does not skip.	I/O	S
SKS	34	Skip next instruction if condition C in device D is true.	I/O	S

CONTROL PANEL COMMUNICATION

INA 1420	131420	Read Control Panel PROM	I/O	S
INA 1620	131620	Input Sense Sws 1-16 → A1-16	I/O	S
INA 1720	131720	Input Data Sws 1-16 → A1-16	I/O	S
OTA1720	171720	Load Lights/PROM Address Register	I/O	S

NOTE: these instructions do not skip

PROCESSOR SERIAL INTERFACE

ISI	000511	Serial Interface Lines → A 13-16, line 1 → A13, etc.	G	S
OSI	000515	A 13-16 → Serial Interface Lines, A13 → line 1, etc.	G	S

INTERRUPT

CAI	000411	Clear Active Interrupt	G	S
ENB	000401	Enable External Interrupts	G	S
ESIM	000415	Enter Std Interrupt Mode (interrupt through '63)	G	S
EVIM	000417	Enter Vectored Interrupt Mode	G	S
INH	001001	Inhibit External Interrupts	G	S
SMK	170020	Set up Interrupt Enable Flags According to Mask in A	G	S

VIRTUAL MEMORY INSTRUCTIONS

EPMJ	000217	Enter Page Mode & Jump	XG	P300
ERMJ	000701	Enter Restricted Mode & Jump	XG	P300
EPMX	000237	Enter Page Mode & Jump to XCS	XG	P300
ERMX	000721	Enter Restricted Mode & Jump to XCS	XG	P300
EVMJ	000703	Enter Virtual Mode & Jump	XG	P300
EVMX	000723	Enter Virtual Mode & Jump to XCS	XG	P300
LPMJ	000215	Leave Page Mode & Jump	XG	P300
LPMX	000235	Leave Page Mode & Jump to XCS	XG	P300

VERIFICATION

VIRY	000311	Execute verification routine, if no error detected, skip next inst; if error detected, execute next inst. (A) = failed-test #.	G	MICRO-VFY

EXTENDED TWO-WORD JUMP INSTRUCTION SET

JDX	15 02	Decrement X; if X not = 0, jump	SMR	P300
JEQ	02 03	Jump if A = 0	XMR	P300
JGE	07 03	Jump if A >= 0	XMR	P300
JGT	05 03	Jump if A > 0	XMR	P300
JIX	15 03	Increment X; if X not = 0, jump	XMR	P300
JLE	04 03	Jump if A <= 0	XMR	P300
JLT	06 03	Jump if A < 0	XMR	P300
JNE	03 03	Jump if A not equal to 0	XMR	P300
JSX	35 03	Jump & Store Return in X	XMR	P300

PROCEDURE STACK CONTROL

CREP	10 02	Call Recursive Procedure	XMR	P300
ENTR	01 03	Enter Recursive Procedure	XMR	P300
RTN	000105	Return From Recursive Proc.	G	P300

OTHER EXTENDED INSTRUCTIONS

EAA	01 01	Effective Address to A Reg.	XMR	P300
FLX	15 01	Load Floating Index	XMR	P300
XEC	01 02	Execute Effective Address Contents as Next Instruction	XMR	P300

Instruction Timing

INST	P100	P200	P300 (600 nsec access)	P300 (440 nsec access)
A1A	1.76	1.36	1.28	1.12
A2A	1.76	1.36	1.28	1.12
ACA	1.76	1.36	1.28	1.12
ADD	2.44	1.96	1.88	1.56
ALL	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
ALR	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
ALS	1.76+0.36N	1.28+0.24N	1.28+0.2N	1.12+0.2N
ANA	2.44	1.96	1.88	1.56
AOA	1.76	1.36	1.28	1.12
ARL	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
ARR	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
ARS	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
CAI	1.76	1.28	1.28	1.12
CAL	1.76	1.36	1.28	1.12
CAR	1.76	1.36	1.28	1.12
CAS	3.52	2.16	2.26	1.94
	3.83	2.44	2.48	2.16
	4.24	2.72	2.60	2.36
CAZ	2.12	1.52	1.48	1.32
	2.48	1.80	1.78	1.52
	2.84	2.08	1.88	1.72
CEA	3.24+1.04I	2.84+0.88I	2.16+0.84I	2.04+0.68I
CHS	1.76	1.36	1.28	1.12
CMA	1.76	1.36	1.28	1.12
CRA	1.76	1.28	1.28	1.12
CRB	1.76	1.28	1.28	1.12
CREP	—	—	3.48	3.08
CRL	2.12	1.48	1.48	1.32
CSA	1.76	1.36	1.28	1.12
DAD	4.56	3.56	3.28	2.80
DBL	1.76	1.28	1.28	1.12
DFAD	—	11.51+.72A +1.N	11.0+.64A +.92N	10.04+.64A +.92N
DFCM	—	5.96	6.52	6.20
DFCS	—	5.18	4.725	4.245
DFDV	—	73.3	67.52	66.56
DFLD	—	5.84	5.56	4.60
DFMP	—	56.73	52.62	51.66
DFSB	—	11.51+.72A +1.N	11.0+.64A +.92N	10.04+0.64A +.92N
DFST	—	6.56	5.48	5.00
DIV	13.78	13.24	11.2725	10.9525
DLD	3.72	2.96	2.72	2.24
DRX	2.48 2.12	1.84 1.56	1.78 1.48	1.52 1.32
DSB	3.6	3.32	3.22	2.74
DST	3.72	3.04	2.64	2.32
E16S	1.76	1.28	1.28	1.12
E32S	1.76	1.28	1.28	1.12
E32R	1.76	1.28	1.28	1.12

E64R	1.76	1.28	1.28	1.12
EAA		—	2.52	2.20
EMCM	--	1.28	1.28	1.12
ENB	1.76	1.28	1.28	1.12
ENTR	—	—	3.24	2.84
EPMJ	—	3.72	3.28	2.80
EPMX	—	—	3.28	2.80
ERA	2.44	1.96	1.88	1.56
ERMJ	—	3.72	3.28	2.80
ERMX	—	—	3.28	2.80
ESIM	1.76	1.28	1.28	1.12
EVIM	1.76	1.28	1.28	1.12
EVMJ	—	3.72	3.28	2.80
EVMX	--	—	3.28	2.80
FAD	—	9.35+.48A +.8N	8.75+.48A +.72N	8.11+.48A +.72N
FCM	—	3.96	3.45	3.32
FCS	—	4.71	4.62	3.98
FDV	—	39.46	37.92	37.28
FLD	—	4.6	4.36	3.72
FLOT	—	5.8+.8N	5.2+.72N	4.88+.72N
FLX	—	3.36	3.32	2.84
FMP	—	27.82	25.20	24.56
FRAC	—	4.96+.48N	4.62+.44N	4.3+.44N
FRN	—	3.68	3.32	3.16
FSB	—	9.35+.48A +.8N	8.75+.48A +.72N	8.11+.48A +.72N
FSGT	—	3.12 2.84	2.88 2.68	2.72 2.52
FSLE	—	3.12 2.84	2.88 2.68	2.72 2.52
FSMI	—	3.12 2.84	2.88 2.68	2.72 2.52
FSNZ	—	3.12 2.84	2.88 2.68	2.72 2.52
FSPL	—	3.12 2.84	2.88 2.68	2.72 2.52
FST	—	5.24	4.80	4.40
FSZE	—	3.12 2.84	2.88 2.68	2.72 2.52
HLT	N/A	N/A	N/A	N/A
IAB	2.84	1.88	1.84	1.68
ICA	1.76	1.36	1.28	1.12
ICL	1.76	1.36	1.28	1.12
ICR	1.76	1.36	1.28	1.12
IMA	3.72	2.88	2.72	2.32
INA	3.92 3.2	2.72 2.06	2.64 2.04	2.28 1.88
INH	1.76	1.28	1.28	1.12
INK	3.56	2.44	2.28	2.12
INT	--	6.20+0.6N	5.70+0.62N	5.50+0.62N
IRS	3.16 3.04	2.80 2.64	2.72 2.56	2.33 2.16
IRX	2.48 2.12	1.84 1.56	1.78 1.48	1.52 1.32
ISI	1.76	1.56	1.28	1.32
JDX	—	—	2.72	2.4
JEQ	—	—	2.72	2.4
JGE	—	—	2.72	2.4
JGT	—	—	2.72	2.4
JIX	—	—	2.72	2.4
JLE	—	—	2.72	2.4
JLT	—	—	2.72	2.4

JMP	1.76	1.28	1.28	1.12
JNE	-		2.72	2.4
JST	3.36	2.64	2.56	2.16
JSX	-	-	2.88	2.56
LDA	2.44	1.88	1.88	1.56
LDX	2.44	1.88	1.88	1.56
LEQ	2.48 2.12	1.84 1.64	1.76 1.56	1.60 1.40
LF	2.48	1.84	1.56	1.40
LGE	2.48 2.12	1.84 1.64	1.75 1.56	1.60 1.40
LGL	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
LGR	1.4+0.36N	1.08+0.24N	1.08+0.2N	0.92+0.2N
LGT	2.48 2.12	1.84 1.64	1.76 1.56	1.60 1.40
LLE	2.48 2.12	1.84 1.64	1.76 1.56	1.60 1.40
LLL	1.4+0.72N	1.08+0.48N	1.08+0.4N	0.92+0.4N
LLR	1.4+1.08N	1.08+0.68N	1.08+0.6N	0.92+0.6N
LLS	1.76+0.72N	1.28+0.48N	1.28+0.4N	1.12+0.4N
LLT	2.48 2.12	1.84 1.64	1.76 1.56	1.60 1.40
LMCM	–	1.28	1.28	1.12
LNE	2.48 2.12	1.84 1.64	1.76 1.56	1.60 1.40
LPMJ	–	–	3.28	2.80
LPMX	–	–	3.28	2.80
LRL	1.4+.72N	1.08+.48N	1.08+.4N	0.92+.4N
LRR	1.4+1.08N	1.08+.68N	1.08+.6N	0.92+.6N
LRS	1.4+.72N	1.08+.68N	1.08+.4N	0.92+.4N
LT	2.12	1.64	1.56	1.40
MPY	11.26	10.48	9.04	8.72
NOP	2.48	1.68	1.68	1.52
NRM	3.42+1.08N	2.96+.68N	2.68+.6N	2.24+.6N
OCP	3.2	2.64	2.64	2.48
OSI	2.12	1.48	1.48	1.32
OTA	4.28 2.84	2.84 1.88	2.64 2.04	2.28 1.88
OTK	2.84	2.12	2.04	1.88
PID	2.84	2.08	1.88	1.72
PIM	2.48	1.84	1.68	1.52
RCB	1.76	1.36	1.28	1.12
RMC	-	1.28	1.28	1.12
RTN	-	–	4.36	3.88
S1A	1.76	1.36	1.28	1.12
S2A	1.76	1.36	1.32	1.16
SCA	2.56	2.16	2.08	1.92
SCB	1.76	1.36	1.28	1.12
SGL	1.76	1.28	1.28	1.12
SKP	3.2	2.32	2.12	1.96
SKS	3.56 3.2	3.0 2.52	2.64 2.44	2.48 2.28
SKIPS:				
(ALL)	3.2 2.84	2.32 2.04	2.12 1.92	1.96 1.76
SMK	3.92	2.59	2.04	1.88
SOA	1.76	1.36	1.28	1.12
SSM	1.76	1.36	1.28	1.12
SSP	1.76	1.36	1.28	1.12
STA	2.32	1.96	1.76	1.52
STX	2.32	1.96	1.76	1.52
SUB	2.44	1.96	1.88	1.56

SVC	4.24	3.24	3.20	2.80
TCA	2.12	1.64	1.48	1.32
VIRY	–	128	128	128
XCA	2.48	1.68	1.68	1.52
XCB	2.48	1.68	1.68	1.52
XEC	–	--	3.24+	2.92+

TIMING NOTES:

1. Values for N =
   number of steps in shifts.
   number of steps in normalize.
   number of steps in normalize routine of floating point operations.
2. A = number of adjust steps in floating point.
3. I = level of indirection.

ASCII Character Codes

Octal Representation	Internal ASCII Char.	Communications Code	Octal Representation	Internal ASCII Char.	Communications Code
200	NUL	NUL	300	@	@
201		SOH	301	A	A
202		STX	302	B	B
203		ETX	303	C	C
204		EOT	304	D	D
205		ENG	305	E	E
206		ACK	306	F	F
207	BEL	BEL	307	G	G
210	BS	BS	310	H	H
211	HT	HT	311	I	I
212	NL	LF	312	J	J
213	VT	VT	313	K	K
214	FF	FF	314	L	L
215	CR	CR	315	M	M
216	RRS	SO	316	N	N
217	BRS	SI	317	O	O
220	RCP	DLE	320	P	P
221	RHT	DC1	321	Q	Q
222	HLF	DC2	322	R	R
223	RVT	DC3	323	S	S
224	HLR	DC4	324	T	T
225		NAK	325	U	U
226		SYN	326	V	V
227		ETB	327	W	W
230		CAN	330	X	X
231		EM	331	Y	Y
232		SUB	332	Z	Z
233		ESC	333	[	[
234		FS	334	\	\
235		GS	335	]	]
236		RS	336	↑	↑
237		US	337		
240	SP	SP	340	'	'

241	!	!	341	a	a
242	"	"	342	b	b
243	#	#	343	c	c
244	$	$	344	d	d
245	%	%	345	e	e
246	&	&	346	f	f
247	'	'	347	g	g
250	(	(	350	h	h
251	)	)	351	i	i
252	*	*	352	j	j
253	+	+	353	k	k
254	,	,	354	l	l
255	-	-	355	m	m
256	.	.	356	n	n
257	/	/	357	o	o
260	Ø	Ø	360	p	p
261	1	1	361	q	q
262	2	2	362	r	r
263	3	3	363	s	s
264	4	4	364	t	t
265	5	5	365	u	u
266	6	6	366	v	v
267	7	7	367	w	w
270	8	8	370	x	x
271	9	9	371	y	y
272	:	:	372	z	z
273	;	;	373	{	{
274	<	<	374	|	|
275	=	=	375	}	}
276	>	>	376	~	~
277	?	?	377		DEL

Input/Output Device Addresses

Address	Device
'00	Polling
'01	Paper Tape Reader
'02	Paper Tape Punch
'03	Line Printer
'04	Teletype
'05	Card Reader
'06	Card Punch
'12	Diskette
'14	Magnetic Tape 1
'15	Magnetic Tape 2
'16	Magnetic Tape 3
'17	Magnetic Tape 4
'20	Series 16 Set Mask Instruction, Control Panel, Real Time Clock
'21	Disk (4002 Controller)
'22	Fixed Head Disk
'23	30M Word Disk
'24	Writable Control Store

Address	Device
'25	Moving Head Disk
'26	Storage Tube Display
'30	I/O Channel 1
'31	I/O Channel 2
'32	I/O Channel 3
'40	Analog Input System
'41, '42	Digital Input System
'43, '44	Digital Output System
'45	Analog Output System
'46	Computer Products Interface
'54	AMLC
'55	MACI
'56	SMLC
'57	SMLC
'60-'67	General Purpose Interface Board
'70	General Purpose Interface Board Function Test
'77	I/O Bus Tester

Reserved Memory Locations

Address	Assignment
'000000	X Register - Index Register
01	A Register - Arithmetic, Shift, I/O
02	B Register - Ext. Arithmetic, Shift
03	Stack Pointer
04	FLPH - Floating Point High (Optional)
05	FLPL - Floating Point Low (Optional)
06	VSC - Visible Shift Counter
07	P Register - Program Counter
10	PMAR - Page Map Address Register (Optional)
11	Microcode Scratch Location
12	EAS - Effective Address Save (ILL, UII, Interrupts, etc.)
13	Microcode Scratch Location
14	Y Register Save for Control Panel & DMA
15	M Register Save for Control Panel & DMA
16	Microcode Scratch Location
17	Microcode Scratch Location
20 } 37	DMA Range/Start Address Pairs
40 } 57	Reserved for DMC Channel Pairs
60	PFI - Power Failure Interrupt and Watchdog Timer
61	RTCI - Real Time Clock Increment (Optional)
62	REVI - Restricted Execution Violation (Optional)
63	INT - Standard Interrupt (Compatible Mode)
64	Page Fault - Addressed Page Not in Mem. (Optional)
65	SVC - Supervisor Call Trap
66	UII - Unimplemented Instruction Interrupt
67	PE - Memory Data Parity Error

Address	Assignment
70	Machine Check - Processor Detected Error
71	Missing Module - No memory at Accessed Location
72	ILL - Illegal Instruction Interrupt
73	PWV - Page Write Violation (Optional)
74	FLEX - Floating Point Exception (Optional)
75	PSU - Procedure Stack Underflow (PRIME 300 only)
76 ⊦ 100	Debugging Scratch Area
101 ⊦ 177	Interrupt Vectors
200 ⊦ 777	General Cross Sector Links

PRIME

145 PENNSYLVANIA AVENUE, FRAMINGHAM, MA 01701

Printed in U.S.A.