PR1ME

Customer Service

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Rev: 0
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BULLETIN

Subject: INTELLIGENT DISK CONTROLLER (IDC1) INFORMATION

- The Intelligent Disk Controller, PRIME part number TLA10019-001, will be referred to in future documentation as the IDC1.

This bulletin clarifies any discrepancies in CSB #528 dealing with the IDC1 disk controller and its verification. CSB #528 may be updated per CSB #561, 562 and 563 or discarded upon receipt of these three CSBs.

o The following are also included in this bulletin:

- Installation
- Reference Document Numbers
- IDC1 Jumper Headers and Indicators
- IDC1 Verification

o Dependencies include:

- Minimum Primos Revision 20.0.2
- Minimum DTS Revision 7.0

- NOTE: Please use Major Unit Code DC1 when calling Central Dispatch with any problems regarding the IDC1 controller, and also when closing service calls.

Originator Jay Welch

Approval

REFERENCE DOCUMENTS

There are a number of useful documents for installation and operation of the new IDC1 controller. The 4735 Site Preparation Addendum, CSB 527, provides pre-install requirement specifications for the 496MB drive and the 7564S peripheral cabinet..

The disk drive is mounted in the new 7564S cabinet. The Service Procedures Manual, SPM460 and CSB #563, provide all necessary information relating to the cabinet.

This document contains the information necessary to install the IDC1 controller, a brief description of necessary jumpers and power-up/verification procedures through the use of diagnostic LEDs mounted on the board.

A CS Technical Manual - TTM470 containing disk drive vendor documentation provides detailed information of the new drive. Refer to the vendor documentation in TTM470 for detailed information about the disk drive.

A CS Technical Manual - TTM501 module supports the IDC1 controller and provides a basic description of the controller board.

The installation procedures for the disk drive will be included in the 496MB Service Procedures Manual - SPM470.

- The IDC1 contains static sensitive logic, requiring ElectroStatic Discharge (ESD) protection. Be sure to follow standard ESD procedures in CSB #443 before handling the controller or its components.

INTRODUCTION TO THE IDC1

Prime P/N TLA10019-001

Marketing Model #6580

The Model 6580 Intelligent Disk Controller (IDC1) is the new controller board replacing the 4005 controller (BSMC). The IDC1 as of Rev M is capable of a 20MHz transfer rate (vs 9.67 MHz w/4005) and will also run any device that previously ran on the 4005 controller.

Unlike the 4005 edge connectors, the IDC1 will have male connectors similar to the connectors on the disk drive I/O ports.

Older cables are physically impossible to attach to the IDC1. ONLY the new cables are to be used when installing the 496 MB disk drive due to the impedance matching necessary with the higher transfer rates.

For more information on cabling, please referrence CSB #561 and 563 dealing with the 4735 disk drive and 7564S peripheral cabinet respectively.

Up to four controllers may be installed in one system and may be mixed with the 4005 BSMC controller.

The IDC1 should be installed in the I/O chassis above all tape controllers.

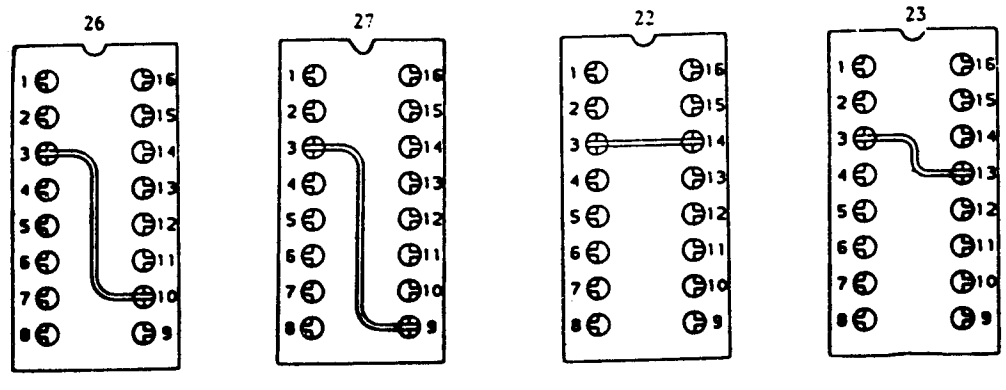
Unlike previous controllers, there will be no PROM to limit the number of drives to be run on the controller. Every IDC1 will be capable of running four disk drives.

The IDC1 will also have a jumper header at location 59L. This header presently has two functions.

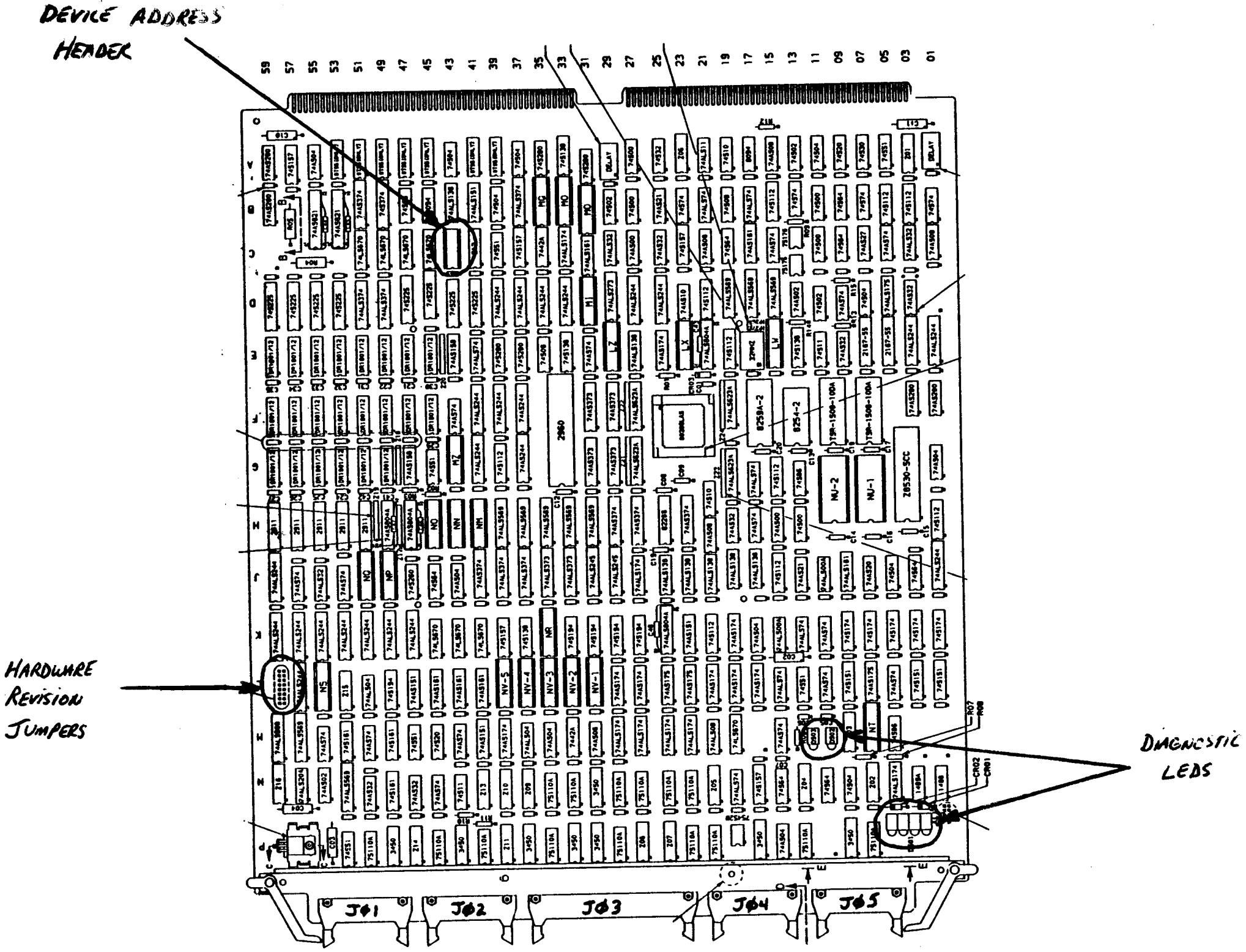
1. Pins 1 and 9 WERE jumpered to implement 4005 mode operation. This jumper initially was used to "lock" the board in 4005 mode. At IDC1 revision M (FCO 474) this jumper MUST be removed.

2. Pins 2 to 8 and 10 to 16 will be used to report the board revision to the on-board microprocessor.

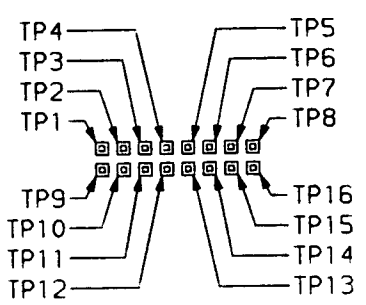
Please see the following illustrations for device address header information, hardware revision header information and general IDC1 board layout.



IDC1 Device Address Header Information (location 43C)



General IDC1 Board Layout



Hardware Revision Jumper Header Information (location 59L)

IDC1 OPERATIONAL VERIFICATION

Upon power-on, receipt of an OCP '17 instruction, or a System Clear pulse, the IDC1 controller will execute its self diagnostic routines. These routines are broken up into test specific hardware modules on the board. A complete verify is only done on power-on or when a memory error condition exists. If these conditions do not exist, all memory tests will be skipped so that memory may be uploaded to the HOST system for analysis.

Six LEDs are provided for error indication. A RED (STOP) and GREEN (GO) LED are used to encode the state of the controller, while four AMBER LEDs are used to encode an error number.

If operating correctly, the IDC1 will increment through the LEDs and finalize self testing with a solid GREEN (GO) LED.

The RED and GREEN LEDs are used to show the state of the board. When both LEDs are lit, the board is in the process of running its verify. If only the RED LED is lit, the verify has failed and the board is in an error loop. Finally, if only the GREEN LED is on, the board has successfully completed its verify and is now in operating mode.

If an error occurs during verify, an error handler will be entered, the RED LED will be lit, the GREEN LED will be extinguished and the four AMBER LEDs will be set to the failing test group number (HEX). The test group number corresponds to a group of specific tests. From this number, one may determine approximately where in the verify the board failed. When facing the LEDs, the MSB LED is the left-most AMBER LED.

The following charts identify start up and operating faults on the IDC1 board.

Error Condition	Green LED	Red LED	Yellow LEDs 4	3	2	1	Hex Value
Microprocessor Divide Error	ON	OFF	OFF	OFF	OFF	ON	1
Microprocessor Single Step Int	ON	OFF	OFF	OFF	ON	OFF	2
NMI	ON	OFF	OFF	OFF	ON	ON	3
Microprocessor Brk. Point Int	ON	OFF	OFF	ON	OFF	OFF	4
Microprocessor Into Overflow	ON	OFF	OFF	ON	OFF	ON	5
Microprocessor Bound Exceeded	ON	OFF	OFF	ON	ON	OFF	6
Microprocessor Invalid Opcode	ON	OFF	OFF	ON	ON	ON	7
Microprocessor Proc. Extension	ON	OFF	ON	OFF	OFF	OFF	8
Microprocessor Proc. Extension	ON	OFF	ON	OFF	OFF	ON	9
Microprocessor Null ISR	ON	OFF	ON	OFF	ON	OFF	A
ECC Error Overflow	ON	OFF	ON	OFF	ON	ON	B

Self Verify Error Display

Test Number	Green LED	Red LED	Yellow LEDs 4	3	2	1	Hex Valve
Invalid Hardware Revision	OFF	ON	OFF	OFF	OFF	OFF	0
TEST 01	OFF	ON	OFF	OFF	OFF	ON	1
TEST 02	OFF	ON	OFF	OFF	ON	OFF	2
TEST 03	OFF	ON	OFF	OFF	ON	ON	3
TEST 04	OFF	ON	OFF	ON	OFF	OFF	4
TEST 05	OFF	ON	OFF	ON	OFF	ON	5
TEST 06	OFF	ON	OFF	ON	ON	OFF	6
TEST 07	OFF	ON	OFF	ON	ON	ON	7
TEST 08	OFF	ON	OFF	ON	ON	ON	7
TEST 09	OFF	ON	ON	OFF	OFF	OFF	8
TEST 10	OFF	ON	ON	OFF	OFF	OFF	8
TEST 11	OFF	ON	ON	OFF	OFF	OFF	8
TEST 12	OFF	ON	ON	OFF	OFF	OFF	8
TEST 13	OFF	ON	ON	OFF	OFF	OFF	8
TEST 14	OFF	ON	ON	OFF	OFF	OFF	8
TEST 15	OFF	ON	ON	OFF	OFF	ON	9
TEST 16	OFF	ON	ON	OFF	ON	OFF	A
TEST 17	OFF	ON	ON	OFF	ON	OFF	A
TEST 18	OFF	ON	ON	OFF	ON	ON	B
TEST 19	OFF	ON	ON	ON	OFF	OFF	C
TEST 20	OFF	ON	ON	ON	OFF	ON	D

Operational Error Display

DIAGNOSTICS

Pléase refer to the DTS User's Guide (DTS Rev 9 User's Guide PE-T-1122) for information pertaining to diagnostic operation.