PRIME CUSTOMER SERVICE

50 SERIES COMPUTER SYSTEMS

SERVICE MANUAL 070

MARCH

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PRIME
Computer
PRIME PARK
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FOREWORD

Prime Computer Corporation is committed to a policy of providing the best possible service for our products and our customers. This manual has been prepared for use by Customer Service Representatives. It is intended to be used as a training aid and as a guide for installation, preventive and corrective maintenance.

The manual is organized into chapters based on tasks the Customer Service Representative performs at the customer's site. Tasks that are too difficult and time consuming to be performed on the customer's site are beyond the scope of the handbook.

Through experience and necessity Customer Service Representatives continually find methods to simplify Installation and Maintenance procedures. With the understanding that the best manuals are an organized collection of these field proven shortcuts, you are encouraged to forward all such procedures to Customer Service, Documentation.

Use of WARNING, CAUTION and NOTE is as follows:

WARNING - To warn the operator of a potentially hazardous condition that may cause physical injury.

CAUTION - To caution the operator of a condition that could cause damage to the equipment.

NOTE - To provide additional information.

INDEX OF SERVICE MANUALS

MANUAL	DEVICE(S) COVERED	PART NUMBER
MAN010	GE TERMINET 30	TEAMAN010
MAN020	KENNEDY MAGNETIC TAPE	TEAMAN020
MAN030	P.E. FOX AND OWL	TEAMAN030
MAN040	CDC 40 & 80 MBYTE SMD	TEAMAN040
MAN050	DIABLO 44B MHD	TEAMAN050
MAN060	DATA PRINTER 300/600 LPM	TEAMAN060
MAN070	50 SERIES COMPUTER SYSTEMS	TEAMAN070-C
MAN080	SYSTEMS SOFTWARE	TEAMAN080
MAN090	CDC 32, 64 & 96 MBYTE CMD	TEAMAN090
MAN100	INTRODUCTION TO COMPUTER MAINTENANCE	TEAMAN100
MAN110	PRINTRONIX MODEL 300 PRINTER	TEAMAN110
MAN120	300 MEGABYTE STORAGE MODULE DRIVE	TEAMAN120-A
MAN130	TELEX 6250 BPI TAPE	TEAMAN130
MAN140	NEC SPINWRITER	TEAMAN140
MAN150	PW90 SERIES WORKSTATIONS	TEAMAN150
MAN160	DATAPRODUCTS PRINTER 300/600 LPM	TEAMAN160
MAN170	CDC 160 MBYTE MMD	TEAMAN170
MAN180	GE TERMINET 2030	TEAMAN180
MAN200	2250 COMPUTER SYSTEM	TEAMAN200
MAN210	CAD GRAPHICS WORKSTATION (PW200)	TEAMAN210
MAN220	CDC 675 MBYTE FMD	TEAMAN220
MAN230	9000-ECL-CPU SYSTEMS	TEAMAN230-A1
MAN240	PRIME SYSTEM TERMINAL (PST100)	TEAMAN240
MAN250	INTELLIGENT COMMUNICATIONS SUBSYSTEM MODEL II (ICS2)	TEAMAN250
MAN270	2550 COMPUTER SYSTEM	TEAMAN270
MAN280	MAGNETIC STREAMING TAPE SUBSYSTEM	TEAMAN280
MAN290	PRIME PRODUCER WORKSTATION (PW100)	TEAMAN290
MAN320	300 MEGABYTE FIXED MODULE DISK	TEAMAN320
MAN340	LETTER QUALITY PRINTER (3185)	TEAMAN340
MAN350	PT200 TERMINAL	TEAMAN350
MAN360	9650 COMPUTER SYSTEM	TEAMAN360
MAN900	INTRODUCTION TO FIELD ENGINEERING	TEAMAN900

RECORD OF CHANGES

LEVEL: REV	UPDATE	ISSUE DATE	NOTES/PAGES AFFECTED
B	0	08/82	Second Revision
C	0	02/85	Third Revision

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CHAPTER 1
GENERAL DESCRIPTION

1.1 INTRODUCTION

Prime's™ current 50 Series™ products are the 150-II™ , 250-II™ , 550-II™ , as shown in Figure 1-1 and Figure 1-2, 750™ , and 850™ , shown in Figure 1-3 and Figure 1-4. Obsolete members of the 50 Series include: 150, 250, 450 (all 2-board processors), 550, and 650 (3-board processors) systems.

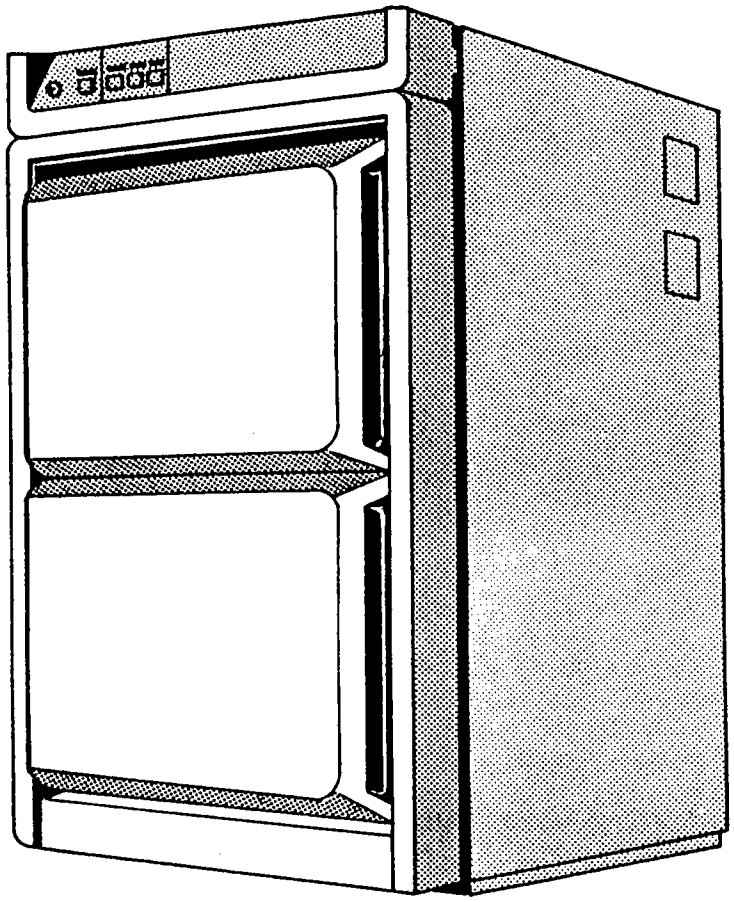


FIGURE 1-1: 150-II/250-II/550-II CPU SYSTEM (NON-FCC)

The main technological improvement of the 50 Series current product line is the Virtual Control Panel (VCP). The VCP is a microprocessor based controller which replaces the System Option Controller (serial interface for the system console) and the Control Panel (system sense switches and lights). The VCP allows the operator to enter English-like commands at the system console, instead of monitoring control panel switches and lights.

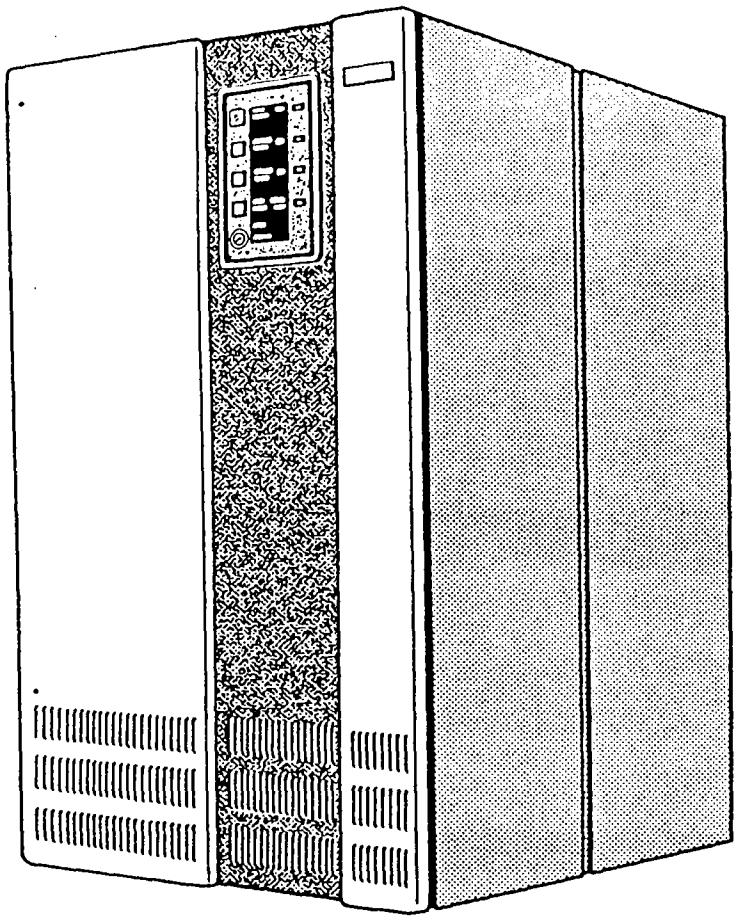


FIGURE 1-2: 150-II/250-II/550-II CPU SYSTEM (FCC)

Besides the VCP, all current models also have 32 bit architecture and a faster arithmetic unit, but are based on the same fundamental design as the original Prime 200. Each processor supports many peripherals, though the maximum configuration varies with each CPU. Prime's 850 processor supports up to 8Mb memory, 8 disk drives, 8 tape drives, 4 parallel printers, 4 unit record (card) devices, 2 synchronous communications boards (MDLC), 1 ring net controller (PNC), and 128 terminals.

All of the 50 Series processors can support Prime's communications equipment (PRIMENET™ Node Controller and PRIMENET software), used to network any Prime systems. When used with other Prime hardware (MDLC) and software (DPTX and RJE), Prime systems can interface with, or simulate, batch-oriented mainframes, including IBM™ , UNIVAC™ , and Honeywell™ . Prime's communications tools allow a user to configure a network that maximizes both Prime's interactive, multi-user features and the batch features of a large mainframe, such as IBM.

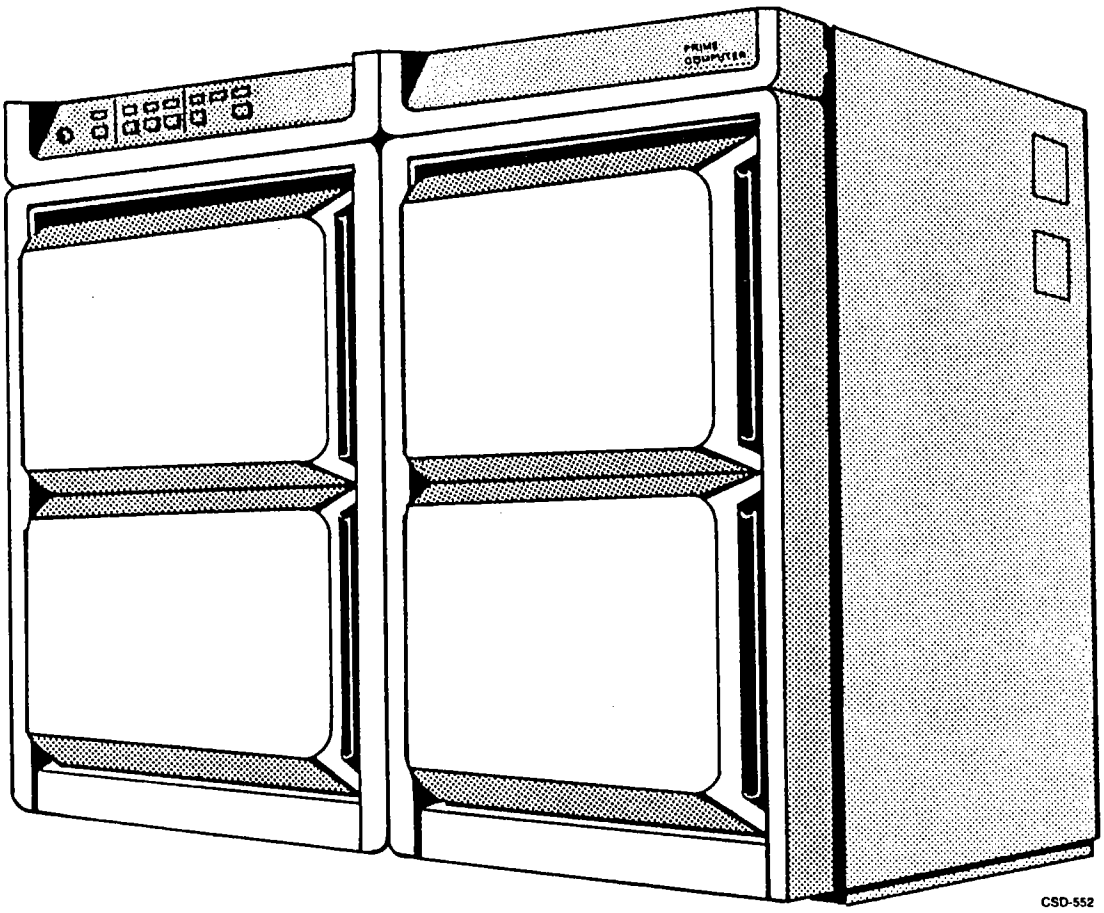


FIGURE 1-3: 750/850 CPU SYSTEM (NON-FCC)

The 250-II 2-board processor performs about 70 percent faster than the 250 CPU. The 250-II is designed for use as a local station (node) in a large computer network, or as a complete system for a small, multi-user environment. The 150-II has an identical processor, but is packaged and sold to a different type of user. Both systems have microcode-implemented floating point and business instructions.

The 550-II (CPU) offers more speed and memory capacity than the 250-II. The system is designed with a 3-board processor, hardware-implemented floating point and business instructions, and larger cache and main memory.

The 5-board 750 processor has two significantly improved features over the 550-II. The Instruction Preprocessor Unit (IPU) is located on the 750's J board. The IPU fetches (from cache) and decodes up to four instruction words ahead of the currently executing instruction. Burst mode I/O uses the DMA channels to transfer 64 bits at a time, instead of 16 bits at a time. This creates an I/O bandwidth of 8Mb per second, compared to the 2.5Mb bandwidth used in nonburst mode I/O. I/O time from disk and tape units is decreased by about two-thirds.

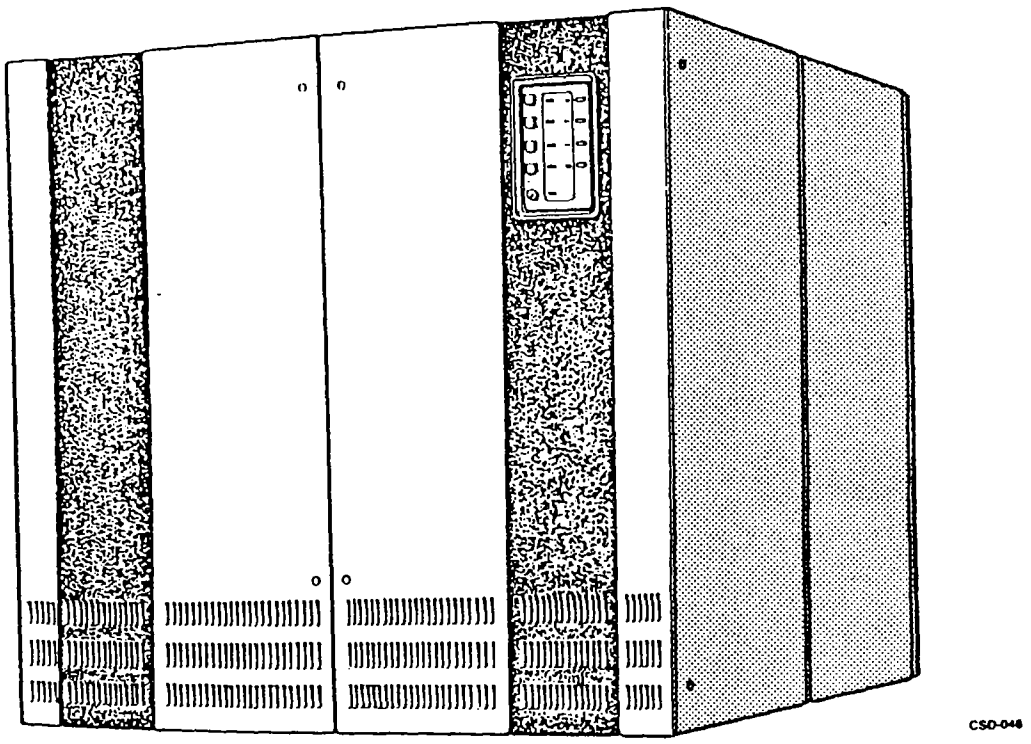


FIGURE 1-4: 750/850 CPU SYSTEM (FCC)

The more powerful 850 CPU, a multi-stream 11-board processor, uses two modified 750 processors under the control of a Stream Synchronization Unit (SSU), speed is increased 60 to 80 percent over the 750. Each processor has its own cache and IPU. The SSU manages physical memory access so that cache is always current; the master CPU (Instruction Stream Unit 1) controls I/O. The 850 is the first system to use ultra-high density MOS memory chips with 64K x 1 bit dynamic RAMs. Each memory board contains either 1/2Mb or 1Mb storage. The 850 supports a maximum of 128 users.

1.2 SPECIFICATIONS

General and physical specifications are presented in Tables 1-1 through 1-4.

TABLE 1-1: GENERAL SPECIFICATIONS: 150, 250-II, 550-II SYSTEMS

CENTRAL SYSTEM	150/250-II	550-II
Processor (number of boards)	2	3
Internal Data Paths	32 bit	32 bit
Instruction Pre-processor Unit	No	No
Multi-stream Achitecture	No	No
Error Correcting Memory	Yes	Yes
Interleaved Memory	Yes	Yes
Minimum Main Memory	.25Mb(150-II) .5Mb(250-II)	.5Mb

TABLE 1-1: GENERAL SPECIFICATIONS: 150, 250-II, 550-II SYSTEMS (Cont.)

CENTRAL SYSTEM	150/250-II	550-II
Maximum Main Memory	1Mb	4Mb
Bipolar Cache Memory	2Kb	8Kb
Avg. Cache Hit Rate (percent)	85	90
Virtual Control Panel	Yes	Yes
Simultaneous Active Processes	128	128
Max. Direct Connect Terminals	32	64
Virtual Address Space Per User	512Mb	512Mb
Maximum User Program Space	32Mb	32Mb
Burst Mode I/O	No	No
DMA,DMC,DMT,DMQ	Yes	Yes
DMA Channels	32	32
I/O Bandwidth (Mb/Sec)	2.5	2.5
Floating Point Instructions	Yes	Yes
32-Bit Integer Arithmetic	Yes	Yes
Instruction Set	500+	500+
Highest Address Mode (16S,32S,32R,64R,64V,32I)	32I	32I
Process Exchange Instructions for Floating Point Arithmetic, Decimal Arithmetic and Character String Operations	Yes microcode	Yes microcode & XIS board
PERIPHERALS		
Disk	Any	Any
Tape	Any	Any
Printers	Any	Any
Terminals	Any	Any
COMMUNICATIONS		
Asynchronous Lines	1-32	1-64
Synchronous Lines (MDLC)	0-2	0-4
PRIMENET Node Controller (PNC)	Yes	Yes

TABLE 1-2: GENERAL SPECIFICATIONS: 750 & 850 SYSTEMS

CENTRAL SYSTEM	750	850
Processor (number of boards)	5	11
Internal Data Paths	32 bit	32 bit
Instruction Pre-processor Unit	Yes	Yes
Multi-stream Achitecture	No	Yes
Error Correcting Memory	Yes	Yes
Interleaved Memory	Yes	Yes
Minimum Main Memory	1Mb	2Mb
Maximum Main Memory	8Mb	8Mb
Bipolar Cache Memory	16kb	32Kb
Avg. Cache Hit Rate (percent)	95	95
Virtual Control Panel	Yes	Yes

TABLE 1-2: GENERAL SPECIFICATIONS: 750 & 850 SYSTEMS (Cont.)

CENTRAL SYSTEM	750	850
Simultaneous Active Processes	128	128
Max. Direct Connect Terminals	96	128
Virtual Address Space Per User	512Mb	512Mb
Maximum User Program Space	32Mb	32Mb
Burst Mode I/O	Yes	Yes
DMA,DMC,DMT,DMQ	Yes	Yes
DMA Channels	32	32
I/O Bandwidth (Mb/Sec)	8	8
Floating Point Instructions	Yes	Yes
32-Bit Integer Arithmetic	Yes	Yes
Instruction Set	500+	500+
Highest Address Mode (16S,32S,32R,64R,64V,32I)	32I	32I
Process Exchange	Yes	Yes
Instructions for Floating Point Arithmetic, Decimal Arithmetic and Character String Operations	microcode & XIS board	microcode & XIS board
PERIPHERALS		
Disk	Any	Any
Tape	Any	Any
Printers	Any	Any
Terminals	Any	Any
COMMUNICATIONS		
Asynchronous Lines	1-96	1-128
Synchronous Lines (MDLC)	0-4	0-4
PRIMENET Node Controller (PNC)	Yes	Yes

TABLE 1-3: CABINET GENERAL DIMENSIONS

	HEIGHT IN.(CM)	WIDTH IN.(CM)	DEPTH IN.(CM)
NON-FCC	62 (160)	25 (64)	38 (83)
FCC	53 (134.6)	52.5 (133.4)	35.3 (89.5)

TABLE 1-4: 50 SERIES WEIGHT

TYPE	WEIGHT LB (KG)
150, 150-II, 250, 250-II, 450	400 (180)
450-II, 550, 550-II, 650	425 (190)
750, 850	450*(200)

*Weight per cabinet.

1.3 RELATED DOCUMENTATION

Related 50 Series CPU system documentation is listed in Table 1-5.

TABLE 1-5: 50 SERIES CENTRAL SYSTEMS DOCUMENTATION

DOCUMENTATION NAME	PART NUMBER
Planning and Installation Guide (Rev.19.0)	DOC6426-901
Prime User's Guide	DOC4130-190
System Administrator's Guide (Rev. 19.0)	DOC5037-190
(Rev 19.1)	UPD5037-191
(Rev 19.2)	UPD5037-192
Site Preparation Guide	IDR5029
System Architecture Guide (19.2)	DOC3060-192
System Operator's Guide Vol. I, (19.2)	DOC7323-192
System Operator's Guide Vol. II, (19.2)	DOC7324-192

1.4 FCO LOG

Prime Field Change Orders (FCOs) are generated whenever a condition exists which requires that a machine(s) in the field be changed. It is important that FCOs be installed in the units in a timely manner and the FCO log with the equipment be kept current. Without an accurate record of the changes which have been installed in the unit, it would be impossible to relate the machine configuration to the manual.

1.5 EQUIPMENT IDENTIFICATION

To locate the equipment identification (ID) and model number plates, go to the rear of the I/O cabinet and look at the lower right corner of the door. The system ID plate provides the number by which each type of system is identified. The model number plate provides the following information:

- Model number
- Serial number
- Voltage and amperage specifications

1.6 PRIME MODEL NUMBERS

The Prime model numbers are generated according to the following schemes:

- Marketing system numbering scheme
- Information system numbering scheme

These numbers, along with Prime type numbers, are explained and listed in this subsection.

1.6.1 MARKETING SYSTEM NUMBERING SCHEME

Prime Marketing uses model numbers to identify an entire system configuration. For example, 550II-HMB refers to a 550-II CPU with 1/2Mb memory and a hard copy system console. Prime Manufacturing and Customer Service Logistics use part numbers instead of model numbers. One Marketing model number can be broken down into many Manufacturing part numbers. For example, 550II-HMB identifies the same equipment as the part numbers for each of the following:

- CPU - 2253-902, 2278-901, 2279-901
- Tophats - ESA2495-903
- Power supply - 1045-901
- Cabinet - 7550-901
- VCP - 2265-901
- Memory - 12128-E6
- Terminal - TTY3754-001

The customer's sales order identifies equipment using Marketing model numbers. The packing slip, shipped with the equipment from the Prime factory, uses Manufacturing part numbers. Therfore, a working knowledge of the Marketing model number scheme is necessary to be able to check the sales order against the packing slip.

The Marketing model numbers assigned to the 50 Series systems consist of six alphanumeric characters. Each character and character position has a special significance. To provide an example, the characters A, B, C, D, E, and F are used to indicate the meaning of each character in the 50 Series model numbers as follows:

ABC-DEF

Position A specifies the central processor type:

1=150-II 2=250-II
5=550-II 7=750 8=850

Position B specifies the product line, currently a 5 for all 50 Series systems.

Position C denotes the Cartridge Module Disk (CMD) Drive size. This only applies to the 150-II and 250-II systems. (A II may be appended to C indicating a MODII product.)

N = None (CMD not provided with system)
0 = 32Mb CMD
4 = 64Mb CMD
6 = 96Mb CMD

Positions D and E indicate the memory size:

QM = 256Kb
HM = 512Kb
34 = 768Kb
1M = 1024Kb
2M = 2048Kb

Position F specifies console type:

B = Terminet #30
C = CRT Terminal
N = None

NOTE

The suffix -A will be added to the model number to indicate a 220 VAC, 50Hz version.

A Prime Marketing model number for a 150-II processor with a 64Mb CMD, 512Kb MOS memory, and no system console, is configured as:

154II-HMN

More examples are illustrated in Table 1-6.

1.6.2 INFORMATION SYSTEM NUMBERING SCHEME

The Marketing model numbers for the INFORMATION family of systems are set up differently. The model number consists of eight alphanumeric characters. Each character and character position has a special significance. To provide an example, the characters A, B, C, D, E, F, G, and H are used to indicate the meaning of each character in the INFORMATION Type Numbers as follows:

ABCD-EFG-H

Position A specifies the product line, currently an I for all INFORMATION systems.

Positions B and C specify the central processor type:

25=250-II 45=450-II
75=750 85=850

Position D denotes the type and size of the disk subsystem.

E = 64Mb CMD
K = 96Mb CMD
J = 80Mb SMD
P = 160Mb MMD
R = 300Mb SMD

Position E indicates the memory size:

Hxx = 512Kb (2 256K boards)
Wxx = 512Kb (1 512K board)
1xx = 1024Kb (2 512K boards)
5xx = 1536Kb (2 512K & 2 256K boards)
2xx = 2048Kb (2 1024K boards)
3xx = 3072Kb (2 1024K & 2 512K boards)
4xx = 4096Kb (4 1024K boards)

Position F specifies tape drive type:

4 = Tape #4512 (800 BPI, 45 IPS)
7 = Tape #4522 (800/1600 BPI, 75 IPS)
N = None

Position G specifies system console type, always N for none.

Position H specifies the number of ports; this only applies to the I250-II.

NOTE

The suffix -A will be added to the model number to indicate a 220 VAC, 50Hz version.

A Prime INFORMATION model number for a 250-II processor with a 64Mb CMD, 512Kb MOS memory, no system console, and 14 open ports, is configured as:

I25E-WNN-14

More examples are illustrated in Table 1-7.

TABLE 1-6: 50 SERIES CONFIGURATIONS

MODEL #	CPU TYPE	MEMORY	CMD TYPE	CONSOLE	CHASSIS	POWER SUPPLIES
150II-QMN	2247-901 2248-901	E4(256K)	32Mb	NONE	17-SLOT	1
154II-QMN	2247-901 2248-901	E4(256K)	64Mb	NONE	17-SLOT	1

TABLE 1-6: 50 SERIES CONFIGURATIONS (Cont.)

MODEL #	CPU TYPE	MEMORY	CMD TYPE	CONSOLE	CHASSIS	POWER SUPPLIES
156II-QMN	2247-901 2248-901	E4(256K)	96Mb	NONE	17-SLOT	1
250II-HMC	2247-901 2248-901	E4(512K)	32Mb	CRT	17-SLOT	1
254II-HMC	2247-901 2248-901	E4(512K)	64Mb	CRT	17-SLOT	1
256II-HMC	2247-901 2248-901	E4(512K)	96Mb	CRT	17-SLOT	1
550II-HMC	2253-902 2278-901 2279-901	E6(512K)		CRT	34-SLOT	2
550II-HMB	2253-902 2278-901 2279-901	E6(512K)		TER. 30	34-SLOT	2
550II-1MB	2253-902 2278-901 2279-901	E6(1Mb)		TER. 30	34-SLOT	2
750-1MC	2259-902 2262-902 2263-902 2264-901 2268-901	E6,E7, E8(1Mb)		CRT	38-SLOT	4
750-1MB	2259-902 2262-902 2263-902 2264-901 2268-901	E6,E7, E8(1Mb)		TER. 30	38-SLOT	4
750-8MB	2259-902 2262-902 2263-902 2264-901 2268-901	E8(8Mb)		TER. 30	38-SLOT	4
850-2MC	2273-901 2274-901 2275-901 2285-901 2286-901 2029-901	E7, E8(2Mb)		CRT	35-SLOT + 19-SLOT	5
850-2MB	2273-901 2274-901 2275-901 2285-901 2286-901 2029-901	E7, E8(2Mb)		TER. 30	35-SLOT + 19-SLOT	5
850-8MC	2273-901 2274-901 2275-901 2285-901 2286-901 2029-901	E8(8Mb)		CRT	35-SLOT + 19-SLOT	5

TABLE 1-7: INFORMATION SYSTEM (DEALER) CONFIGURATIONS

MODEL #	CPU TYPE	MEMORY	DISK TYPE	TAPE	POWER SUPPLIES	PORTS
I25E-HNN-6	2247-901 2248-901	E4(512K)	64Mb CMD	--	1	6
I25J-14N-14	2247-901 2248-901	E4(1Mb)	80Mb SMD	4512	1	14
I45E-HNN	2292-901 2210-902	E6(512K)	64Mb CMD	--	2	
I45J-14N	2292-901 2210-902	E6(1Mb)	80Mb SMD	4512	2	
I45P-17N	2292-901 2210-902	E6(1Mb)	160Mb FMD	4512	2	
I45R-57N	2292-901 2210-902	E6(1.5Mb)	300Mb SMD	4522	2	
I75P-1NN	2259-902 2262-902 2263-902 2264-901 2268-901	E6,7,8(1Mb)	160Mb FMD	--	4	
I75P-1NN	2259-902 2262-902 2263-902 2264-901 2268-901	E6,7,8(3Mb)	300Mb SMD	--	4	
I75R-47N	2259-902 2262-902 2263-902 2264-901 2268-901	E6,7,8(4Mb)	300Mb SMD	4522	3	
I85R-2NN	2273-901 2274-901 2275-901 2285-901 2286-901 2029-901	E8(2Mb)	300Mb SMD	--	5	
I85R-27N	2273-901 2274-901 2275-901 2285-901 2286-901 2029-901	E8(2Mb)	300Mb SMD	4522	5	
I85R-47N	2273-901 2274-901 2275-901 2285-901 2286-901 2029-901	E8(4Mb)	300Mb SMD	4522	5	

1.6.3 PRIME TYPE NUMBERS

Each board in a Prime system has a unique part number. Some of the more common parts are listed in Table 1-8. For a more detailed listing, refer to Chapter 7 of this book.

TABLE 1-8: COMMON PRIME TYPE NUMBERS

DESCRIPTION	PART NUMBER
P400 CPU	2244-902
P400 A Board	2241-902
P400 B Board	2242-902
P350 CPU	2240-901
P350 A Board	2243-901
P350 B Board	2245-901
P150-II, 250-II CPU	2208-901
P250-II, 150-II A Board	2247-901
P250-II, 150-II B Board	2248-901
P500 CPU	2250-901
P500 A Board	2251-901
P500 B Board	2252-901
P500 XIS Board	2253-901
P550-II CPU	2281-901
P550-II XIS Board	2253-902
P550-II A Board	2278-901
P550-II B Board	2279-901
P750 CPU	2260-902
P750 A Board	2259-902
P750 C Board	2262-902
P750 CS Board	2263-902
P750 XIS Board	2264-901
P750 J Board	2268-901
P850 CPU	2276-901
P850 J Board (E.V.)	2273-901
P850 C Board (E.V.)	2274-901
P850 CS Board (E.V.)	2275-901
P850 A Board (E.V.)	2285-901
P850 XIS Board (E.V.)	2286-901
P850 SSU Board (E.V.)	2029-901
I450-II CPU	
I450-II A Board	2292-901
I450-II B Board	2210-902
P750/850 top-hat w/o FEP*	ESA2495-905
P750/850 top-hat w/FEP*	ESA2495-906
P550-II top-hat w/FEP*	ESA2495-903
P550-II top-hat w/o FEP*	ESA2495-909
P250-II top-hat w/FEP*	ESA2495-902
P250-II top-hat w/o FEP*	ESA2495-908

TABLE 1-8: COMMON PRIME TYPE NUMBERS (Cont.)

DESCRIPTION	PART NUMBER
Memory	
256Kb ECC board (E.V.)	12128-E4
256Kb ECC WWM board (E.V.)	12128-E6
512Kb ECC WWM board (E.V.)	12256-E7
1024Kb ECC WWM board (E.V.)	12512-E8
64K x 1 bit RAM (1Mb board)	ICD4871
Memory Extender Chassis	1025-903
750 Mem. Ext. Main Board	2022-902
Mem. Ext. Main Board	2082-901
Mem. Ext. Extendor Board	2083-901
PRIMENET Node Controller	2257-902
Virtual Control Panel (VCP)	2265-902
Control Panel, 7520 Cab.	1032-901

*Top-Hat is also known as Jumper Bd. Assy. and Jumper Assy.

CHAPTER 2
INSTALLATION

2.1 INTRODUCTION

This chapter contains instructions for the installation, configuration and operational verification of the 50 Series systems. For installation procedures of peripheral devices refer to the appropriate Service Manual for that device. To properly install a system, follow the installation instructions in the order presented.

2.2 CHECKING FOR SHIPPING DAMAGE

Prior to and during unpacking, the packaged unit should be examined for possible shipping damage. If any damage is noticed, proceed as follows:

1. DO NOT repair or install any of the damaged equipment before an insurance claim inspection is completed. Equipment may be opened to inspect for damage. When unpacking, retain all shipping material in case a module needs to be returned.

2. Have the delivering carrier's agent inspect the damage. Give a copy of the damage report to the Customer Service Administrator who will forward the report to:

   Prime Computer, Inc.
   Customer Service Material Control
   145 Pennsylvania Avenue MS 01-25
   Framingham, Ma. 01701

3. Provide a complete description of the damage and how it can be corrected. The Customer Service Administrator will contact Customer Service Material Control, who will arrange for inspection by a Prime insurance carrier and initiate activity to obtain materials necessary to correct the damage.

NOTE

Inspection by a Prime insurance carrier should occur within two working days of notifying Customer Service Material Control.

2.3 UNPACKING INSTRUCTIONS

Unpacking instructions are provided for the following:

- 50 Series Cabinets (Non-FCC)
- 50 Series Cabinet (FCC)
- Peripherals
- Miscellaneous Items and Software Boxes

NOTE

The customer is responsible for moving the equipment into its approximate location in the computer room.

2.3.1 UNPACKING 50 SERIES CABINETS (NON-FCC)

Unpacking instructions for the 50 Series Non-FCC cabinets are as follows:

1. Cut the banding straps and remove the shipping box or cover. A typically packaged system appears in Figure 2-1.

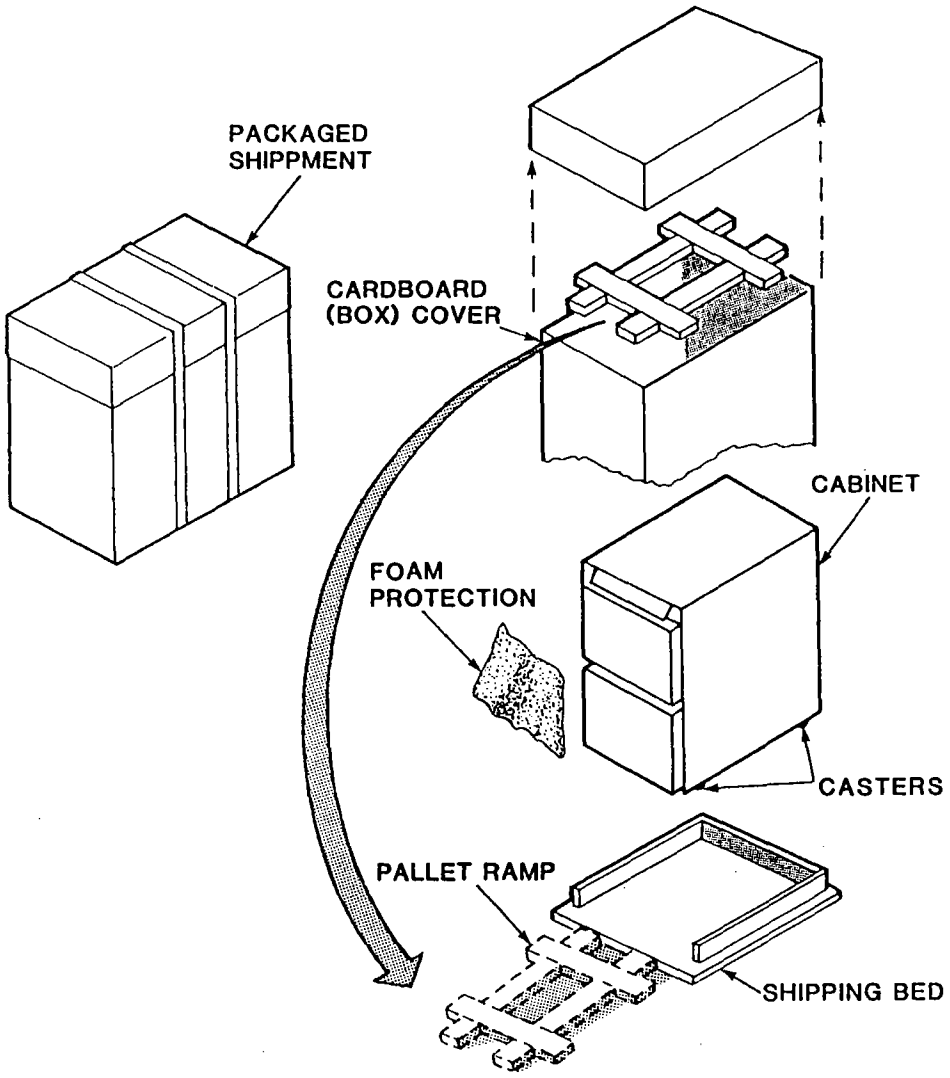


FIGURE 2-1: UNPACKING THE NON-FCC CABINET

2. Cut the banding strap binding the pallet ramp to the cabinet, remove the ramp. Install the ramp on the pallet in front of the cabinet.

WARNING

Two persons are required to remove the cabinet from the pallet.

3. Roll the cabinet down the ramp and off of the pallet. Remove any additional packing material from the cabinet and check for any signs of damage.

4. Remove required cable access panels from the cabinet and roll the cabinet into its permanent position. Lower the four leveling pads on the cabinet (Figure 2-2) until the weight on the rollers has been relieved, the cabinet is level and resting firmly on the floor.

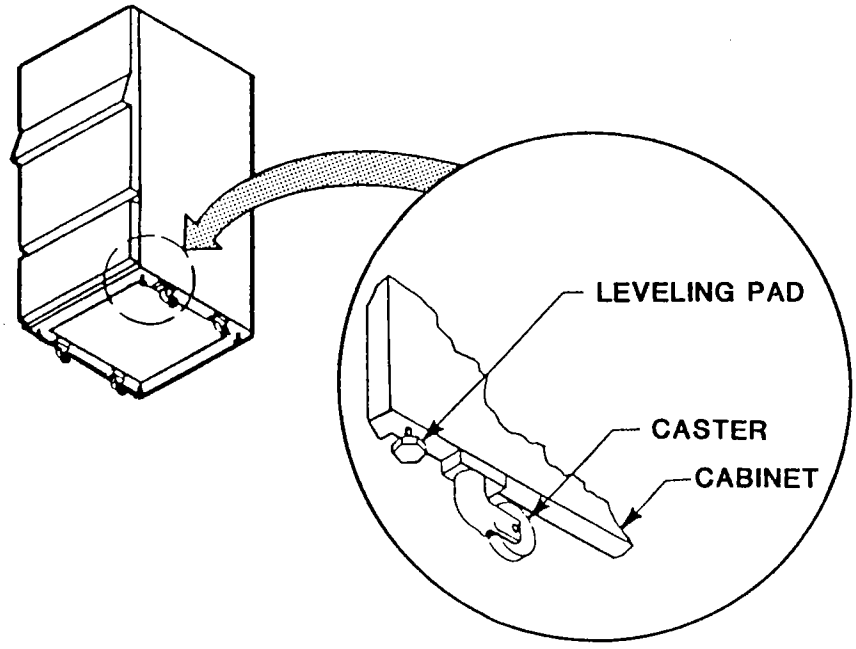


FIGURE 2-2: CABINET LEVELING PADS

5. Repeat step 4 for the other cabinet, if you are installing a dual-cabinet system. Both cabinets must rest firmly on the floor with adjacent sides completely flush. As you face them, the main CPU cabinet must be on the left and the secondary I/O cabinet must be on the right. Install the hardware supplied to bolt the cabinets together. The leveling pads may require further adjustment.

6. Remove the red shipping restraints from the boards and 1045 or 1051 power supplies in the chassis (Figure 2-3).

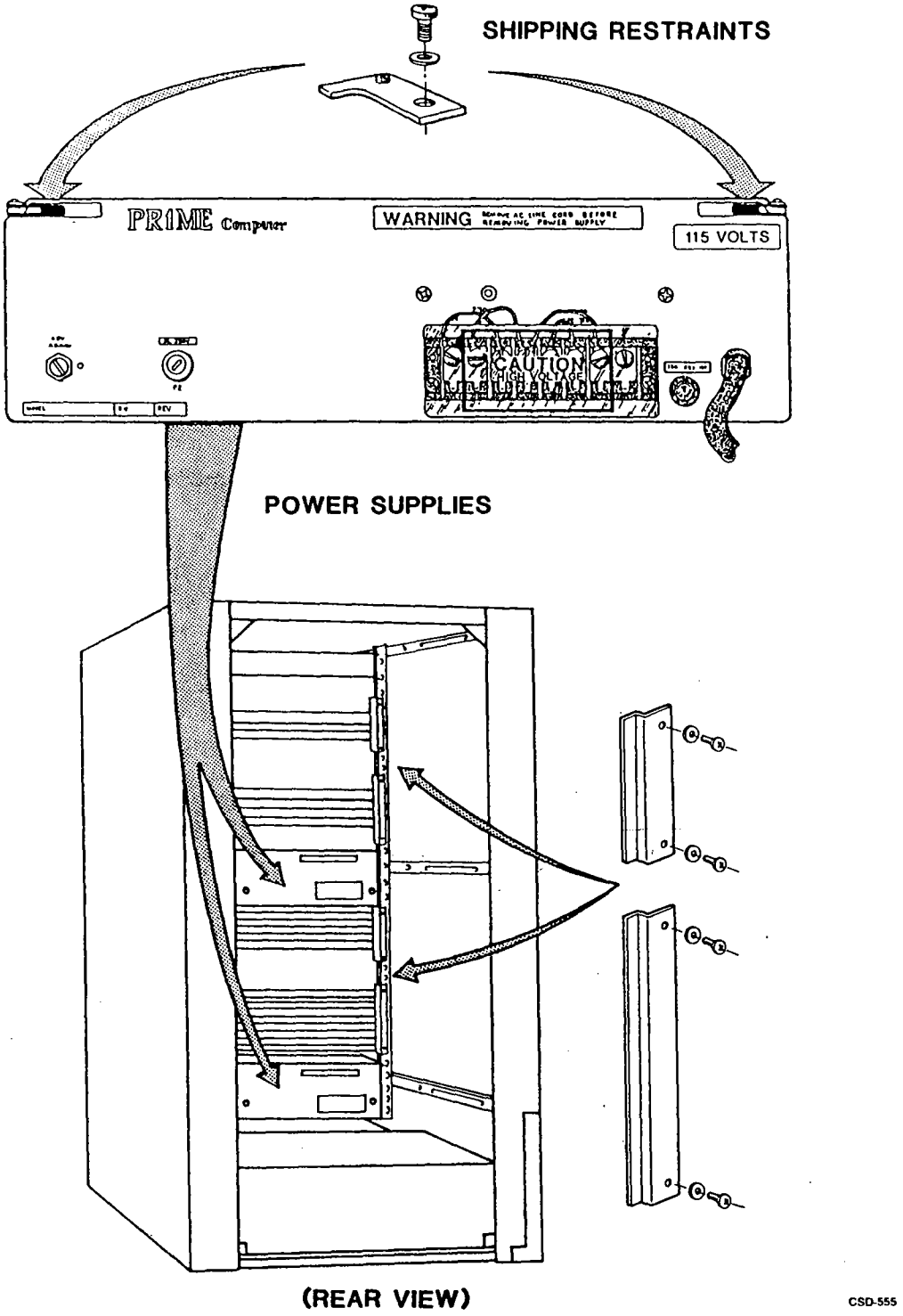


FIGURE 2-3: SHIPPING RESTRAINTS REMOVAL

2.3.2 UNPACKING A 50 SERIES CABINET (FCC)

The 50 Series System dual-bay cabinet has each bay packed separately. The I/O boards and the memory boards are also packed in separate containers. Detailed unpacking instructions follow.

NOTE

Save all of the packaging material. If the system requires repackaging, reverse the unpackaging instructions.

1. Cut the banding straps and remove the shipping carton. A typically packaged cabinet appears in Figure 2-4.

2. Remove the strapping tape that secures the pallet ramp to the cabinet and remove the ramp.

3. Install the ramp on the pallet in front of the cabinet.

4. Using a hex nut wrench, remove the four red shipping restraints that secure the cabinet to the pallet as shown in Figure 2-4.

5. Roll the cabinet down the ramp and off of the pallet. Remove any additional packing material from the cabinet and check for any signs of damage.

6. The cabinet should now be placed in the approximate location in which it will be installed.

7. Using a Phillips screwdriver, remove the red shipping restraints from the two 1051 power supplies in the chassis as shown in Figure 2-3. Each power supply has two shipping restraints, one on each side of the power supply.

8. Locate and remove the board shipping restraints secured to the rear of the card cage by Phillips screws (Figure 2-3).

2.3.3 PERIPHERALS

Unpack all cabinet-mounted and free-standing peripherals according to the instructions in the appropriate Service Manual. Move all free-standing peripherals into their permanent positions and level as required.

2.3.4 MISCELLANEOUS ITEMS AND SOFTWARE BOXES

Unpack all miscellaneous items and software boxes, as well as the following:

- Memory array boards
- I/O cables
- I/O boards

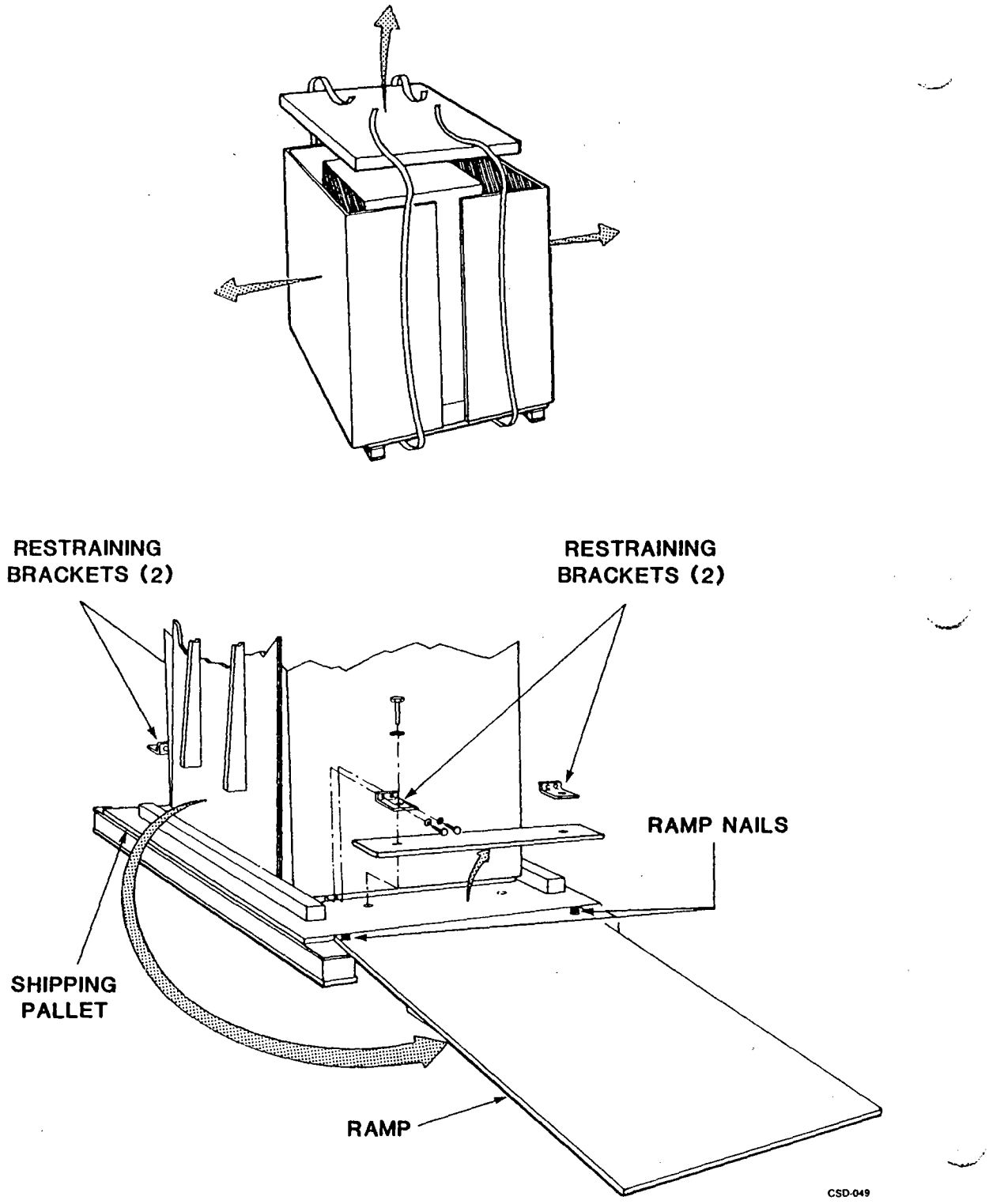


FIGURE 2-4: UNPACKING THE FCC CABINET

Lay out the cables in their approximate locations. Put the plug-end of each cable near the peripheral's bulkhead (or mating connector if no bulkhead is present). Place the receptacle-end near the bulkhead of the 50 Series cabinet. Locate all power cords and place them in their approximate locations.

2.4 INVENTORY

Complete the inventory of system hardware. Compare the inventory to the shipping list, report any missing items in the Installation Report and place a short-ship order form via the Customer Service Regional Administrator for these missing parts.

2.5 SITE SURVEY

Tables 2-1 and 2-2 list electrical and environmental specifications for the 50 Series system. Table 2-3 lists the power cords and connectors for the 50 Series system. Verify that these specifications are met for the system being installed.

TABLE 2-1: ELECTRICAL SPECIFICATIONS

SPECIFICATION	DOMESTIC	INTERNATIONAL
Voltage	208 Vac	240 Vac
Amperage (Service)	30 A	30 A
AC Input Tolerance	±10%	±10%
DC +5V Tolerance	±5%	±5%
Current - Start (Run/Phase):		
150, 250, 450, 550	130A (10A)	117A (9A)
150II, 250II, 450II	130A (10A)	117A (9A)
500, 650, 550II	150A (18A)	135A (16A)
750, 850	160A (24A)	144A (21A)
BTU Per Hour:		
150, 250, 450	8,200	7,300
150II, 250II	8,200	7,300
550, 650, 550II	14,700	13,000
750	19,700	16,000
850	23,750	18,000

TABLE 2-2: ENVIRONMENTAL SPECIFICATIONS:

OPERATING TEMPERATURE	STORAGE TEMPERATURE	HUMIDITY*
68 - 78°F (20 - 26°C)	32°F - 104°F (0 - 40°C)	20% to 80%

*Non-condensing

TABLE 2-3 : POWER CORDS AND CONNECTORS

PRODUCT CATEGORY	SERVICE	AC OUTLET	NEMA REF	POWER CORDS PROVIDED
Mainframe Cabinet (Domestic)	120/240 or 120/208 Vac	Hubbell 2713,2710 or equiv.	L14-30R	L14-30
Peripheral Cabinet (Domestic)	120Vac	Hubbell 2613,2610 or equiv.	L5-30R	L5-30 (P&R)
Mainframe& Peripheral Cabinets (Int'l)	240Vac	Hubbell 2623,2620 or equiv. (S)	L6-30R	L6-30 (P&R) (S)
Standard Free-Standing Peripherals (Int'l)	120Vac	American style ac wall socket	5-15R	5-15
Other* Free-Standing Peripherals (Domestic)	208Vac	Hubbell 2323 twistlock	L6-20R	L6-20 (P&R)
Standard Free-Standing Peripherals (Int'l)	240Vac	European style ac wall socket as applicable	6-15R (S)	5-15 (P&R) (S)
Other* Free-Standing Peripherals (Int'l)	240Vac	Hubbell 2333 twistlock (S)	L7-20R (S)	L7-20 (P&R) (S)

KEY:

(S) - Suggested
* - 300Mb SMD, Card Reader/Punch, Character Band Reader
(P&R) - Plug and Receptacle

2.6 PRINTED CIRCUIT BOARD (PCB) CURRENT SPECIFICATIONS

The +5V current specifications for the 50 Series PCBs are listed in Table 2-4.

TABLE 2-4: OPERATING SPECIFICATIONS: DC CURRENT DRAW PER BOARD

BOARD NAME	BOARD TYPE	+5C CC1 (AMPS)
CPU BOARDS:		
200 CPU (one-board processor)	2502-257	15.1
300 CPU (one-board processor)	2503-360	15.6
400 CPU [A Board]	2241-902	24.5
400 CPU [B Board]	2242-902	18.6
450,150-II,250-II CPUs [A Board]	2247-901	22.0
450,150-II,250-II CPUs [B Board]	2248-901	18.5
550,650,450-II, 550-II CPUs [A Board]	2278-901	21.3
550,650,450-II, 550-II CPUs [B Board]	2279-901	19.1
550,650,450-II, 550-II CPUs [XIS Board]	2253-902	19.2
750 (850) CPU [A Board]	2250-902 (2285-901)	17.8
750 (850) CPU [C Board]	2262-902 (2274-901)	17.9
750 (850) CPU [CS Board]	2263-902 (2275-901)	19.8
750 (850) CPU [J Board]	2268-901 (2273-901)	17.7
750 (850) CPU [XIS Board]	2264-901 (2286-901)	20.5
I/O BOARDS:		
AMLC (16-line)	5154-901	8.6
BMSMC (Burst Mode Storage Module)	4005-901	10.2
BMTC (Burst Mode Tape)	2023-901	13.5
DDF-MTC (Integrated Formatter)	2270-901	12.3
DTC (Tape only)	6105-902	4.2
FMTR (Formatter)	2269-901	7.0
ICS1	2036-901	6.7
ICS2	2034-901	12.8
MACI (6-line)	5402-001	5.0
MDLC (2-line)	5602-903	11.1
MDLC (4-line)	5602-913	11.5
MTC (9-track)	2081-902	10.2
MTC (NRZ1)	4020-902 (2295-901)	10.2
OPT-A	3003-901	6.1
PNC	2257-902	12.7
SMC	4004-94X	10.1
SOC	3006	7.8
STSC (Streamer)	2301-901	6.9
URC	3156-901 (2294-90X)	10.3
VCP	2265-902	15.8

TABLE 2-4: OPERATING SPECIFICATIONS: DC CURRENT DRAW PER BOARD (Cont.)

BOARD NAME	BOARD TYPE	+5C CC1 (AMPS)
MEMORY BOARDS:		
32Kb MEMORY	1232-B1085	2.4
256Kb MEMORY	12128-E4	4.2
256Kb WW MEMORY	12128-E6	5.3
512Kb WW MEMORY	12256-E7	5.5
1024Kb (1Mb) WW MEMORY	12512-E8	5.7
1024Kb (1Mb) WW MEMORY (E9)	7615-XXX	6.4
I/O TESTER*	MEC2024-901	6.2

* NOTE: This item is test equipment for Repair Center only.

2.7 VOLTAGE AND FREQUENCY CONVERSIONS

The 50 Series system should be configured to accept the ac line voltage available. To check that the system has been properly configured, locate the model number plate located on the rear of each 1045 and 1051 power supply. If a 901 suffix follows the model number, the power supply has been configured for domestic use. A 902 suffix indicates that the model is configured for international use.

If the improper suffix follows the model number, convert the 1045 or 1051 power supply as outlined in one of the following procedures.

NOTE

If the incorrect PDU or blower unit has been shipped with the system, a complete new unit should be ordered. The PDU and blower units cannot be converted in the field. Removal and replacement procedures for these units are located in Chapter 7.

2.7.1 1045 POWER SUPPLY CONVERSION

Convert the 1045 power supply from 115 Vac (60 Hz) to 230 Vac (50 Hz) service using the steps below. Refer to Figure 2-5 during the procedure.

1. Locate and remove the internal jumper cable (part number CBL8259-901) as shown in Figure 2-5.

CAUTION

Failure to remove/add this jumper when converting to/from 115 Vac will cause damage to the supply.

2. Change the jumpers on the terminal strip for 230 Vac operation as shown in Figure 2-5.

3. Change the 15A fuse (SLO-BLO) to 10A (SLO-BLO).

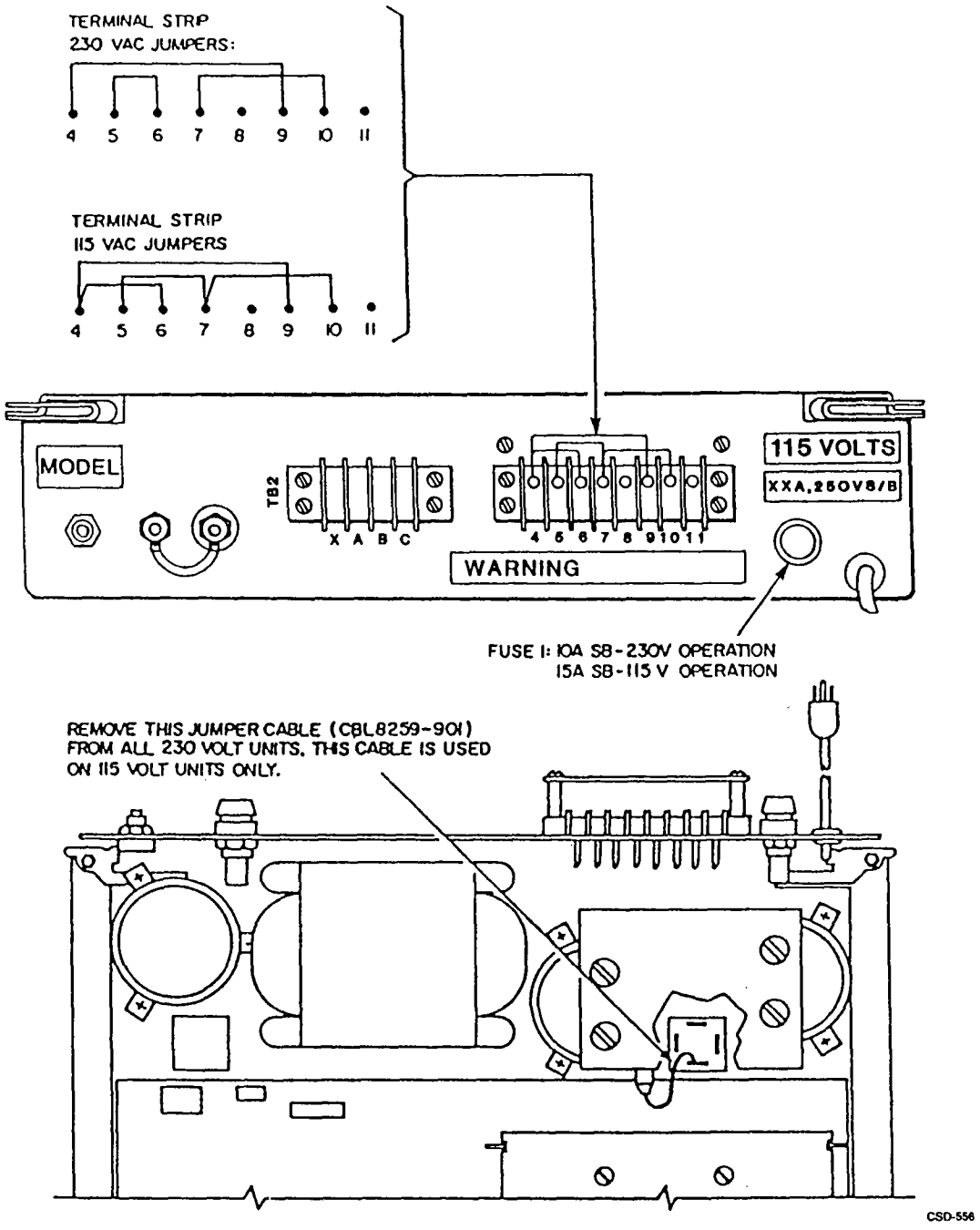


FIGURE 2-5: 1045 POWER SUPPLY CONVERSION JUMPERS

2.7.2 1051 POWER SUPPLY CONVERSION

Convert the 1051 power supply from 115 Vac (60 Hz) to 230 Vac (50 Hz) service using the following steps. Refer to Figure 2-6 during the procedure.

1. Locate and remove the internal jumper cable (part number CBL8259-901) as shown in Figure 2-6.

CAUTION

Failure to remove/add this jumper when converting to/from 115 Vac will cause damage to the supply.

2. Change the jumpers on the terminal strip for 230 Vac operation as shown in Figure 2-6.

3. Change the 15A fuse (SLO-BLO) to 10A (SLO-BLO).

4. Change the 3A fuse (SLO-BLO) to 2.0A (SLO-BLO) for international operation.

2.8 SYSTEM INSTALLATION

System installation procedures are presented in the following order:

- 850 Dual-Cabinet (Non-FCC) Installation
- 850 Dual-Cabinet (FCC) Installation
- CPU Verification & Top Hat Installation
- Memory Board Installation Procedure
- I/O Cabling Guidelines
- 1045/1051 Power Supply Installation Verification
- Uninterruptible Power Supply (UPS) Installation
- PDU Cabling
- System Console Installation
- System Configuration
- Free-Standing Peripheral Cabling
- Peripheral Equipment Grounding

2.8.1 850 DUAL-CABINET (NON-FCC) INSTALLATION

The 850 system is contained in two cabinets, the Mainbay cabinet and the I/O cabinet. Installation of the cabinets is described as follows.

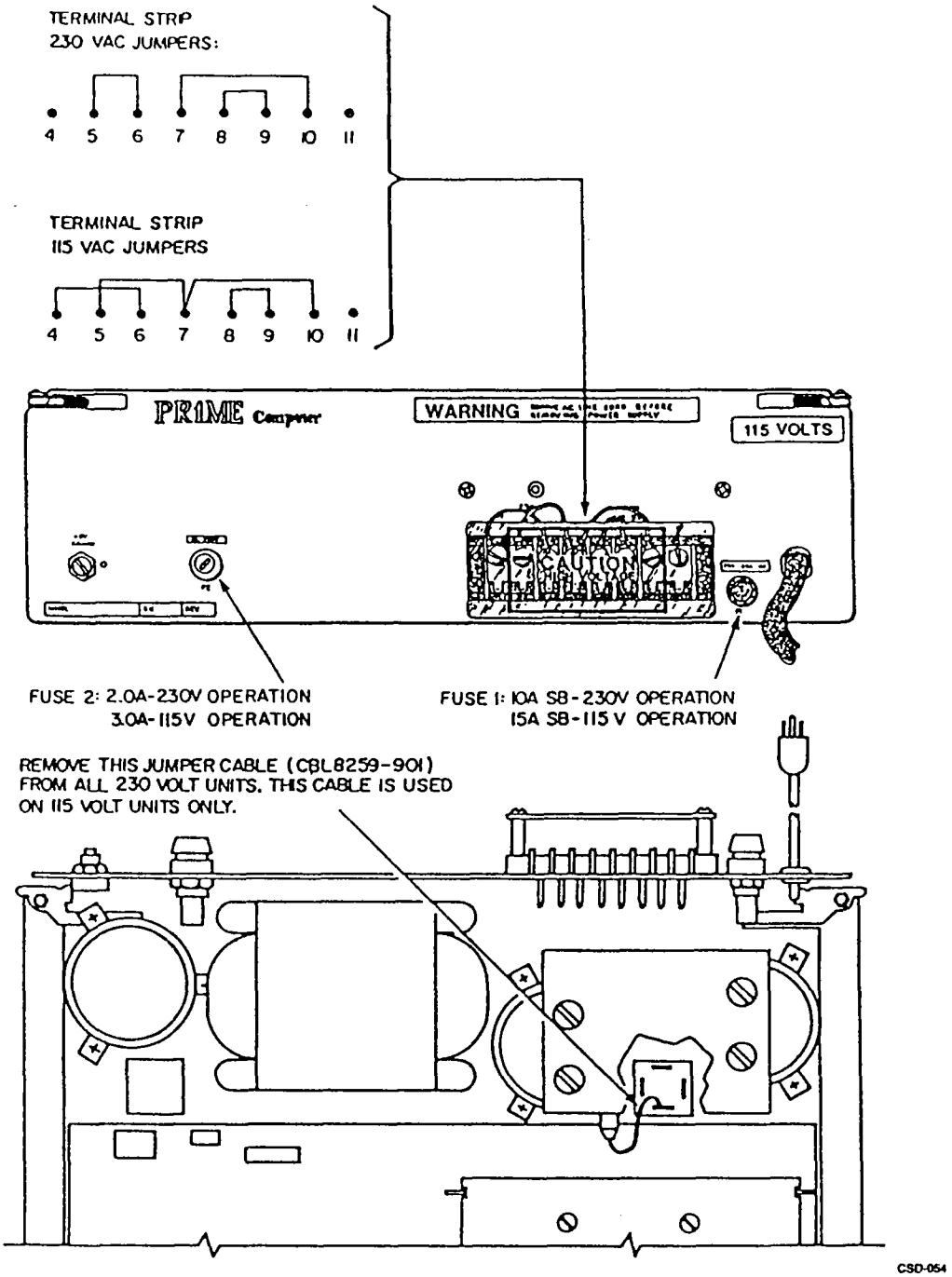


FIGURE 2-6: 1051 POWER SUPPLY CONVERSION JUMPERS

2.8.1.1 Dual-Cabinet VCP Bezel Installation

Install the Dual-Cabinet VCP Bezel as follows:

1. Verify that the Mainbay cabinet and the I/O cabinet have been bolted together as noted in the Unpacking section.

2. Remove the VCP bezel panel from its packaging, and locate the hardware (4 screws, 4 washers) necessary to install it.

3. Lay the bezel over the top of the two cabinets with the hinges hanging down over the front of the cabinets. The hinge slots should be located directly over the threaded holes.

4. Install the four screws through the hinge slots on each side of the bezel. The screws should not be tightened at this time.

5. Align the bezel so that it is flush with both the sides and the top of the cabinets, and tighten the four screws.

6. Place the bezel in its upright position, then mate the A and B connectors of the cabinet with the A and B connectors of the VCP bezel.

7. Leave the bezel in its upright position for interchassis I/O cable installation procedure (see Figure 2-7).

2.8.1.2 Dual-Cabinet Interchassis I/O Cable Installation

The PCBs should be seated in the chassis as shown in Figures 2-8 and 2-9.

1. Verify that the VCP bezel is in its upright position.

2. Locate the six ribbon cables to be used for interchassis I/O connection.

3. Install these cables as shown in Figures 2-7. Ensure that the cables are folded carefully and held by the supplied plastic clips, so as to prevent damage by VCP bezel. Also make certain that the cables are installed using the cabinet-mounted strain relief.

4. Close the VCP bezel carefully. The I/O ribbon cables should not interfere with the closing of the bezel in any way. If they do, they must be repositioned accordingly.

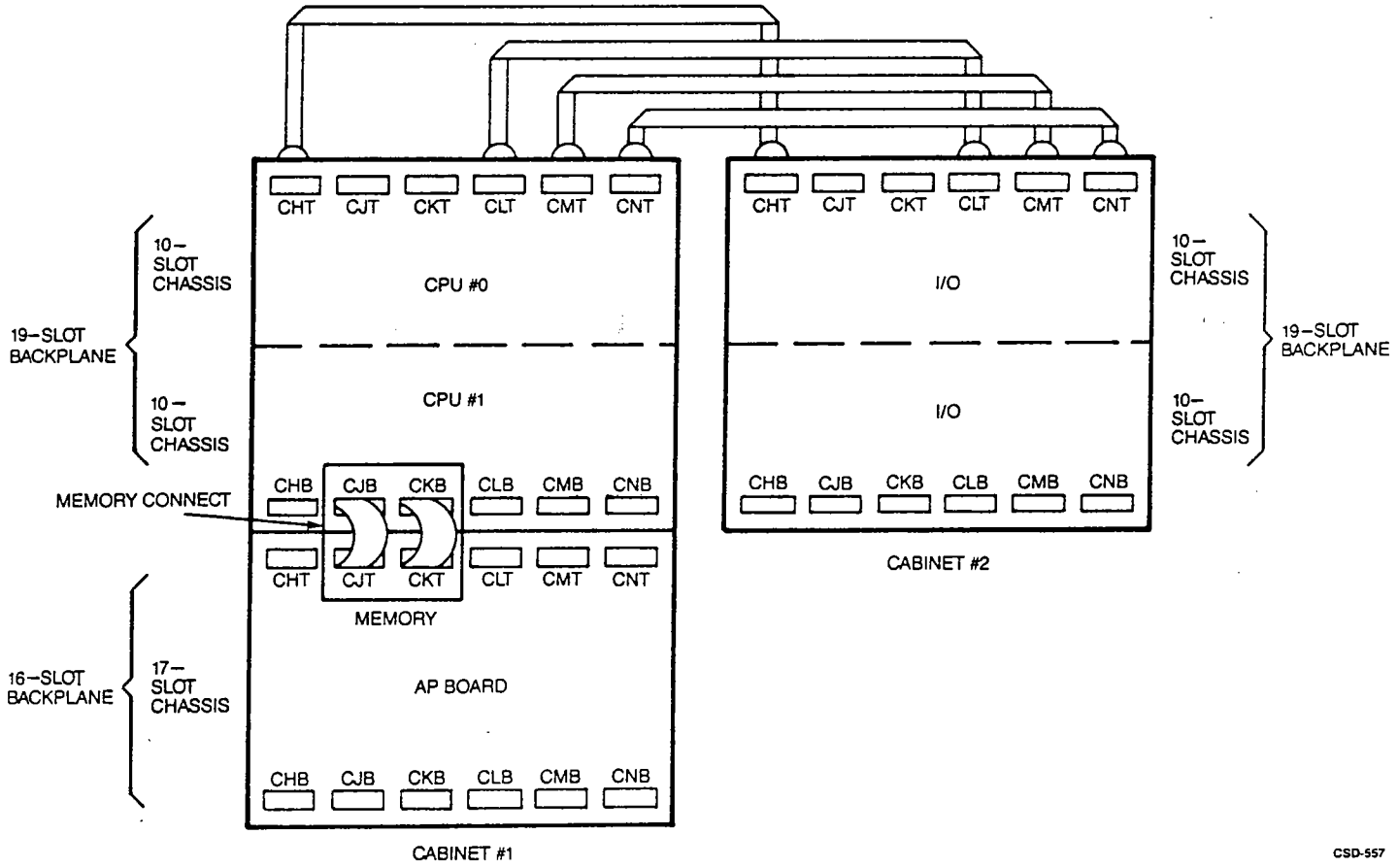


FIGURE 2-7: DUAL CHASSIS LAYOUT AND CHASSIS INTERCONNECTION

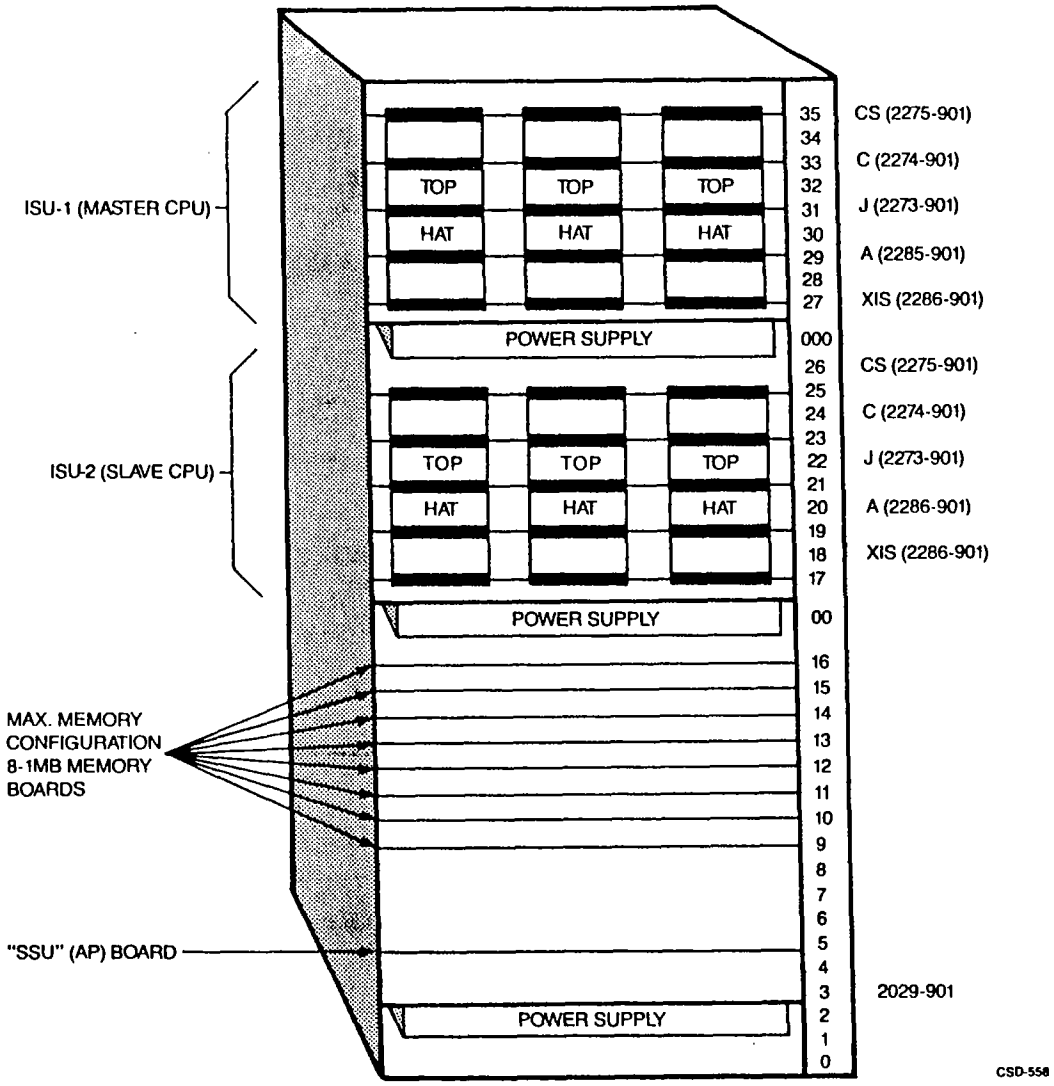


FIGURE 2-8: 850 MAIN BAY CABINET

2.8.2 850 DUAL CABINET (FCC) INSTALLATION

The 850 system is contained in two cabinets, the Mainbay cabinet and the I/O cabinet (Figures 2-8 and 2-9). Installation of the cabinets is described as follows.

2.8.2.1 Joining The Cabinets

Perform the following procedure to mechanically join the mainbay and I/O cabinets.

WARNING

Prior to joining the cabinets, do not open the front and side doors of a single cabinet at the same time. Doing so could result in personal injury and/or damage to the equipment.

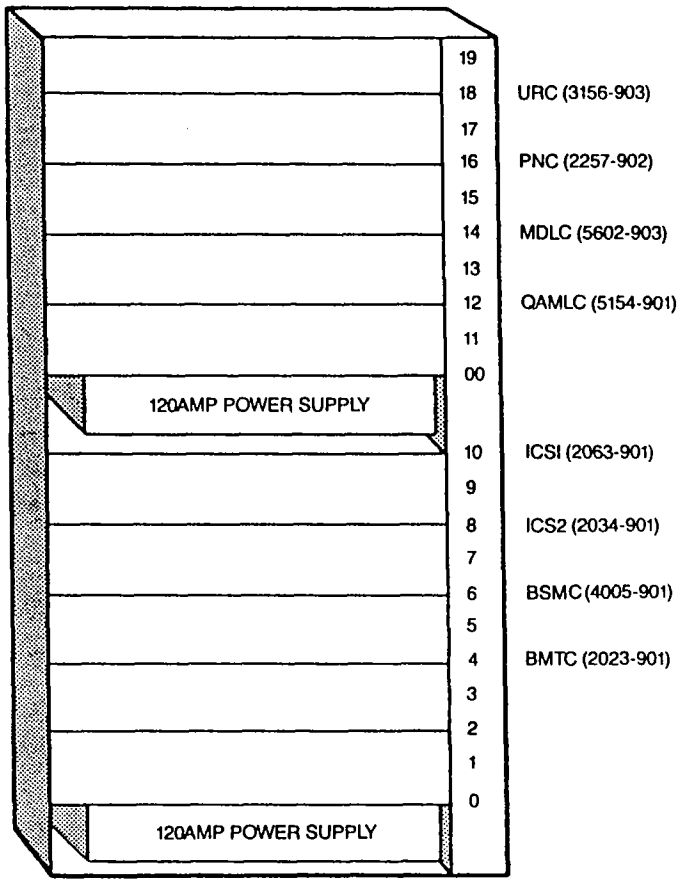


FIGURE 2-9: 850 I/O CABINET

Refer to Figure 2-10 during procedure steps 1 through 11.

1. Place the cabinets in their approximate location in the computer room. Facing the front of the cabinets, the mainbay cabinet is placed on the right and the I/O cabinet on the left.

2. Open the front door to the I/O cabinet.

3. Using a Phillips screwdriver, remove the four screws from the front collar.

4. Using a 3/8-inch hex-nut driver, remove the nut, lock washer and washer from the threaded-stud screw protruding from the front of the I/O cabinet top cover.

5. Go to the rear of the I/O cabinet and open the rear door.

6. Using a Phillips screwdriver, remove the four screws from the rear of the cabinet frame.

7. Using a 3/8-inch hex-nut driver, remove the nut, lock washer, and washer from the threaded-stud screw protruding from the rear of the I/O cabinet top cover.

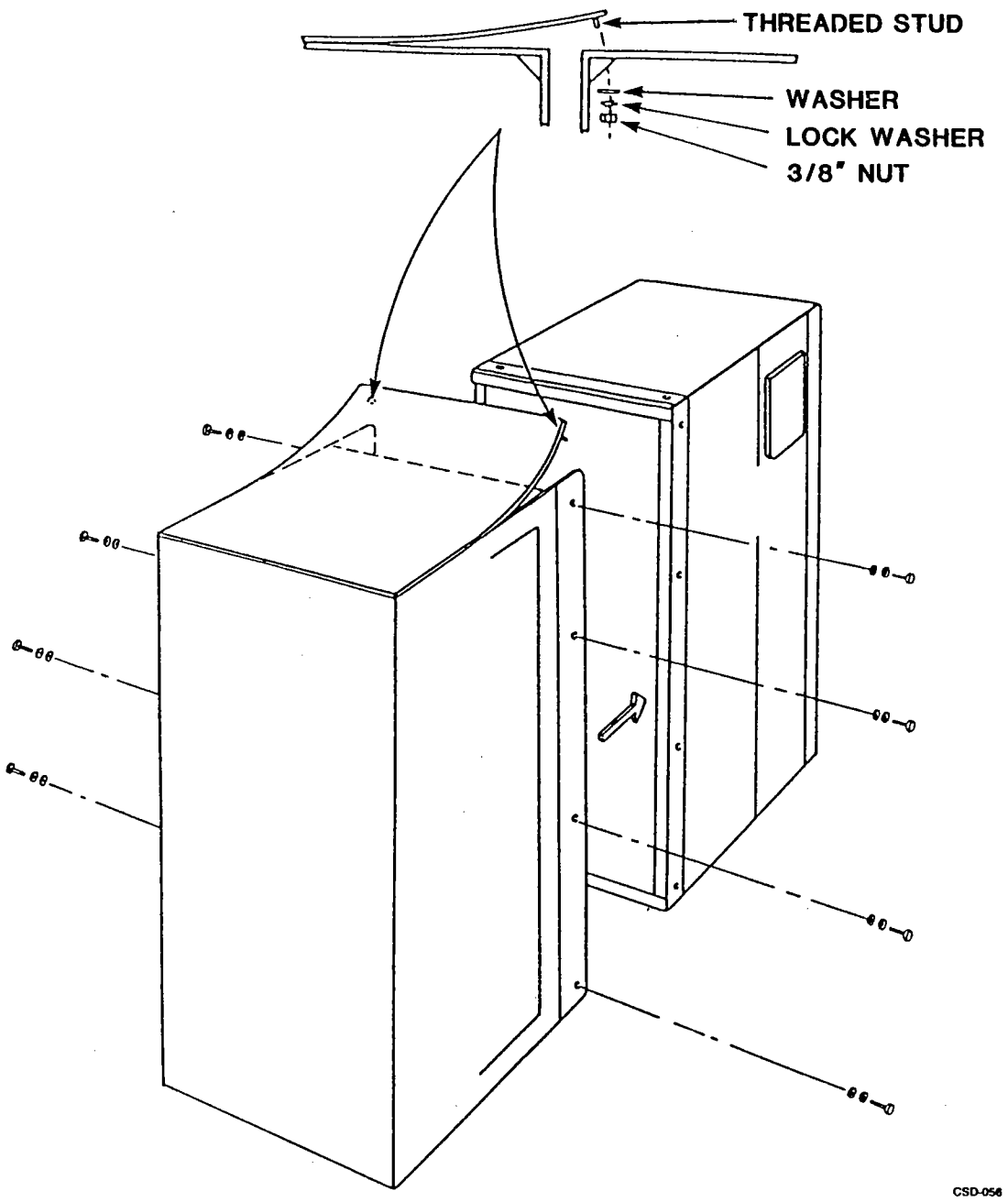


FIGURE 2-10: JOINING THE CABINETS

8. Raise the I/O cabinet top cover. Keep the cover in an elevated position by inserting an object underneath the cover. This prevents damage to the threaded-stud screws when joining the two cabinets.

9. Push the two cabinets together. Make sure the threaded-stud screws fall into the holes on the top of the mainbay cabinet by guiding the screws into the holes.

NOTE

The top panel on the mainbay cabinet may have to be loosened in order to align the screws and holes properly.

10. Replace the screws on the front and rear collars to secure the two cabinets.

11. Replace the two sets of nuts and washers that were removed in steps 4 and 7. The rear threaded-stud screw is easily accessible but the threaded-stud screw located on the front of the cabinet may be difficult to reach.

Refer to Figure 2-11 during procedure step 12.

12. Install the non-skid leveling leg into the front right corner of the mainbay cabinet. Turn the leg clockwise and lower it to the floor. Repeat this step for the leg under the front left corner of the I/O cabinet. Tighten the legs by turning them counter-clockwise.

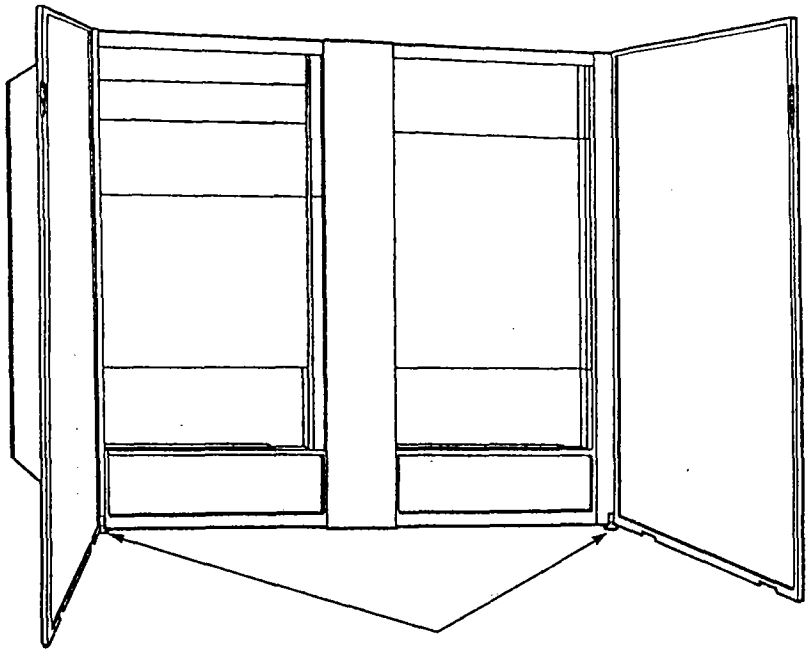


FIGURE 2-11: LEVELING LEGS

2.8.2.2 Dual (FCC) Cabinet Inter-Cabinet Cabling

Cable the inter-cabinet cables as follows:

1. Locate and install the six ribbon cables used for interchassis I/O connection (Figures 2-7 and 2-12).

2. Install the cable from connectors B and C of the status panel to connector J12 of the PDU (Figure 2-10).

3. Install the cable from blower assembly 2 to connector J8 of the PDU (Figure 2-12).

2.8.3 CPU VERIFICATION & TOP-HAT INSTALLATION

The typical 50 Series configurations are shown in Figures 2-8, 2-13 and 2-14. To install the top-hat connectors:

1. Verify that the boards are in their proper slots.

2. Inspect the top-hats for damage to the housing and pins. Do not attempt to install defective top-hats.

3. Install the top-hat connectors on the CPU boards. Verify that the top-hats are firmly seated and that the CPU boards are installed in their proper slots.

CAUTION

The correct way to install the top-hat is to put it on the uppermost board of the set. Move the top-hat from side to side until it centers with minimal pressure and snaps on. Once the first connection is made, the other connectors will snap on easily. Do not bang the top hat on.

2.8.4 MEMORY BOARD INSTALLATION PROCEDURE

The E6, E7, E8 and E9 wide word memory boards (2 x 16-bit words) are the standard memory for the 50 Series machines. Wide-word memory allows two words (32 bits) to be transferred at one time. Standard memory allows one word (16 bits) to be transferred at one time. Switch settings allow the memory boards to operate with the different types of CPUs.

The wide-word memory provides the same functionality as the 12128-E4 ECC memory. It also has the capability of using the memory address bus for a data word transfer. This capability allows for two memory locations to be transferred at the same time: one on the address bus and one on the data bus.

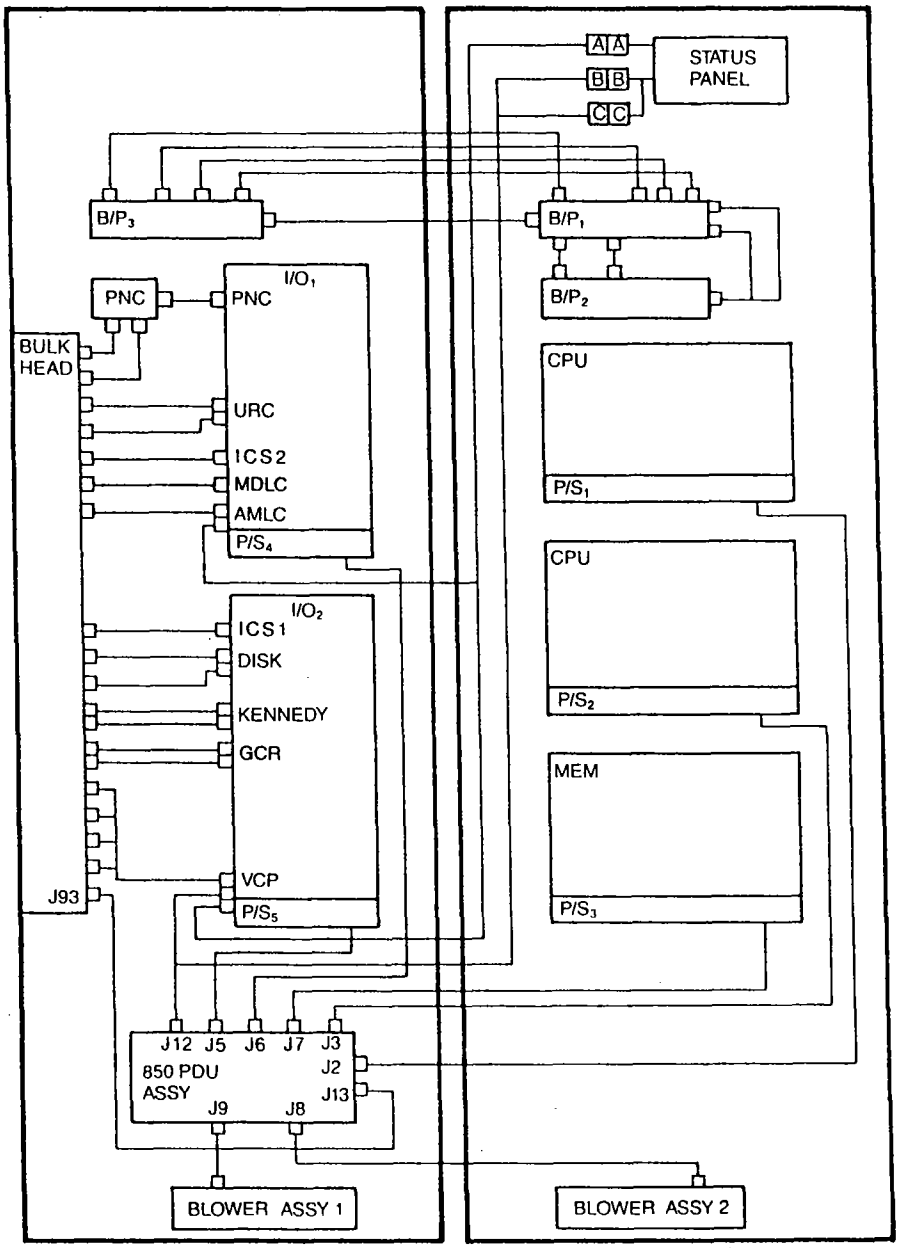


FIGURE 2-12: 850 FCC CABINETS CABLING OVERVIEW

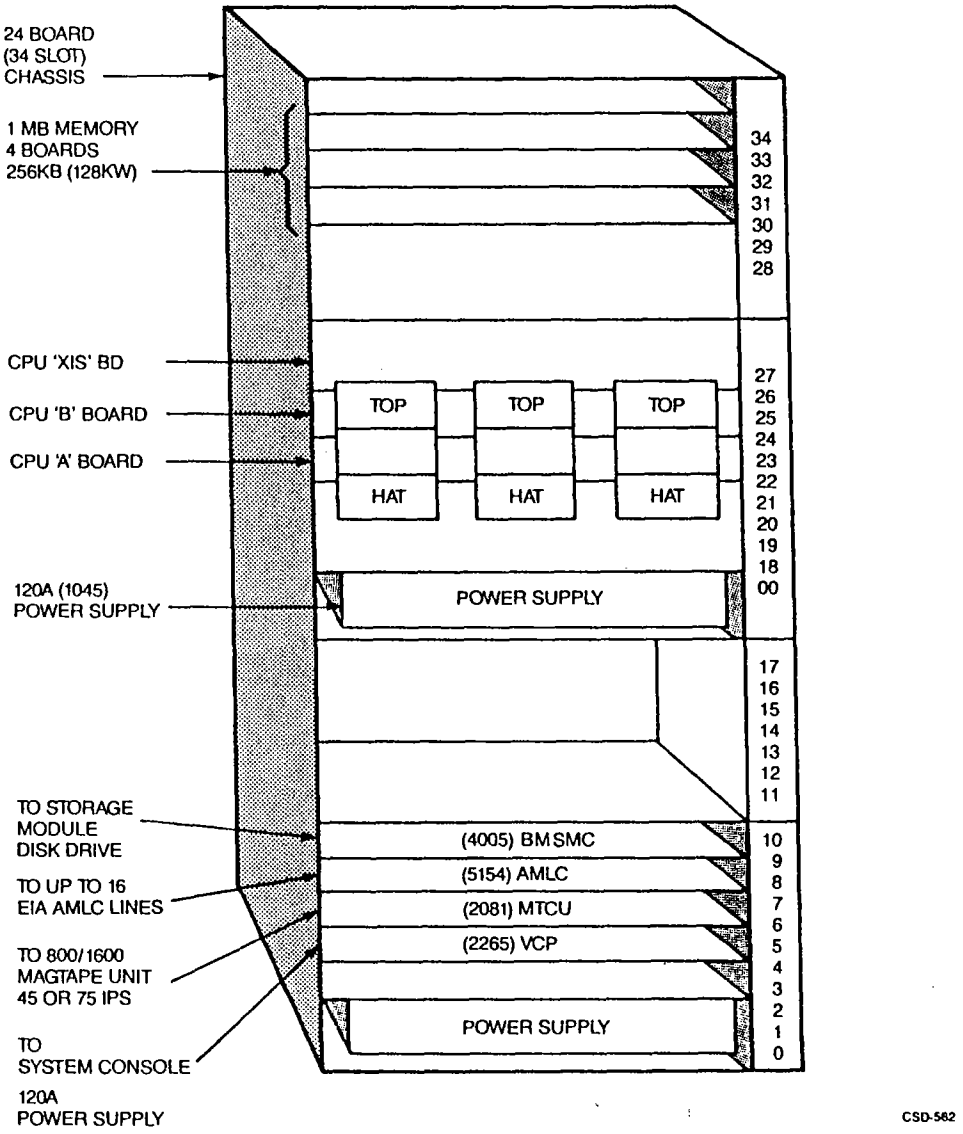


FIGURE 2-13: 550-II CABLING

Table 2-5 lists the capacity of each type of board.

TABLE 2-5: MEMORY BOARD CAPACITY

MEMORY BOARD	CAPACITY
12128-E6	.25 Mb
12256-E7	.50 Mb
12512-E8	1.00 Mb
7615-902 (E9)	1.00 Mb

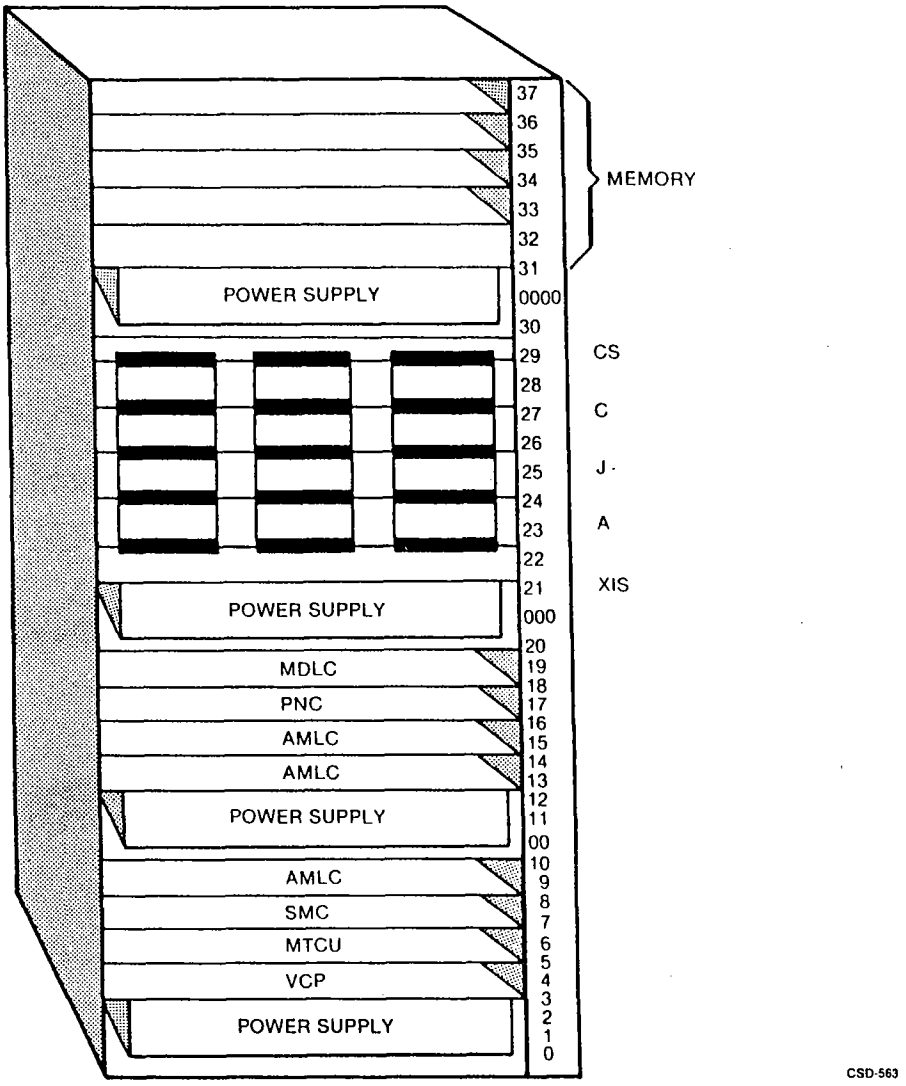


FIGURE 2-14: 750 CABINET

2.8.4.1 Handling E6, E7, E8 and E9 Memory Boards

The following information is provided to prevent damage to memory boards used in the 50 Series systems.

CAUTION

MOS IC chips can be easily damaged by a discharge of static electricity. When handling MOS memory boards (E6, E7 and E8), adhere to the following rules:

- Before handling the boards, momentarily touch a solid ground to eliminate the static charge from your body.
- Avoid unnecessary handling of the board when the board is out of its protective shipping bag.
- Avoid carpeted floors (especially in low humidity areas) when handling the boards out of their shipping bags.

Use the Field Service Grounding Kit (TEATTFSKIT) whenever handling of E6, E7, E8 and E9 boards is required. The kit consists of a 15-foot ground cord, work surface and 5-foot wrist strap. Use the following procedure:

1. Attach the work surface to ground via the 15-foot ground cord. Ground can be equipment frames, electrical conduits, building frames or water pipes.

2. Attach the wrist strap to ground via the 5-foot ground cord.

3. Slip on the wrist strap.

4. When removing a memory board be sure to place it on the grounded work surface. Always place the board in a static shielding bag if further handling or shipping is required.

2.8.4.2 Memory Configuration

Rules for configurating memory to a system are as follows:

1. E6, E7, E8 and E9 memories may be mixed in the CPU chassis, but not in the memory extender chassis. 12128-E4 (256Kb) non-wide-word memories may be substituted for E6 memories in most systems; however, E4 memories may not be used in the P750 or 850. In older systems, 256Kb and 64Kb memory may be mixed in the CPU chassis, but not in the memory extender chassis.

2. E6/E7/E8/E9 memories resident in a P750/850 system should be configured for wide-word interleaved mode (switches 2,3,4,6 ON only); in all other processors they should be set up as non-wide-word interleaved (switches 2,4,6 ON only).

3. Address overlap between memories is not permissable. Memory boards respond to the addresses shown in Table 2-6. Tables 2-7 through 2-18 list all possible 50 Series fully interleaved memory configurations. Tables 2-6 through 2-18 refer to a 35-slot chassis. These tables can be used with any size chassis by substituting the slot numbers with slot numbers of the chassis in question, starting with the top slot of the memory chassis.

NOTE

The slash convention (\ /) used in the standard memory configuration section denotes interleaved memory pairs.

TABLE 2-6: 50 SERIES MEMORY ADDRESSING

SLOT #	PHYSICAL PAGE NUMBER:		
	12128-E6	12256-E7	12512-E8 7615-902 (E9)
35	0000-0177	0000-0377	0000-0777
34	0200-0377	0400-0777	1000-1777
33	0400-0577	1000-1377	2000-2777
32	0600-0777	1400-1777	3000-3777

TABLE 2-6: 50 SERIES MEMORY ADDRESSING (Cont.)

SLOT #	PHYSICAL PAGE NUMBER:		
	12128-E6	12256-E7	12512-E8 7615-902 (E9)
31	1000-1177	2000-2377	4000-4777
30	1200-1377	2400-2777	5000-5777
29	1400-1577	3000-3377	6000-6777
28	1600-1777	3400-3777	7000-7777

TABLE 2-7: 50 SERIES MEMORY SIZE CONFIGURATIONS - 2.0 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E8 or E9 (902)	0000-1777 \	E7	0000-0777 \
34	E8 or E9 (902)	0000-1777 /	E7	0000-0777 /
33	----------	----------	E7	1000-1777 \
32	----------	----------	E7	1000-1777 /
31	----------	----------	----------	----------
30	----------	----------	----------	----------
29	----------	----------	----------	----------
28	----------	----------	----------	----------
35	E7	0000-0777 \	E6	0000-0377 \
34	E7	0000-0777 /	E6	0000-0377 /
33	----------	----------	E6	0400-0777 \
32	----------	----------	E6	0400-0777 /
31	E6	1000-1377 \	E6	1000-1377 \
30	E6	1000-1377 /	E6	1000-1377 /
29	E6	1400-1777 \	E6	1400-1777 \
28	E6	1400-1777 /	E6	1400-1777 /

TABLE 2-8: 50 SERIES MEMORY SIZE COFIGURATIONS - 2.5 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E6	0000-0377 \	E6	0000-0377 \
34	E6	0000-0377 /	E6	0000-0377 /
33	E8 or E9 (902)	2000-3777 \	E7	1000-1777 \
32	E8 or E9 (902)	2000-3777 /	E7	1000-1777 /
31	----------	----------	E7	2000-2777 \
30	----------	----------	E7	2000-2777 /
29	----------	----------	----------	----------
28	----------	----------	----------	----------
35	E6	0000-0377 \		
34	E6	0000-0377 /		
33	E6	0400-0777 \		
32	E6	0400-0777 /		
31	E6	1000-1377 \		
30	E6	1000-1377 /		
29	E7	3000-3777 \		
28	E7	3000-3777 /		

TABLE 2-9: 50 SERIES MEMORY SIZE CONFIGURATIONS - 3.0 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E8 or E9 (902)	0000-1777 \	E7	0000-0777 \
34	E8 or E9 (902)	0000-1777 /	E7	0000-0777 /
33	----------	----------	E7	1000-1777 \
32	----------	----------	E7	1000-1777 /
31	E7	2000-2777 \	E7	2000-2777 \
30	E7	2000-2777 /	E7	2000-2777 /
29	----------	----------	----------	----------
28	----------	----------	----------	----------
35	E6	0000-0377 \	E6	0000-0377 \
34	E6	0000-0377 /	E6	0000-0377 /
33	E8 or E9 (902)	2000-3777 \	E6	0400-0777 \
32	E8 or E9 (902)	2000-3777 /	E6	0400-0777 /
31	E6	1000-1377 \	E7	2000-2777 \
30	E6	1000-1377 /	E7	2000-2777 /
29	----------	----------	E7	3000-3777 \
28	----------	----------	E7	3000-3777 /

TABLE 2-10: 50 SERIES MEMORY SIZE CONFIGURATIONS - 3.5 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E6	0000-0377 \	E6	0000-0377 \
34	E6	0000-0377 /	E6	0000-0377 /
33	E7	1000-1777 \	E7	1000-1777 \
32	E7	1000-1777 /	E7	1000-1777 /
31	E8 or E9 (902)	4000-5777 \	E7	2000-2777 \
30	E8 or E9 (902)	4000-5777 /	E7	2000-2777 /
29	----------	----------	E7	3000-3777 \
28	----------	----------	E7	3000-3777 /
35	E6	0000-0377 \		
34	E6	0000-0377 /		
33	E6	0400-0777 \		
32	E6	0400-0777 /		
31	E6	1000-1377 \		
30	E6	1000-1377 /		
29	E8 or E9 (902)	6000-7777 \		
28	E8 or E9 (902)	6000-7777 /		

TABLE 2-11: 50 SERIES MEMORY SIZE CONFIGURATIONS - 4.0 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E8 or E9 (902)	0000-1777 \	E8 or E9 (902)	0000-1777 \
34	E8 or E9 (902)	0000-1777 /	E8 or E9 (902)	0000-1777 /
33	E8 or E9 (902)	2000-3777 \	----------	----------
32	E8 or E9 (902)	2000-3777 /	----------	----------
31	----------	----------	E7	2000-2777 \

TABLE 2-11: 50 SERIES MEMORY SIZE CONFIGURATIONS - 4.0 MB (Cont.)

SLOT NO.	TYPE	PPN	TYPE	PPN
30	----------		E7	2000-2777 /
29	----------		E7	3000-3777 \
28	----------		E7	3000-3777 /
35	E7	0000-0777 \	E7	0000-0777 \
34	E7	0000-0777 /	E7	0000-0777 /
33	E7	1000-1777 \	E8 or E9 (902)	2000-3777 \
32	E7	1000-1777 /	E8 or E9 (902)	2000-3777 /
31	E7	2000-2777 \	E6	1000-1377 \
30	E7	2000-2777 /	E6	1000-1377 /
29	E7	3000-3777 \	E6	1400-1777 \
28	E7	3000-3777 /	E6	1400-1777 /

TABLE 2-12: 50 SERIES MEMORY SIZE CONFIGURATIONS - 4.5 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E6	0000-0377 \	E6	0000-0377 \
34	E6	0000-0377 /	E6	0000-0377 /
33	E8 or E9 (902)	2000-3777 \	E7	1000-1777 \
32	E8 or E9 (902)	2000-3777 /	E7	1000-1777 /
31	E8 or E9 (902)	4000-5777 \	E7	2000-2777 \
30	E8 or E9 (902)	4000-5777 /	E7	2000-2777 /
29	----------		E8 or E9 (902)	6000-7777 \
28	----------		E8 or E9 (902)	6000-7777 /

TABLE 2-13: 50 SERIES MEMORY SIZE CONFIGURATIONS - 5.0 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E7	0000-0777 \	E7	0000-0777 \
34	E7	0000-0777 /	E7	0000-0777 /
33	E8 or E9 (902)	2000-3777 \	E7	1000-1777 \
32	E8 or E9 (902)	2000-3777 /	E7	1000-1777 /
31	E8 or E9 (902)	4000-5777 \	E7	2000-2777 \
30	E8 or E9 (902)	4000-5777 /	E7	2000-2777 /
29	----------		E8 or E9 (902)	6000-7777 \
28	----------		E8 or E9 (902)	6000-7777 /
35	E6	0000-0377 \		
34	E6	0000-0377 /		
33	E6	0400-0777 \		
32	E6	0400-0777 /		
31	E8 or E9 (902)	4000-5777 \		
30	E8 or E9 (902)	4000-5777 /		
29	E8 or E9 (902)	6000-7777 \		
28	E8 or E9 (902)	6000-7777 /		

TABLE 2-14: 50 SERIES MEMORY SIZE CONFIGURATIONS - 5.5 MB

SLOT NO.	TYPE	PPN
35	E6	0000-0377 \
34	E6	0000-0377 /
33	E7	1000-1777 \
32	E7	1000-1777 /
31	E8 or E9 (902)	4000-5777 \
30	E8 or E9 (902)	4000-5777 /
29	E8 or E9 (902)	6000-7777 \
28	E8 or E9 (902)	6000-7777 /

TABLE 2-15: 50 SERIES MEMORY SIZE CONFIGURATIONS - 6.0 MB

SLOT NO.	TYPE	PPN	TYPE	PPN
35	E7	0000-0777 \	E8 or E9 (902)	0000-1777 \
34	E7	0000-0777 /	E8 or E9 (902)	0000-1777 /
33	E7	1000-1777 \	E8 or E9 (902)	2000-3777 \
32	E7	1000-1777 /	E8 or E9 (902)	2000-3777 /
31	E8 or E9 (902)	4000-5777 \	E8 or E9 (902)	4000-5777 \
30	E8 or E9 (902)	4000-5777 /	E8 or E9 (902)	4000-5777 /
29	E8 or E9 (902)	6000-7777 \	----------	----------
28	E8 or E9 (902)	6000-7777 /	----------	----------

TABLE 2-16: 50 SERIES MEMORY SIZE CONFIGURATIONS - 6.5 MB

SLOT NO.	TYPE	PPN
35	E6	0000-0377 \
34	E6	0000-0377 /
33	E8 or E9 (902)	2000-3777 \
32	E8 or E9 (902)	2000-3777 /
31	E8 or E9 (902)	4000-5777 \
30	E8 or E9 (902)	4000-5777 /
29	E8 or E9 (902)	6000-7777 \
28	E8 or E9 (902)	6000-7777 /

TABLE 2-17: 50 SERIES MEMORY SIZE CONFIGURATIONS - 7.0 MB

SLOT NO.	TYPE	PPN
35	E7	0000-0777 \
34	E7	0000-0777 /
33	E8 or E9 (902)	2000-3777 \
32	E8 or E9 (902)	2000-3777 /
31	E8 or E9 (902)	4000-5777 \
30	E8 or E9 (902)	4000-5777 /
29	E8 or E9 (902)	6000-7777 \
28	E8 or E9 (902)	6000-7777 /

TABLE 2-18: 50 SERIES MEMORY SIZE CONFIGURATIONS - 8.0 MB

SLOT NO.	TYPE	PPN
35	E8 or E9 (902)	0000-1777 \
34	E8 or E9 (902)	0000-1777 /
33	E8 or E9 (902)	2000-3777 \
32	E8 or E9 (902)	2000-3777 /
31	E8 or E9 (902)	4000-5777 \
30	E8 or E9 (902)	4000-5777 /
29	E8 or E9 (902)	6000-7777 \
28	E8 or E9 (902)	6000-7777 /

4. According to Table 2-6, an E8 or E9 (1Mb) board in slot #35 responds to the same addresses as E6 boards in all eight slots. Therefore if an E8 or E9 (1Mb) board is placed in slot #35, E6 boards could not be resident in any of the remaining seven slots.

5. Generally boards of smaller memory size should be placed in the upper memory slots (lowest addresses). The most desirable configuration is for memory to be fully interleaved with no addressing holes if possible.

6. Memory must begin at address 000000 (top memory slot). Addressing must be contiguous (no holes) for the first .256 Mb. After that holes are permissable, but they should be minimized if possible.

7. Figure 2-15 shows the memory switch locations. Table 2-19 is a list of standard switch settings for E6, E7, E8, and E9 memory boards.

TABLE 2-19: E6, E7, E8 AND E9 MEMORY BOARD SWITCH SETTINGS

CPU TYPE	12128-E6	12256-E7 12512-E8	7615-902 (E9)
P150 P250 P350	INTERLEAVE 1,3,5 OFF	INTERLEAVE 1,3,5,OFF	INTERLEAVE 1,3,5,6,7,8 OFF
P400 P450 P650	NON-INTERLEAVE 1,3,5,6 OFF	NON-INTERLEAVE 1,3,5,6 OFF	NON-INTERLEAVE 1,3,5,6,7,8 OFF
P750 P850	INTERLEAVE &WIDE WORD 1 & 5 OFF	INTERLEAVE &WIDE WORD 1 & 5 OFF	INTERLEAVE &WIDE WORD 1,5,7,8 OFF

2.8.5 I/O CABLING GUIDELINES

Cabling instructions for non-bulkhead (non-FCC) and bulkhead (FCC) cabinets are presented in this subsection.

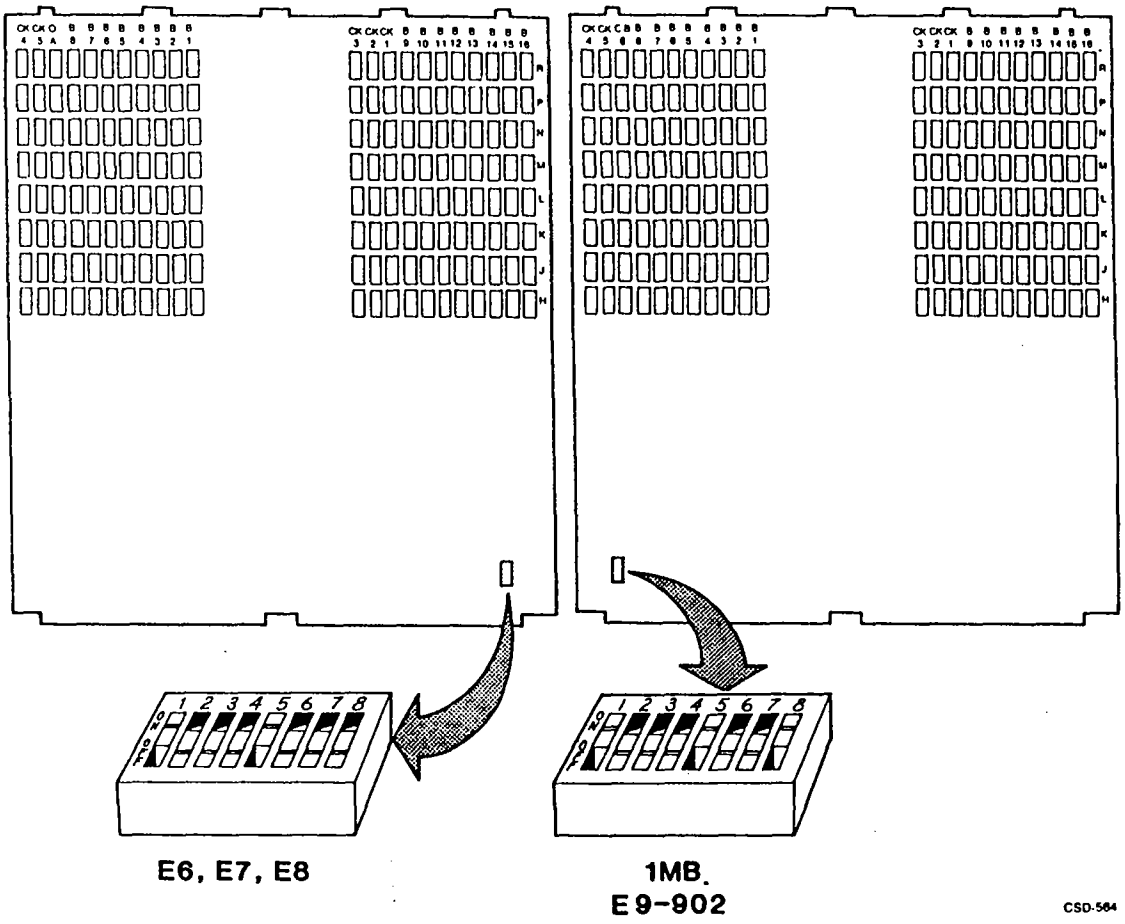


FIGURE 2-15: MEMORY BOARD SWITCHES

2.8.5.1 I/O Cabling Guidelines For Non-FCC Cabinets

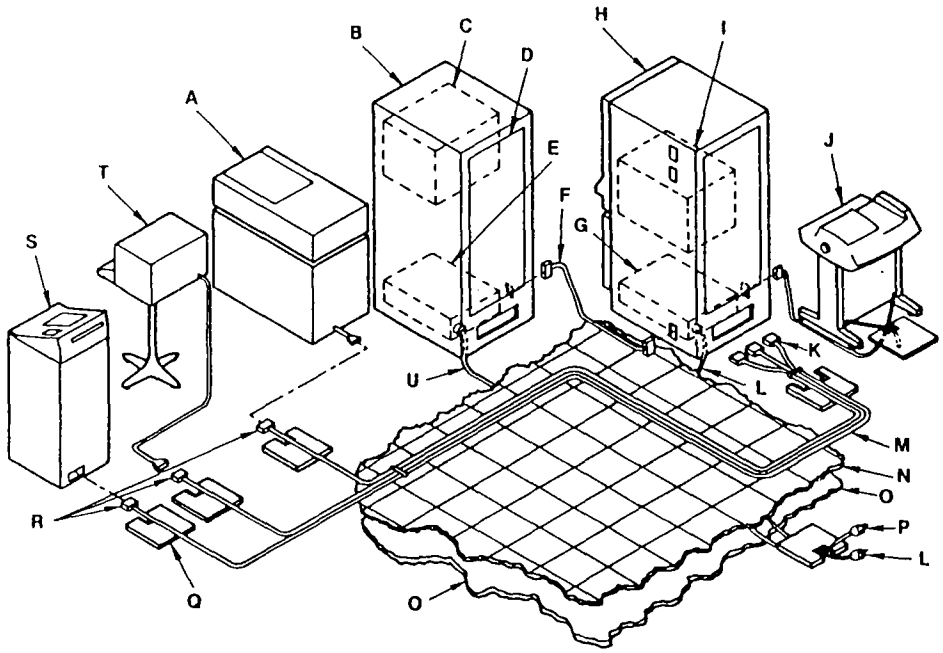
The following are basic non-bulkhead I/O cabling guidelines.

1. Reseat the circuit boards in the backplane before connecting any cables.

2. Remove the cable-access plate at the bottom rear of the mainframe cabinet. If the computer room has a raised floor, the cables may be brought up through the bottom of the cabinet, instead of through the cable-access plate (see Figure 2-16).

3. Run the receptacle-connector end of each cable into the mainframe cabinet through the access plate. Connect cables to the lowest boards in the cabinet first, then work up. This saves time adjusting cables as new ones are installed.

4. Mate the receptacle-connector end of each cable with its respective color-coded edge connector on the board in the backplane. Tighten the receptacle-connector screws on each mated connector (see Figure 2-17). If problems exist in identifying particular cables, connections, etc., consult the Service Manual that explains the particular installation of the device.



A — Disk Storage Module
B — Peripheral Cabinet
C — Magnetic Tape Transport
D — Cabinet's Rear Door
E — Peripheral Cabinet's PDU
F — Interconnection Cable for Tape Transport
G — Mainframe Cabinet's PDU
H — Mainframe Cabinet
I — Mainframe Chassis
J — Terminet #30
K — Receptacle-Ends of Interconnection Cables
L — Power Cord and Four-Wire Twistlock Plug for Mainframe Cabinet
M — Harnessed Cables-Layed-Out
N — Raised Floor
O — Structural Floor
P — Three-Wire Twistlock Plug
Q — Floor-Section with Cutout
R — Plug-end of Cables
S — Printer/Plotter
T — User Terminal
U — Power Cord for Peripheral Cabinet

Note:
Mainframe and peripheral cabinets normally installed at abutting locations.

CSD-565

FIGURE 2-16: TYPICAL LAYOUT OF CABLES AND EQUIPMENT

5. Mark the line number connections on all cables that are not marked by color-code. For example, AMLC cables 1469/1470 may be connected to any one of the four AMLC edge connectors. Each connector runs 4 of the possible 16 lines on an AMLC. The cable receptacle-connector ends must be marked with the 4 line numbers (0-3, 4-7, 8-11, or 12-15) connected to the cable.

6. Verify that all connector screws are tightened.

7. Using cable ties, dress the cables in the mainframe cabinet so they will offer minimum interference when removing boards for service.

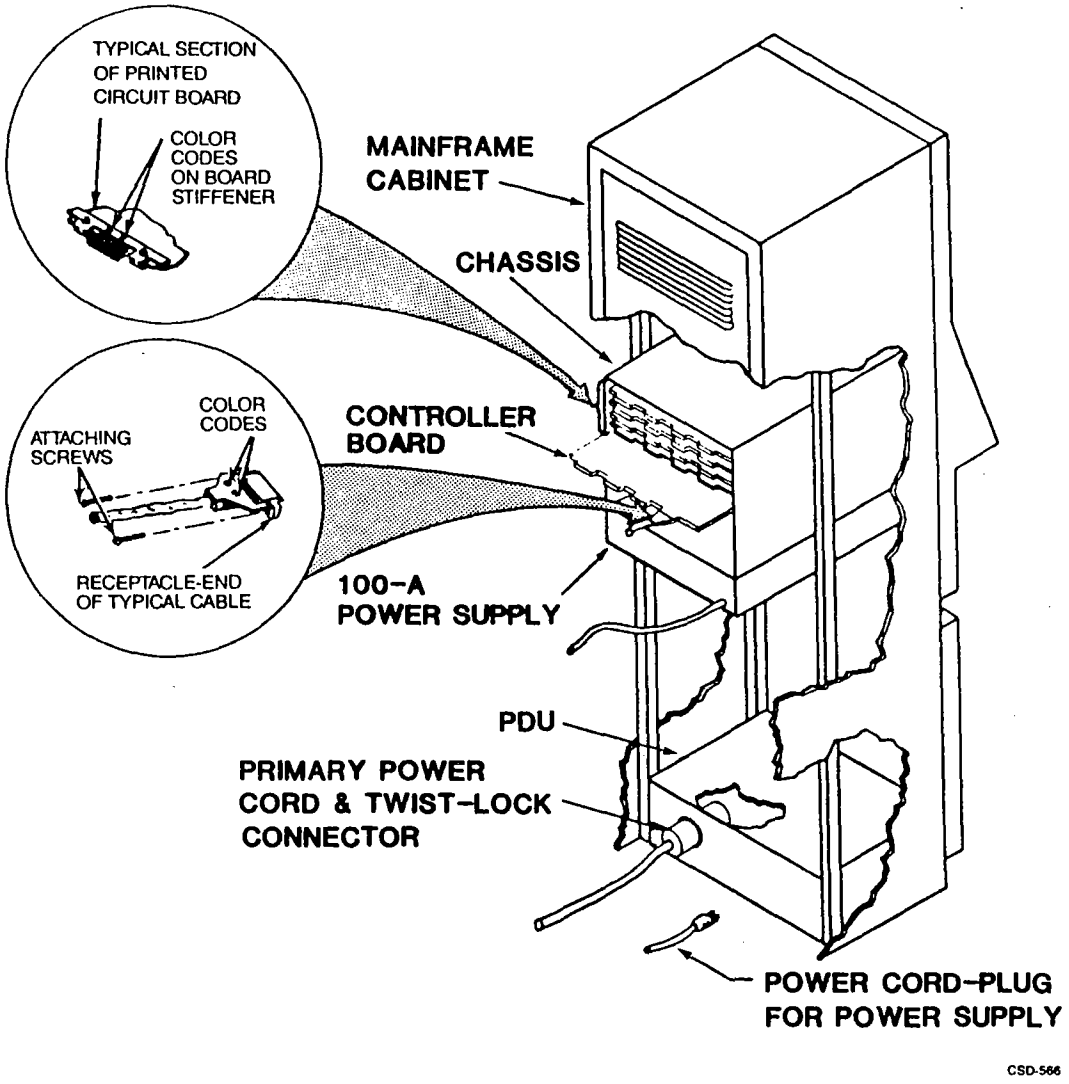


FIGURE 2-17: TYPICAL CABLE CONNECTIONS AT MAINFRAME CABINET

2.8.5.2 I/O Cabling For FCC Cabinets

The following are basic bulkhead I/O cabling guidelines.

1. Reseat the circuit boards in the backplane before connecting any cables.

2. Mate the receptacle-connector end of each cable with its respective color-coded edge connector on the board in the backplane. Tighten the receptacle-connector screws on each mated connector.

3. Connect cables to the lowest board in the cabinet first, then work up. This saves time adjusting cables as new ones are installed.

4. Mate the bulkhead connector end of each cable with the appropriate opening in the bulkhead (Figure 2-18) and tighten the screws on each mated connector.

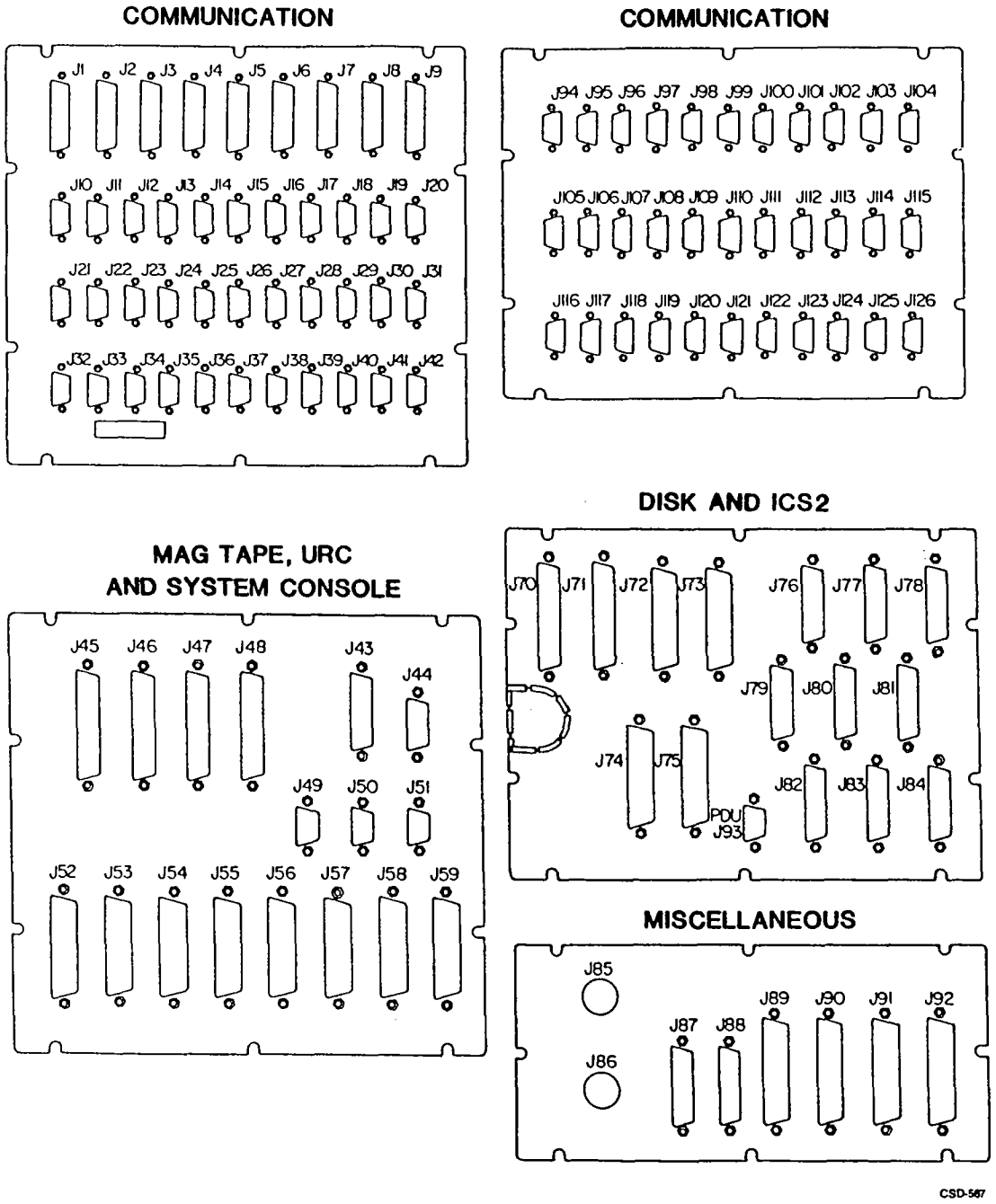


FIGURE 2-18: BULKHEAD PANELS

5. Mark the line number connections on all cables that are not marked by color-code. For example, AMLC cable 6126 may be connected to any one of the four AMLC edge connectors. Each connector runs four of the possible sixteen lines on an AMLC. The cable receptacle-connector ends must be marked with the four line numbers (0-3, 4-7, 8-11, or 12-15) connected to the cable.

6. For all external cabling, run the bulkhead-connector end of each cable to the rear of the cabinet to the bulkhead.

7. Verify that all connector screws or slide-locks are tightened.

8. Using cable ties, dress the cables in the cabinet so they will offer minimum interference when removing boards for service.

9. All internal cables have a female connector at the bulkhead port. All external cables other than extender/adapter cables, use male connectors at both ends.

10. All extender/adapter cables use female connectors at both ends.

11. All right angle connectors are secured to the bulkhead by screws and slide-locks. These connectors have more than 25 pins.

12. The 9-pin and 25-pin connectors are each secured by two standard screws and flat washers.

Among communications devices, all asynchronous devices have priority over synchronous communications devices. Priority for I/O controllers is presented in Table 2-20. If you have any further questions concerning priority, contact a system analyst.

TABLE 2-20: 50 SERIES PRIORITY: BASIC ORDER

PRIORITY	I/O CONTROLLER
Lowest	Synchronous
•	Asynchronous
•	Disk #1
Highest	Tape *

* All tape controllers have a higher priority than disk controllers. In multiple tape controller systems, the Integrated Formatter has highest priority (lowest in chassis) over all other tape controllers.

Table 2-21 provides a summary of 50 Series non-bulkhead cables, Table 2-22 provides a summary of 50 Series bulkhead cables and Table 2-23 lists any special cables to be used with standard system bulkhead cables.

TABLE 2-21: SUMMARY OF 50 SERIES NON-BULKHEAD CABLES

DEVICE CONTROLLER	CABLE NUMBER	LENGTH FT(M)	EDGE CONNECTOR
SYSTEM OPTION CONTROLLER (SOC)			
System Terminal			
ASR & KSR	1430-001	25(7.5)	D
	1453-001	15(4.5)	
Terminet 30 & CRT's	1449-002	30(9.0)	C
Paper Tape (3003,3032,SPL1407)			
Paper Tape Reader	0565-002	10(3.0)	F
Paper Tape Reader/Punch	1434-002	10(3.0)	F
Paper Tape (3006,3007,3009)			
Paper Tape Reader	1451-101	10(3.0)	F
Paper Tape Reader/Punch	1431-001	10(3.0)	E
	1451-001	10(3.0)	F
Serial Printer (Mates with CBL1449-002 for System Term)			
Tally or Centronics	2932-901		
Printer Plotter (3009)	2320-901		E & F
UNIT RECORD DEVICES			
Line Printer to Controller	1454-001	40(12.0	C
Card Reader to Controller(all)	1323-001	15(4.5)	D
Card Reader/Punch to Controller (LC50)	1496-001	20(6.0)	D & E
CARTRIDGE DISK DEVICES			
Pertec to Controller (1st device)	0578-002	15(4.5)	C & D
Pertec to Pertec Daisy Chain (expansion)	1296-903	10(3.0)	
Diablo to Controller (1st device)	1486-901		C & D
Diablo to Diablo Daisy Chain (expansion)	1491-901		
Diablo to Pertec Daisy Chain (expansion)	2891-901		
CDC 60 Mbyte to controller	1999-001	15(4.5)	C,D & F
CDC 60 Mbyte to 60 Mbyte Daisy Chain	2289-901	7(2.1)	
CDC 60 Mbyte and Pertec to Controller	1447-001	35(10.5)	C,D & F

TABLE 2-21: SUMMARY OF 50 SERIES NON-BULKHEAD CABLES (Cont.)

DEVICE CONTROLLER	CABLE NUMBER	LENGTH FT(M)	EDGE CONNECTOR
DISKETTE DEVICES			
AC from Power Supply	1437-001	3(0.9)	
DC from Power Supply	1438-001	3(0.9)	
Controller to 1st two drives	1499-002	15(4.5)	E
Controller to 4 drives	1499-003	18(5.4)	E
STORAGE MODULE DEVICES			
Controller to 1st device (control)	1475-901	10(3.0)	D & E
Controller to 1st device(data)	1479-901	10(3.0)	C
Device to device (daisy chain)	1481-901	10(3.0)	
FMD AND CMD DISK DEVICES			
Controller to 1st device (control)	3715-901	6(1.8)	E
Controller to 1st device(data)	3714-901	6(1.8)	C
Device to device (daisy chain)	3713-901	20(6.0)	
MAGNETIC TAPE DRIVES			
Pertec, NRZI Drives (1 drive)	1468-101		C, D & E
Pertec, NRZI Drives (2 drives)	1468-201		C, D & E
Pertec, NRZI Drives (3 drives)	1468-301		C, D & E
Pertec, NRZI Drives (4 drives)	1468-401		C, D & E
PERTEC AND KENNEDY PE DRIVES			
Controller to Pertec formatter	1401-001		C, D & E
Pertec formatter to 1st drive	PER 102201		
Pertec MTA to MTA (2 drives)	2493-001		
Pertec MTA to MTA (3,4 drives)	1489-001		
Controller to Kennedy formatter	3126-901		C, D & E
Kennedy formatter to 1st drive	3128-903		
Kennedy to Pertec daisy chain (adaptor)	MTT3199-001		
PERTEC AND KENNEDY PE/NRZI DRIVES			
Controller to formatter	ESA3872-901		D
FRMT to MTA	3893-902		C
DDFMPC to MTA	3893-904		C

TABLE 2-21: SUMMARY OF 50 SERIES NON-BULKHEAD CABLES (Cont.)

DEVICE CONTROLLER	CABLE NUMBER	LENGTH FT(M)	EDGE CONNECTOR
TELEX DRIVE			
Controller to formatter	3390-901		C I/O 1
	3390-902		D I/O 2
Formatter to 1st drive	TLX91C22378-25		
ASYNCHRONOUS COMMUNICATIONS			
AMLC with full data set control to data set	1258-001	30(9.0)	
AMLC with limited data set control to data set	1469-001		
AMLC with limited data set control to user terminal	1470-001	30(9.0)	
Adaptor	1456-001	6(1.8)	
SYNCHRONOUS COMMUNICATIONS			
SMLC to 201,208 data sets	1472-001	30(9.0)	
SMLC to 203,209 data sets	1471-001	30(9.0)	
HSSMLC to 303 data sets	2279-901	30(9.0)	
HSSMLC to DSU data sets	2278-901	30(9.0)	
MULTIPLE AUTOCALL INTERFACE			
Cable to 801 ACU	1459-001	30(9.0)	
PRIMENET NODE CONTROLLER			
Controller to Relay Box	3265-901		C
Relay Box to Relay Box	3288-901	10(3.0)	
	3532-901	10(3.0)	
	3533-901	50(15.0)	
	3534-901	200(60.0)	
	3535-901	500(150)	

* Cables marked with an asterisk are recommended for stocking.

TABLE 2-22: SUMMARY OF 50 SERIES BULKHEAD CABLES

CABLE#	NAME	TYPE OF CONNECTORS		USED WITH
		PRODUCT	BLKHD SIDE	
3533	Data Network J-Box to Bulkhead	NA	NA	PNC Junction Box
6113	50-Pin Edge Card to Bulkhead	50-Pin	50-Pin	Streaming and Magnetic Tapes Controllers
6117	MDLC Synchronous Port to Bulkhead	44-Pin	25-Pin (2)	MDLC
6125	Synchronous Port to Bulkhead	44-Pin Edge	25-Pin	ICS1
6126	Asynchronous Ports to Bulkhead IMCS	44-Pin Edge	9-Pin (4)	ICS1 and AMLC
6267	Dual Buffer Controller 64 lines	50-Pin	50-Pin	ICS2
6268	Single Buffer Controller 32 lines	50-Pin	50-Pin	ICS2
6358	26 POS Socket to 25-Pin D, IDC	26-Pin	25-Pin	Disk Controller
6361	60 POS EC with 1/2 E to 62 POS D	60-Pin Edge	62-Pin Edge	Disk Controller (Connector E only)
6363	60 POS EC FE to 62 POS D	60-Pin Edge	62-Pin	GRC Controller
6364	44 POS EC to 50 POS D	44-Pin Edge	50-Pin Edge	URC
6473	44 POS EC to 50 POS D	44-Pin Edge	50-Pin D	URC
6736	PDU to Bulkhead	4-Pin	9-Pin	PDU

TABLE 2-23: 50 SERIES SPECIAL BULKHEADING CABLES

CABLE	FUNCTION
CBL6366-001	Used to convert any 25-pin male D cable end to a 25-pin female D cable end with 4-40 screws at final hookup end.
CBL6366-002	Used to convert any 25-pin male D cable end to a 25-pin female D cable end with 3mm screws at final hookup end.

TABLE 2-23: 50 SERIES SPECIAL BULKHEAD CABLES (Cont.)

CABLE	FUNCTION
CBL6366-003	Used to convert any 25-pin male D cable end to a 25-pin male D device cable. 4-40 standoff at both ends.
CBL6596-XXX	Used for the following conversions: • CBL6596-XXX + CBL6109 (asynchronous modems only)= CBL6124-XX (asynchronous devices and terminals). • To drive the PST100 terminal, add CBL6596-XXX to CBL1470-XXX.
CBL7515-001	Used to support one line of a 20 mA current loop interface to bulkhead port. 9-pin D male.
CBL7508-001	Used to adapt existing 44-position edge card (communication) cables to bulkhead ports in support of the AMLC and ICS2 controllers.

2.8.6 1045/1051 POWER SUPPLY INSTALLATION VERIFICATION

Verify that the 1045/1051 power supply shown in Figure 2-19 is installed in the system cabinet. Reseat the power supplies using the ejector arms.

CAUTION

Failure to verify proper installation of the power supplies could result in serious damage to the system.

Cable the power supply to the PDU as outlined under the PDU Cabling Procedure in this chapter.

2.8.7 UNINTERRUPTIBLE POWER SUPPLY INSTALLATION

The Uninterruptible Power Supply (UPS) maintains ac power if main power is shut off. Normally, the supply only maintains power to the mainframe.

Presently, Prime does not install or support the UPS. However, Prime recommends the UPS as an alternative to poor electrical power. Prime's hardware and software have been configured to support the UPS. The customer must arrange for purchase, installation and maintenance support of a UPS.

2.8.8 POWER DISTRIBUTION UNIT (PDU) CABLING

Instructions for cabling PDUs in non-FCC and FCC cabinets are presented in the following subsections.

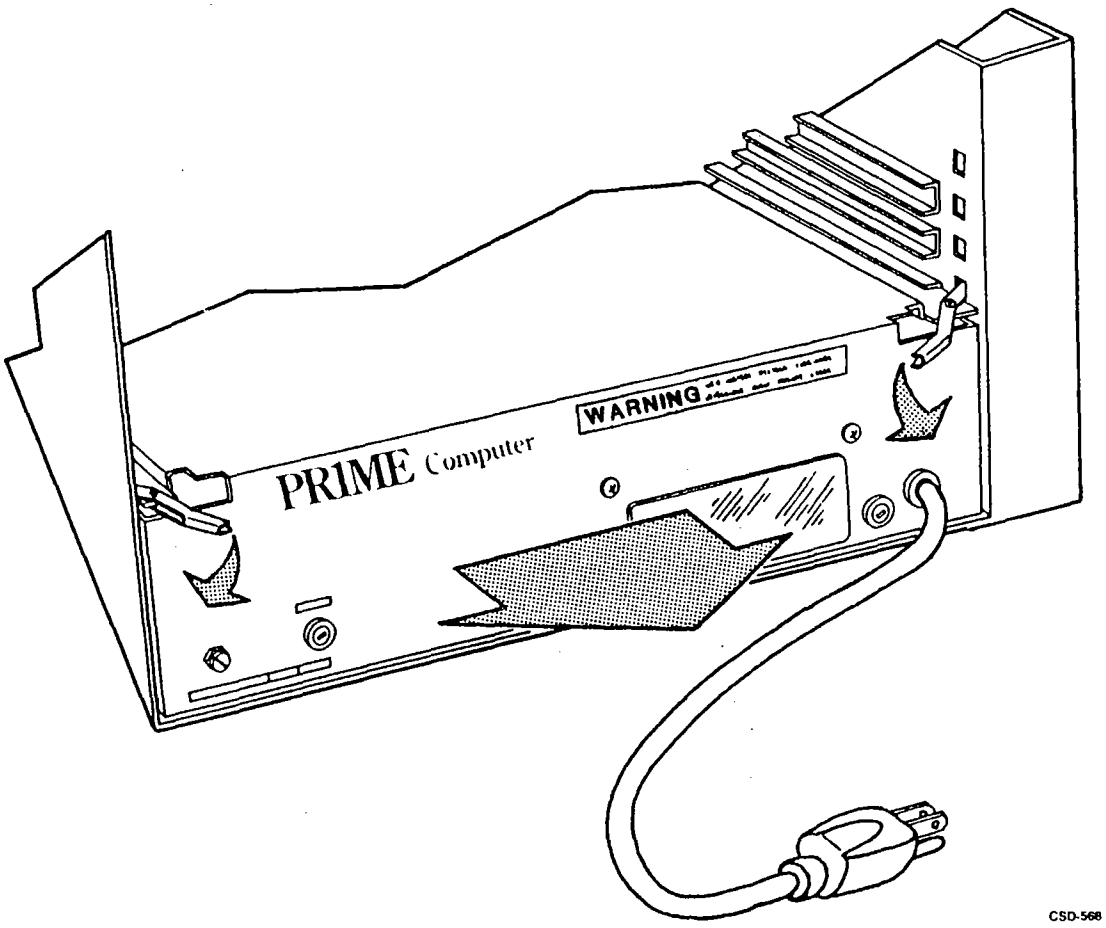


FIGURE 2-19: POWER SUPPLY INSTALLATION

2.8.8.1 Non-FCC Cabinet PDU Cabling

PDU cabling instructions are presented for the following:

- Mainframe Cabinet (Domestic)
- Peripheral Cabinet (Domestic)
- Mainframe and Peripheral (International) cabinets
- Free-Standing Peripherals
- PDU Interconnections

2.8.8.1.1 Mainbay Cabinet (Domestic)

Mainbay PDUs (all but 750 systems) are equipped with three switched power receptacles and one unswitched receptacle; the 750 PDU is equipped with four switched power receptacles (see Figures 2-20 and 2-21). The switched receptacles normally service the CPU, memory, and I/O power supplies; the unswitched receptacle services the power supply of a mainbay cabinet-mounted peripheral (older systems). The POWER button on the VCP status panel can be used to control power to all switched receptacles on PDUs in a multicabinet configuration. The

CPU power supply should be connected to the right-most switched outlet, so it will be the last cabinet powered up.

When all cables have been installed, verify that there is no peripheral or power supply plugged into the mainbay cabinet PDU.

CAUTION

DAMAGE to equipment could occur if the PDU is plugged into an untested ac power source.

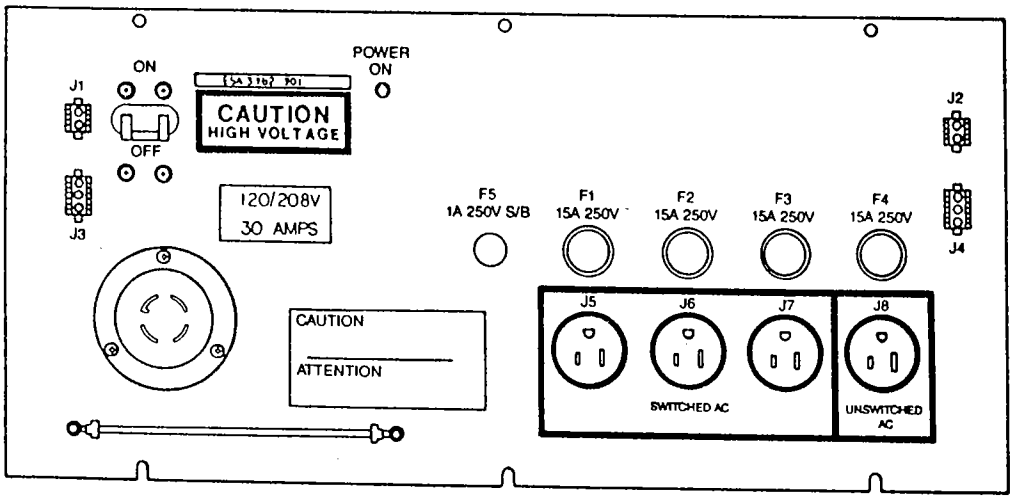


FIGURE 2-20: MAINFRAME PDU DOMESTIC

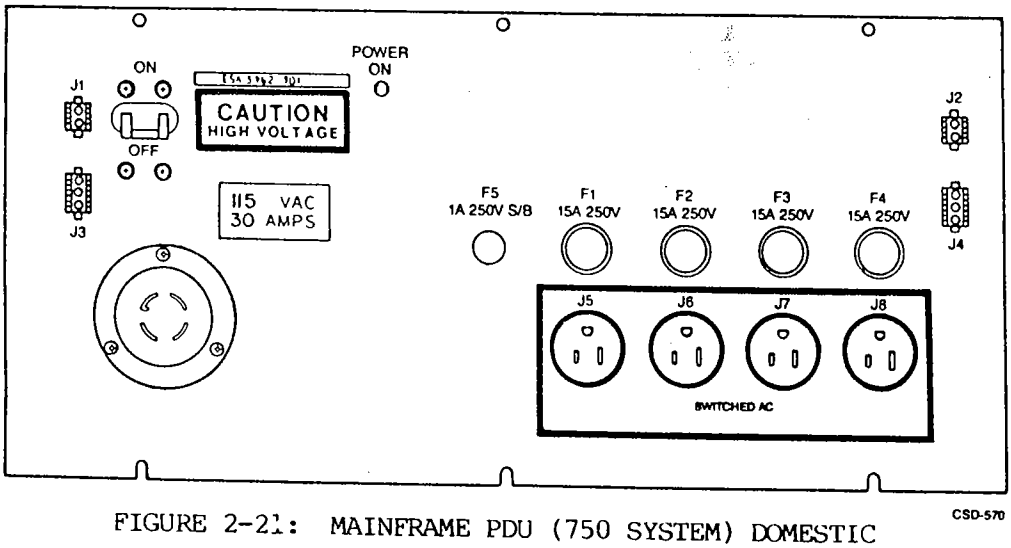


FIGURE 2-21: MAINFRAME PDU (750 SYSTEM) DOMESTIC

To cable a domestic PDU in a Non FCC Mainbay cabinet proceed as follows:

1. Run the power cord from the cabinet PDU to the ac power source receptacle. The power cord is the four-wire cord with the twistlock (2713) connector.

2. Verify that the PDU ac circuit breaker is set in the off position.

3. Plug the power cord into the PDU. Plug the cord into the power source receptacle.

4. Set the circuit breaker to on and verify that the cabinet blowers function normally. Verify that ac power is wired properly, using a 3-wire circuit analyzer plugged into an unswitched ac receptacle.

5. Press the power button on the VCP status panel. Using the ac circuit analyzer, verify that power is good from the switched receptacles.

6. Press the power button off and turn the PDU ac circuit breaker to off.

7. Plug in all power supplies to the switched ac receptacles in the PDU.

CAUTION

Do not plug in any more than one power supply per switched ac duplex and do not plug in any device along with the power supply on the same duplex.

2.8.8.1.2 Peripheral Cabinet (Domestic)

Peripheral cabinets are equipped with one switched receptacle and three unswitched receptacles (see Figure 2-22). The procedure for mainbay cabinets (Domestic) also applies to domestic peripheral cabinets, with the following exceptions:

1. The PDU uses three-wire service not four-wire.

2. Peripherals should be plugged into unswitched ac if they will be run with mainbay power turned off. Otherwise, plug peripherals into switched ac duplexes.

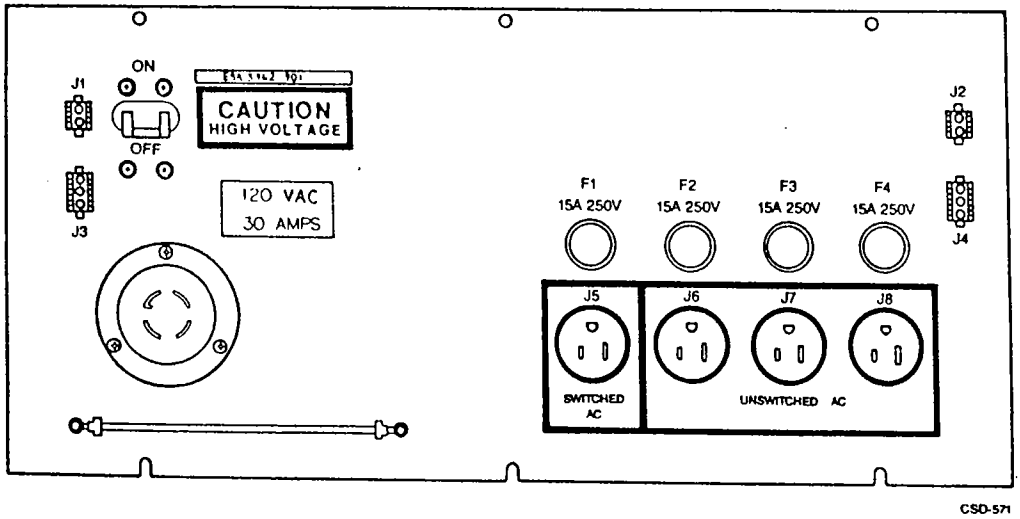


FIGURE 2-22: PERIPHERAL PDU DOMESTIC

2.8.8.1.3 Mainbay and Peripheral Cabinets (International)

The procedure for domestic mainbay cabinets applies to the international cabinets (Figure 2-23), with the following exceptions:

1. The PDU is equipped with a 3-wire (230v, 50 Hz) service.

2. Only the twistlock 2613 receptacle (no power cord) is provided.

WARNING

A step-down (230/115) transformer is mounted and connected to the cabinet blower. If not connected properly the blower motor may be damaged. It is connected and checked out in the factory and should be of little concern when the system is installed. However, be aware of this transformer's presence!

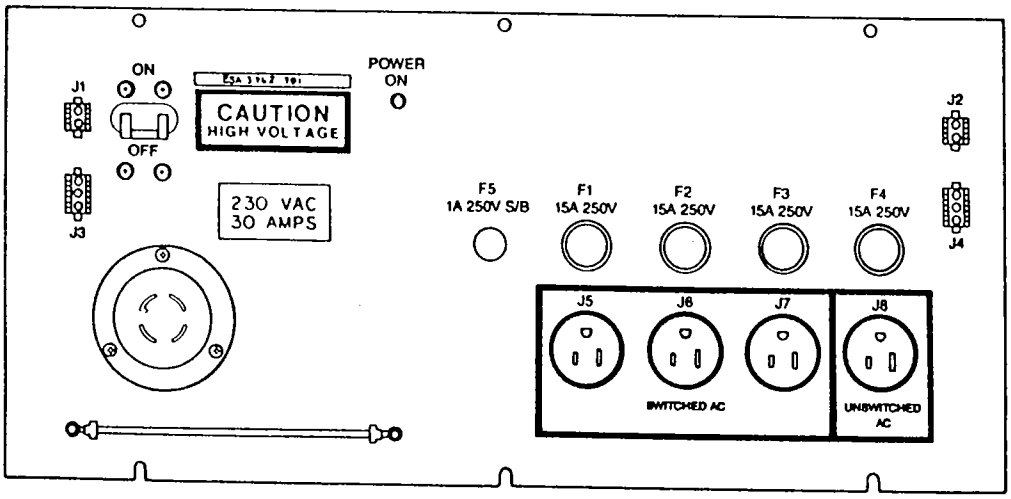


FIGURE 2-23: MAINFRAME/PERIPHERAL PDU INTERNATIONAL

2.8.8.1.4 Free-Standing Peripherals

Connect all free-standing peripherals to their ac power source according to the procedures in the appropriate CS Service Manual.

2.8.8.1.5 PDU Interconnections

To install the single-cabinet and dual-cabinet PDU interconnections, refer to Figures 2-24, 2-25 and proceed.

1. Verify that the orange colored two-wire line from the VCP bezel is connected to J2 on the mainframe PDU.

2. Locate and install the two-wire (orange/white colored) lines with plastic mate-n-lock connectors. Connect one cabinet PDU J3 to another cabinet J4 until the mainframe CPU and all peripheral PDUs are daisy-chained together.

NOTE

The J4 receptacle is located on the right side of the peripheral cabinet's PDU; the J3 is located on the left side of the mainframe cabinet's PDU.

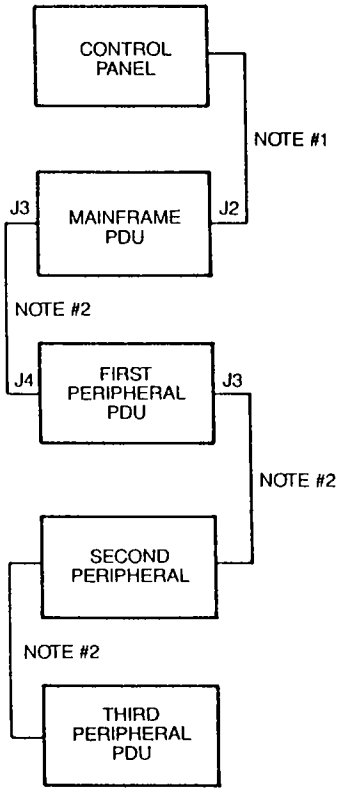


FIGURE 2-24: PDU TO PDU INTERCONNECTIONS SINGLE CABINET PROCESSOR

2.8.8.2 FCC Cabinet PDU Cabling

To properly cable the Power Distribution Unit (PDU) in an FCC cabinet follow the steps below.

1. Open the side and rear doors of the cabinet.

2. Locate the main power cable on the PDU. (Note that the PDU power cable has been inserted through a cable cover port, MEC6658-001.) Perform either step 3a or 3b depending on whether the facility has a raised or solid floor. Refer to Figure 2-26 for either procedure.

3a. RAISED FLOOR: Facing the side of the cabinet, locate the cable cover port (P/N MEC6085-001) on the bottom corner frame inside of the cabinet. This port is referenced as "A" in Figure 2-26. Remove and discard the port.

Also remove the smaller cable access panel, "B" in Figure 2-26, located to the immediate right of the cable cover port.

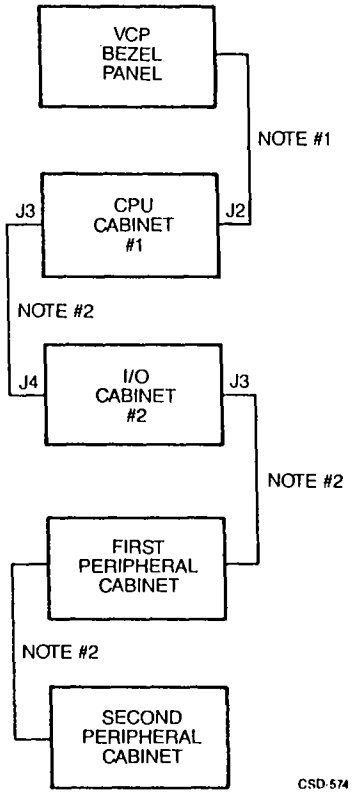


FIGURE 2-25: PDU TO PDU INTERCONNECTIONS DUAL CABINET PROCESSOR

3b. SOLID FLOOR: Locate the cable cover port (P/N MEC6085-001) on the inside corner frame of the cabinet. This port is referred to as "C" in Figure 2-26. Remove and discard the port. Also remove the smaller cable access panel, "D" in Figure 2-26, located to the immediate right of the cable cover port.

4. Slide the main power cable through the smaller cable access panel. Position the cable into the empty cover port trough.

5. Secure the cable cover port, MEC6658-001, into the empty trough.

6. Replace the smaller cable access panel.

7. Run the cable to the appropriate receptacle illustrated.

2.8.8.2.1 Power Supply Cables Installation

To properly install all cables for the power supplies into the PDU refer to Figure 2-27 and plug the power supplies into J2, J3, J5, J6 and J7. Make sure that the memory power supply is plugged into J7.

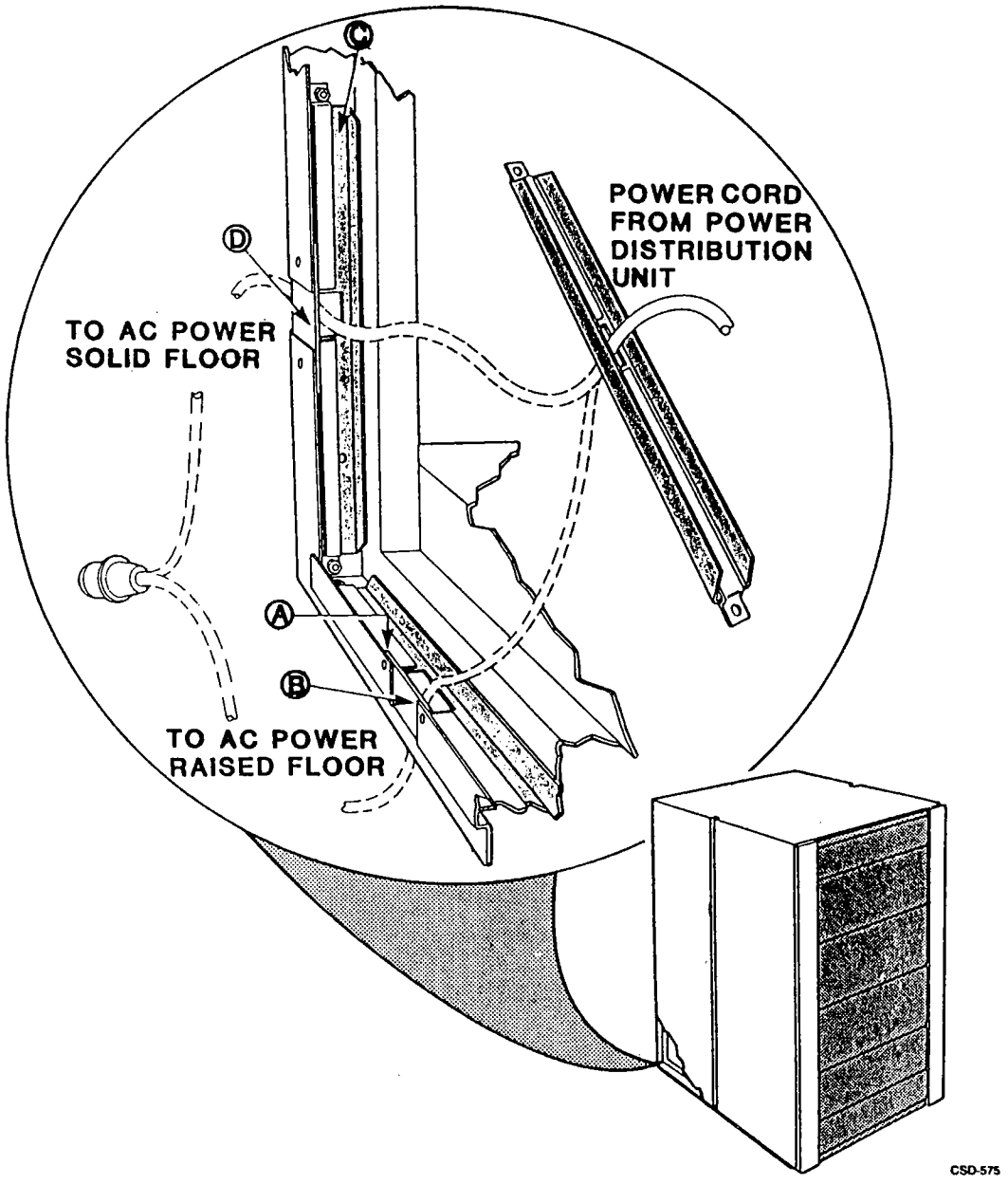


FIGURE 2-26: MAIN POWER CABINET INSTALLATION

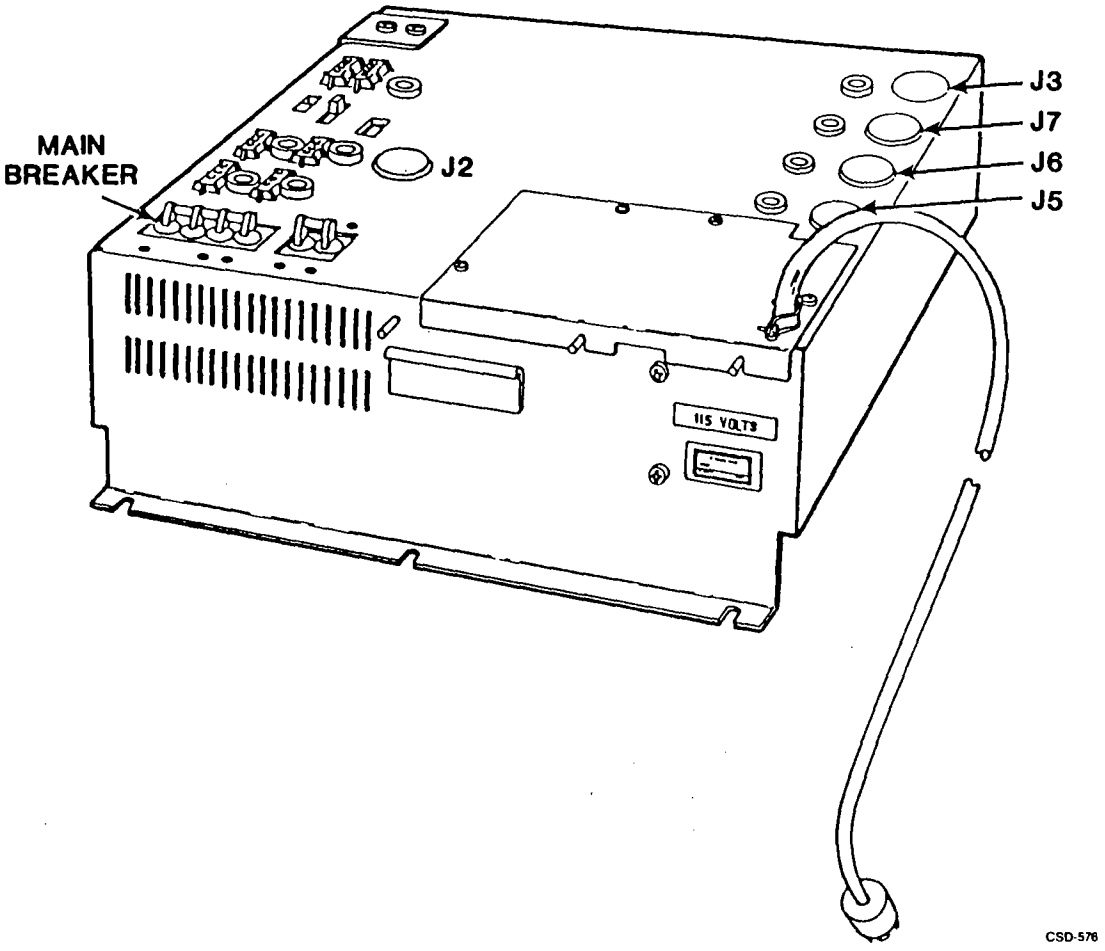


FIGURE 2-27: POWER SUPPLY OUTLETS

2.8.8.3 Blower Power Cables Installation

To properly install the blower cables, refer to Figure 2-12 and connect the system blower power cable into J8 of the PDU.

2.8.9 SYSTEM CONSOLE INSTALLATION

The VCP can support one local system console, one remote system console and one serial printer. If possible the printer should be connected to an AMLC line instead of the VCP, due to speed and overhead requirements.

Refer to Figure 2-28 and install the system console as follows:

1. Plug the VCP to bulkhead cable into connector CF of the VCP PCB.

2. Using a standard screwdriver attach the other ends of the cable to connectors J43, J49, J50 and J51 of the bulkhead.

3. Connect the system console cable to J50.

4. If there is a remote console, connect the console modem cable to J43.

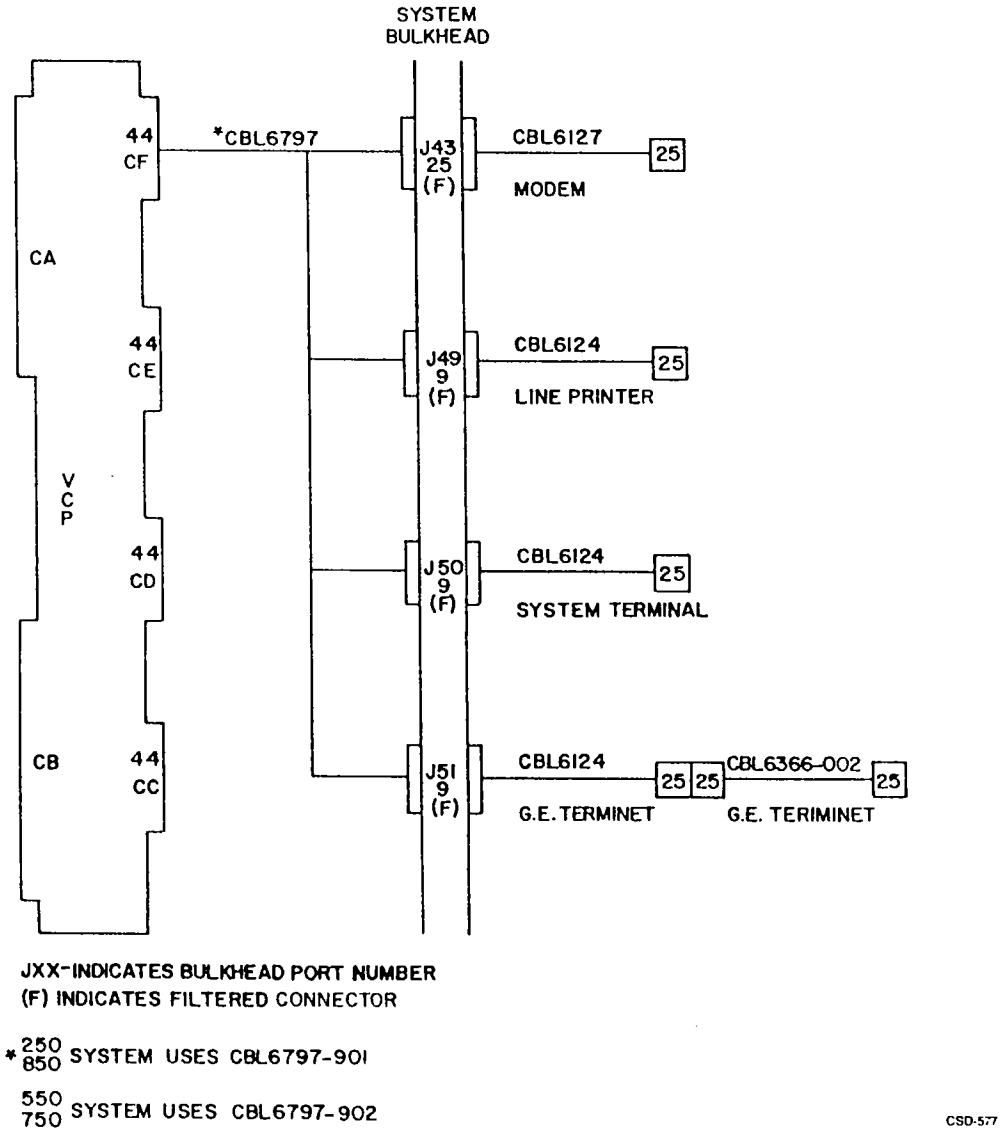


FIGURE 2-28: VCP CABLING

5. If there is a serial printer and there is no available AMLC line, connect it to J49.

2.8.10 SYSTEM CONFIGURATION

Board, jumper and cable configurations as well as address conversion instructions for the following 50 Series hardware and I/O options are provided in this subsection:

- Disk Controller
- Tape Controller Device Address Conversion
- GRC Magnetic Tape Controller
- Kennedy Model Magnetic Tape Configuration

- Streaming Tape Drive Controller
- Unit Record Controller
- System Option Controller
- Intelligent Communication Subsystem 1
- Intelligent Communication Subsystem 2
- Asynchronous Multi-Line Controller
- Synchronous Controller
- PRIMENET Node Controller
- Main Bay to Peripheral Bay Cabling
- Air Baffle

Table 2-24 summarizes all 50 Series applicable controller device addresses.

TABLE 2-24: CONTROLLER DEVICE ADDRESSES

DEVICE ADDRESS OCTAL	CONTROLLER MODEL	DESCRIPTION
00	----	-----
01	3000	Paper Tape Reader
02	3000	Paper Tape Punch
03	3100	URC #1 (Line Printer, Card Reader, Card Punch)
04	3000	System Terminal
05	3100	URC #2 (Line Printer, Card Reader, Card Punch)
06	7000	IPC (Interprocessor Communications Board)
07	7040	PRIMENET Node Controller #1
10	----	ICS2 #1 or ICS1 (Intelligent Communications Subsystem)
11	----	ICS2 #2 or ICS1
12	4300	Floppy Disk
13	2270	Magnetic Tape #2
	2301	" " "
	4020	" " "
14	2270	Magnetic Tape #1
	2301	" " "
	4020	" " "
15	5000	AMLC/QAMLC #5 or ICS1
16	5000	AMLC/QAMLC #6 or ICS1
17	5000	AMLC/QAMLC #7 or ICS1
20	3000	Control Panel, RTC (Real-time Clock)
21	4002	Disk Option B'
22	4004	Disk Controller #3
	4005	" "
23	4004	Disk Controller #4
	4005	" "

TABLE 2-24: CONTROLLER DEVICE ADDRESSES (Cont.)

DEVICE ADDRESS OCTAL	CONTROLLER MODEL	DESCRIPTION
24	2076	Writable Control Store
	2461	" " "
25	4000	Disk Option B
26	4004	Disk Controller #1
	4005	" "
27	4004	Disk Controller #2
	4005	" "
30	3007	Buffered Parallel I/O Channel #1
31	3025	Buffered Parallel I/O Channel #2
32	5000	AMLC/QAMLC #8 or ICS1
33	3009	VERSATEC Printer Plotter
	3008	GOULD Printer Plotter
34	3009	VERSATEC Printer Plotter
	3008	GOULD Printer Plotter
35	5000	AMLC/QAMLC #4 or ICS1
36	----	ICS1 #1
37	----	ICS1 #2
40	6000	PRIMAD (AIS, Analog Input System)
	6005	"
41	6020	Digital Input #1 (DIS)
42	6020	Digital Input #2
43	6040	Digital Output #1 (DOS)
44	6040	Digital Output #2
45	6060	Digital to Analog (Analog Output System)
46	6080	Computer Products Interface
47	7040	PRIMENET Node Controller #2
50	5300	HSSMLC #1 (High Speed Synchronous Multiline Controller) or MDLC (Multiple Data Link Controller)
51	5300	HSSMLC # or MDLC
52	5000	AMLC/QAMLC #3 or ICS1
53	5000	AMLC/QAMLC #2
54	5000	AMLC/QAMLC #1
55	5400	Multiple Autocall
56	5200	SMLC (Synchronous Multiline Controller)
57	----	----------
60	7000	General Purpose Interface Board
61	7000	General Purpose Interface Board
62	7000	General Purpose Interface Board
63	7000	General Purpose Interface Board
64	7000	General Purpose Interface Board
65	7000	General Purpose Interface Board
66	7000	General Purpose Interface Board
67	7000	General Purpose Interface Board
70	----	Reserved for Specials
71	----	Reserved for Specials
72	----	Reserved for Specials
73	----	Reserved for Specials
74	----	Reserved for Specials
75	----	Reserved for Controllers Using T$GPPI
76	----	Reserved for Controllers Using T$GPPI
77	----	I/O Bus Tester

2.8.10.1 Disk Controller Configuration and Cabling

Configuration instructions are provided for the 4004/4005 disk controller. Cabling instructions for the disk controllers are presented under the following categories:

- Rack-Mounted Devices
- Stand-Alone Devices
- Mixed Devices

2.8.10.1.1 Model 4005 Disk Controller Configuration

Each 4005 disk controller can support up to four disk drives. A maximum of two disk controllers and eight drives are supported per system. At Rev 19.3, PRIMOS™ can support four disk controllers and eight drives per system. Dual-port installation (two systems connected to the same drive) is described in the appropriate disk drive Service Manual.

A maximum of two disk controllers may be configured on each system. The first controller has a device address of '26 and the second controller has a device address of '27. Controllers shipped from the factory as spares or add-ons have an address of '26. Address conversion instructions follow.

Address Conversion: '26 to '27 - To change the device address from '26 to '27 use the steps below.

1. Remove signal DAD06 by turning the controller over so that the etch side faces up. Cut the etch run of signal DAD06- between IC 37C (7442) pin 7 and IC 35D (74S02) pin 5.

2. Add signal DAD07- from IC 37C pin 9 to IC 35D pin 5 by using 30 gauge wire. Solder the wire to the respective dip leads on the component side of the board.

3. Change the device selection PROM as outlined under Model 4004/4005 PROM Conversion procedures in this chapter.

Address Conversion: '27 to '26 - To change the controller device address from '27 to '26, use the following steps.

1. Remove the jumper wire at IC 37C from pin 9.

2. Solder the jumper wire to IC 37C pin 7.

3. Change the device selection PROM as outlined under Model 4004/4005 PROM Conversion procedures below.

2.8.10.1.2 Model 4004 Disk Controller Configuration

Each 4004 disk controller can support up to four disk drives. A maximum of two disk controllers and eight drives are supported per system. Dual port installation (two systems connected to the same drive) is described in the appropriate disk drive Service Manual.

A maximum of two disk controllers may be configured on each system. The first controller has a device address of '26 and the second controller has a device address of '27. Controllers shipped from the factory as spares or add-ons have an address of '26. Address conversion instructions follow.

To change the device address from '26 to '27 (Figure 2-29):

1. Cut the etch at IC 39B (7442) between the feed-through pad and pin 7.

2. Run a jumper from the feed-through pad to IC 39B pin 9.

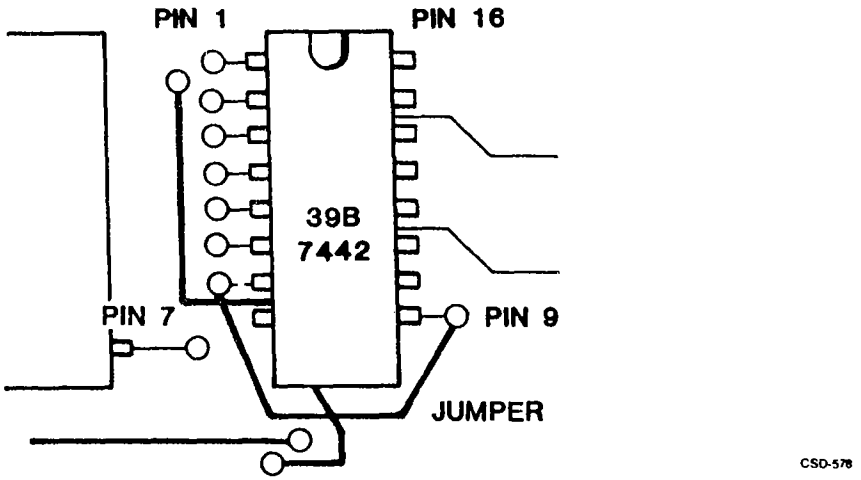


FIGURE 2-29: 4004 ADDRESS CONVERSION

To reconvert to address '26, reverse the procedure.

2.8.10.1.3 Model 4004/4005 PROM Conversion

When disk drives are added to a 4004/4005 controller, the device selection PROM must be changed. This PROM is located at 33M on etch version and 27M on wire wrap versions.

NOTE

This PROM is required for the controller to function properly. Customers must order the PROM when they order additional disk devices.

Refer to Table 2-25 to determine the proper PROM for a particular 4005 device configuration.

NOTE

Never install a PROM designed for more devices than are connected to the controller. For example, do not install PROM JC if only three devices are connected to the controller. Consult your manager before replacing this PROM.

TABLE 2-25: DEVICE CONFIGURATION PROMS

NUMBER OF DEVICES	PROM
1	JD
2	JE
3	JF
4	JC

2.8.10.1.4 Disk Controller Cabling

Proper cabling of rack-mounted, stand-alone and mixed-disk devices is shown in Figures 2-30 through 2-32 respectively.

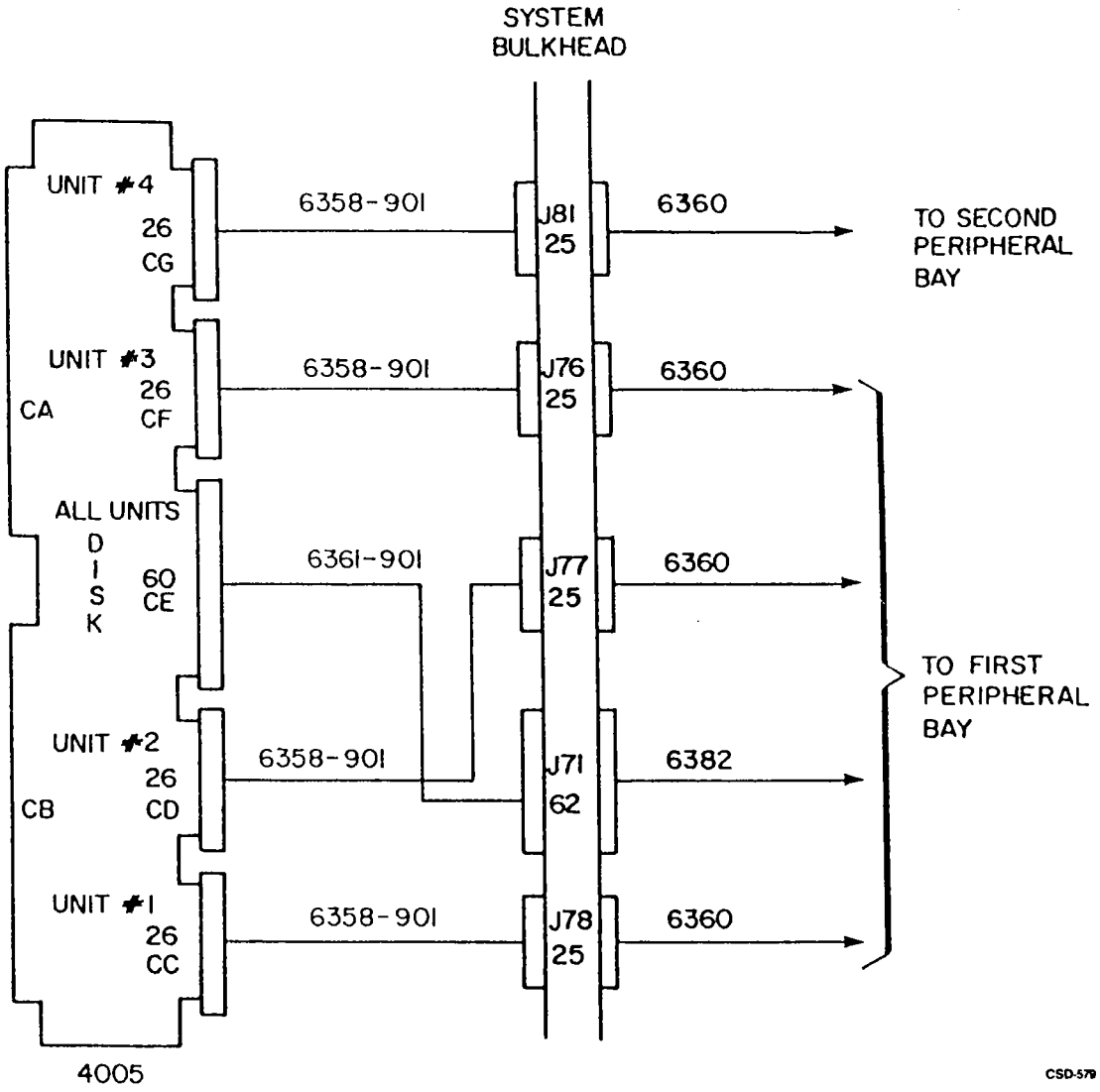


FIGURE 2-30: RACK-MOUNTED DISK BULKHEAD CABLING

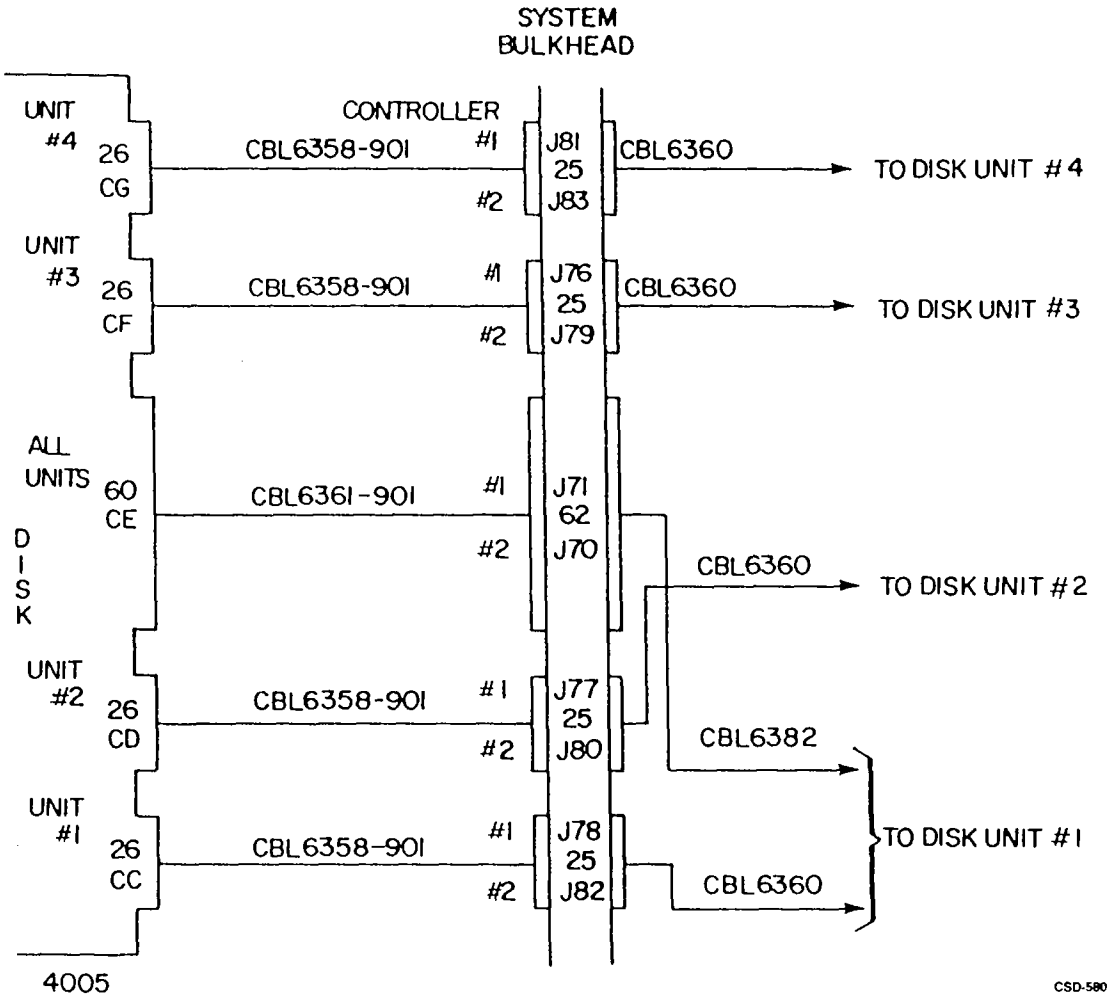


FIGURE 2-31: STAND-ALONE DISK BULKHEAD CABLING

2.8.10.2 Tape Controller Device Address Conversion

A maximum of two tape controllers may be configured on each system. The first controller has a device address of '14 and the second controller has a device address of '13. The standard address is '14.

To change the address to '13 on burst mode (2301) controllers:

1. Locate header dip 37C on the component side of the board.

2. Change the jumper from pin 5-16 to pin 4-16.

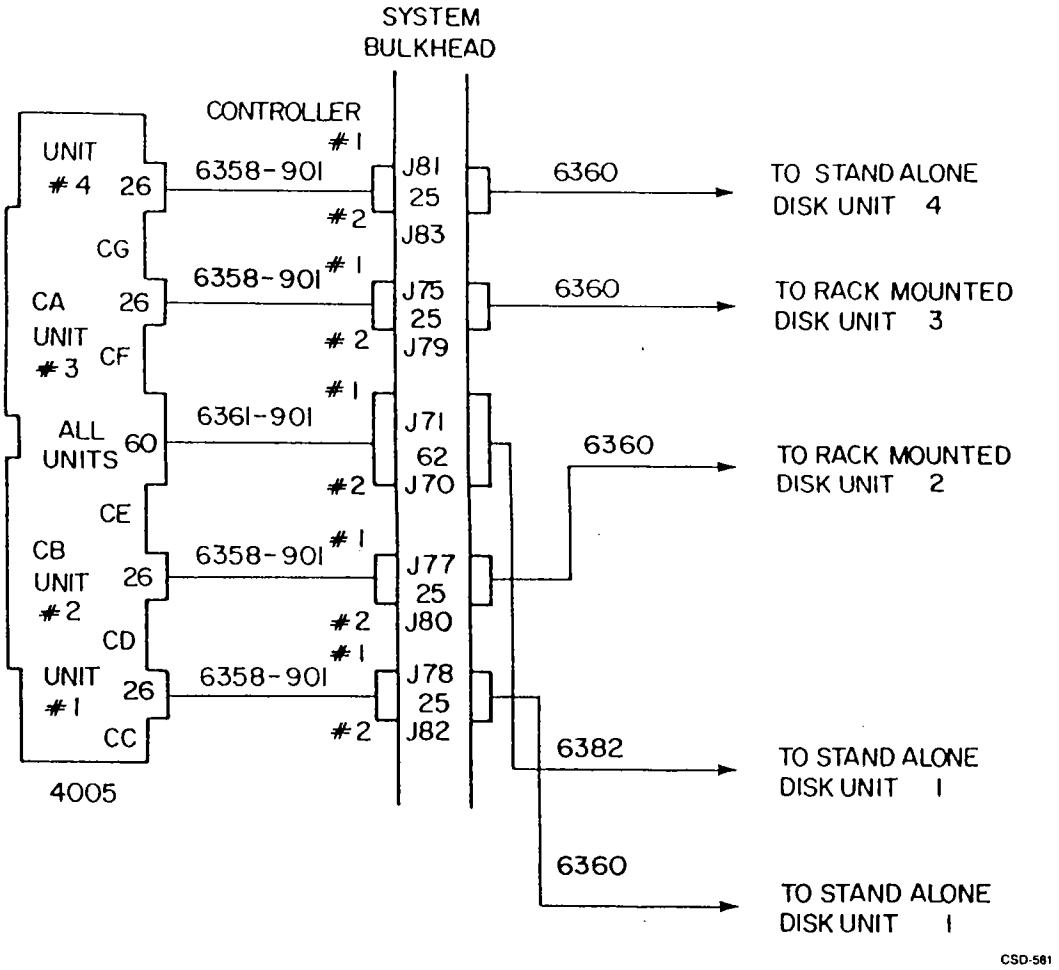


FIGURE 2-32: MIXED-DISK BULKHEAD CABLING

To change the address to '13 on nonburst mode (4020) controllers:

1. On the component side of the board locate the IC 37B.
2. Disconnect 37B output pin 05 (signal DAD04-) and connect it to 37B04 (DAD03-).

To change the address to '13 on nonburst mode (2270) controllers:

1. On the component side of the board locate the IC 39C.
2. Disconnect 39C output pin 05 (signal DAD04-) and connect it to 39C04 (DAD03-).

2.8.10.3 GCR Magnetic Tape Controller Configuration

Proper cabling for the Model 6250 GCR magnetic tape controller is shown in Figure 2-33.

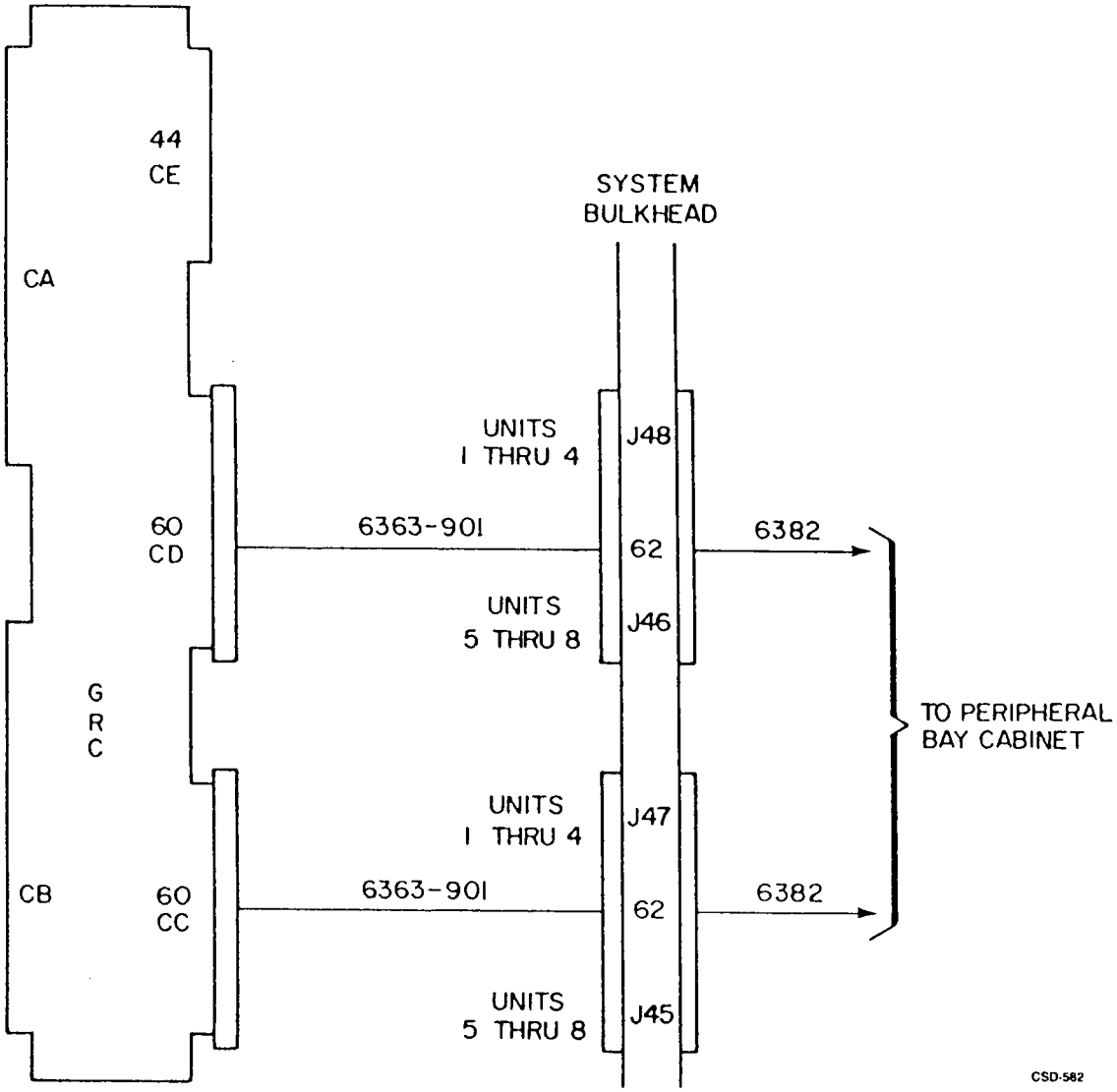


FIGURE 2-33: GRC BULKHEAD CABLING

2.8.10.4 Kennedy Model Magnetic Tape Configuration

Proper cabling for the Kennedy model magnetic tape controller is shown in Figure 2-34.

2.8.10.5 Streaming Tape Subsystem (STS) Controller Configuration

To properly cable the STS controller, refer to Figure 2-35.

2.8.10.6 Unit Record Controller (URC) Configuration

The maximum configuration per system is two URCs. Each URC supports up to three devices consisting of two line printers and one card reader. No more than two printers can be supported by each URC.

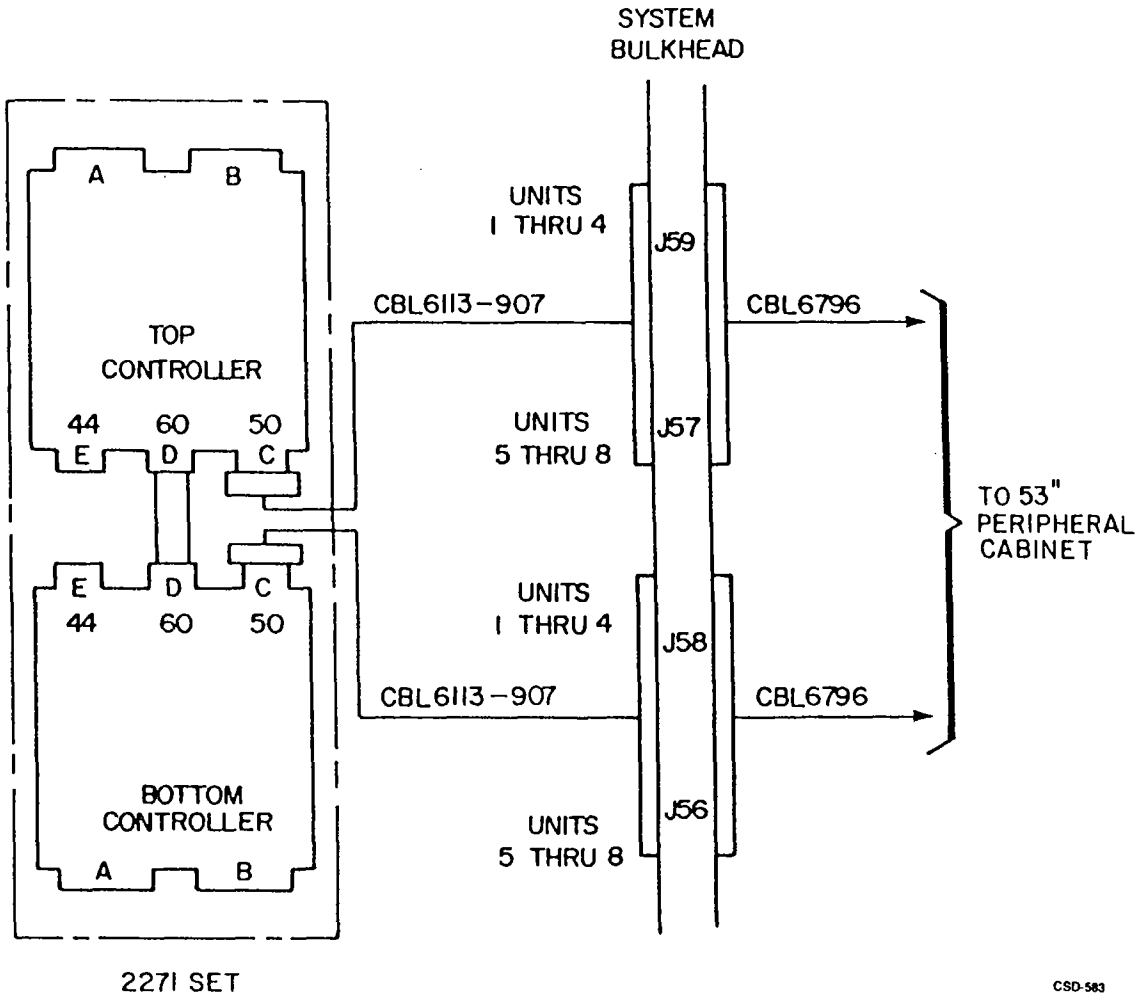


FIGURE 2-34: KENNEDY TAPE CONTROLLER BULKHEAD CABLING

The URC should be the topmost controller in the cabinet. As with all controller boards, there should be no more than three empty slots between the URC and the next controller. Address conversion and cabling information follows.

2.8.10.6.1 URC Address Conversion

The first URC controller has a device address of '03 and the second controller has a device address of '05. To convert the address from '03 to '05, move the jumper on pin #4 of 37B (7442) to pin #6.

2.8.10.6.2 URC Cabling

Table 2-26 shows the URC model numbers and the proper URC connector to use for each particular device. Figure 2-36 shows the proper URC to bulkhead cabling procedure.

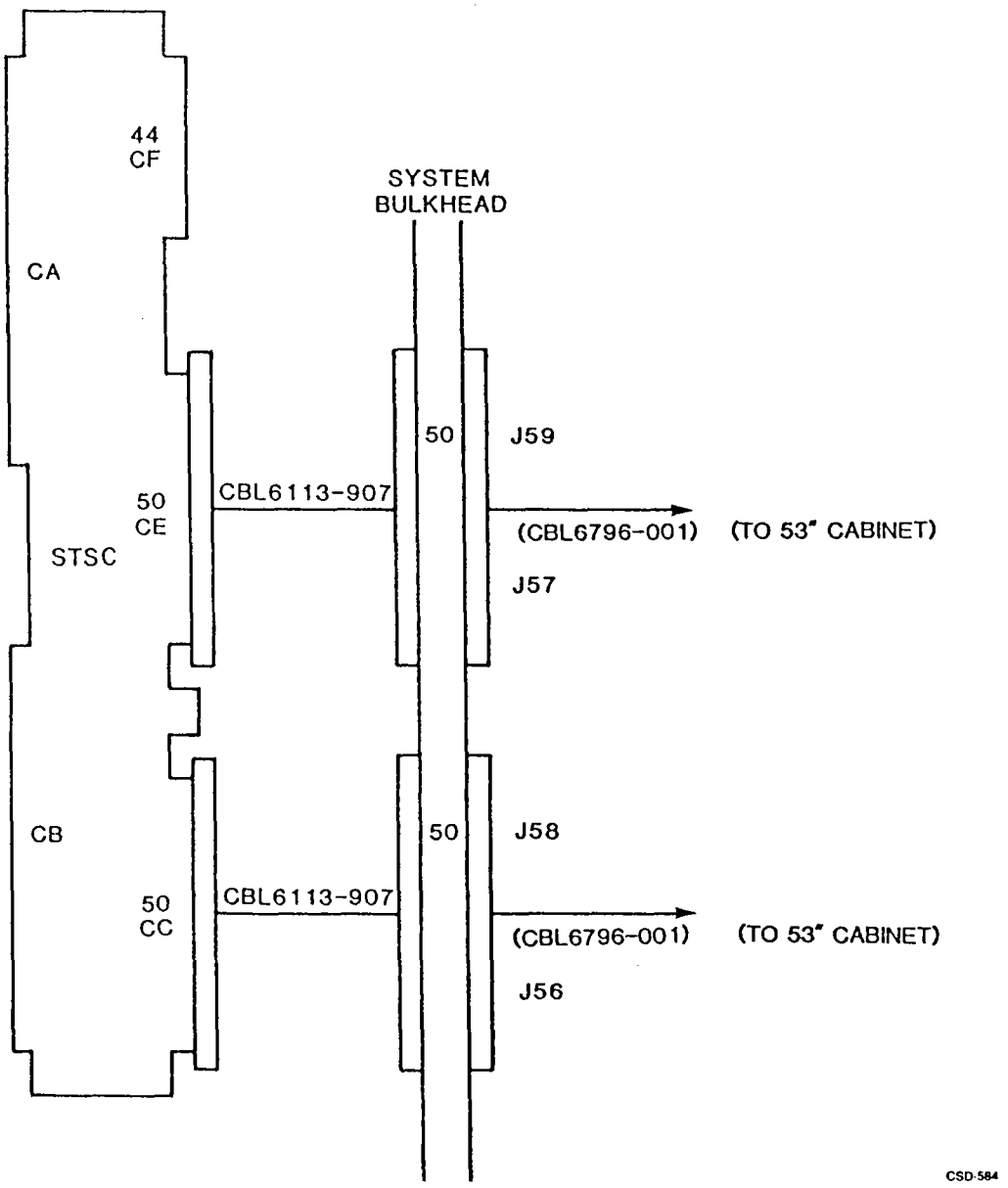


FIGURE 2-35: STREAMING MAGNETIC TAPE BULKHEAD CABLING

TABLE 2-26: URC CONFIGURATIONS

MODEL 3156	LPM	URC CONNECTOR FOR:		
		PRINTER #1	CARD READER	PRINTER #2
-901	≤ 600	C	D	E
-902	≤ 600	C	E	NA*
-903	> 600	C	D	E
-904	> 600	C	E	NA

*Not applicable.

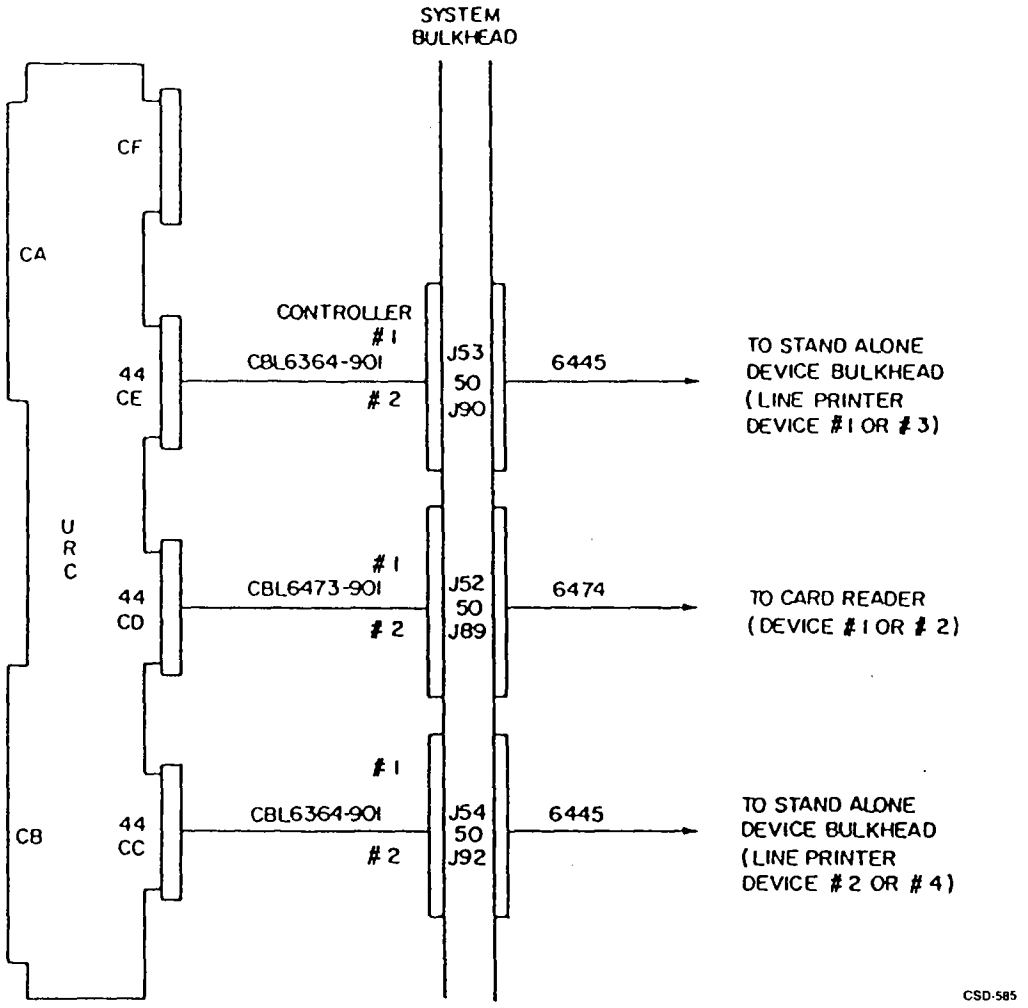


FIGURE 2-36: URC BULKHEAD CABLING

2.8.10.7 System Option Controller (SOC) Configuration and Address Conversion

The SOC controller is only used if the system includes an electrostatic printer/plotter (SOC model 3009) or a paper tape device (SOC model 3006). Each SOC can support only these devices and cannot be used with any other peripherals. SOC replacement and address conversion procedures are provided below.

When replacing a SOC, change the header dips on the replacement board to match the ones on the original board.

2.8.10.7.1 SOC General Address Conversion

When the SOC is installed in a system with a VCP, two addresses on the SOC board must be modified to allow the system to recognize the VCP as the interface for the system console. This is accomplished by changing the SOC device address '04 to '71 and the Real-Time Clock (RTC) address '20 to '70. Changing the RTC address disables the Real-Time Clock.

The SOC device address is controlled by pin 12 on header dips 35D and 37D. The RTC address is controlled by pin 15 on the same dips. The procedure to change the SOC address to '71 varies according to the type of controller being configured.

2.8.10.7.2 SOC Specific Address Conversion

Address conversion procedures are provided for the following controller configurations:

- Model 3009
- Model 3006 with paper tape reader
- Model 3006 with paper tape punch
- Model 3006 or 3007 with both paper tape reader and paper tape punch
- Two Model 3006

Model 3009 - The 3009 SOC supports a Versatec printer/plotter. The SOC's device and RTC address must be modified.

To change the 3009 SOC's device address to '71:

1. Connect jumper 35D pin 12 to 35D pin 09.

2. Connect jumper 37D pin 12 to 37D pin 02.

To change the RTC address to '70:

1. Connect jumper 35D pin 15 to 35D pin 09.

2. Connect jumper 37D pin 15 to 37D pin 01.

NOTE

Do not use existing jumper wires. Use new 24 gauge insulated wire and a heat sink applied to the header dip. Plug the header into an unused socket while soldering the jumpers in place.

Model 3006 with Paper Tape Reader - The paper tape reader is supported by a 3006 SOC. Change the SOC's device and RTC address as presented in Model 3009. Also change the paper tape device address from '30 to '33 using the following steps:

1. Connect jumper 35D pin 13 to 35D pin 04.

2. Connect jumper 37D pin 13 to 37D pin 04.

Model 3006 with Paper Tape Punch - The paper tape punch is also supported by a 3006 SOC. Change the device address as outlined for the 3009 controller. In addition, change the paper tape punch device address from '31 to '34:

1. Connect jumper 35D pin 14 to 35D pin 04.

2. Connect jumper 37D pin 14 to 37D pin 05.

Model 3006 or 3007 with Paper Tape Reader and Paper Tape Punch - A single 3006 or 3007 SOC may be used to support both the paper tape reader and paper tape punch. In this case, make all four address changes listed in the previous subsections.

Model 3006 (two boards) - If two SOC 3006 boards are used in a system with a VCP, several changes must be made. On the first SOC, change the SOC device address to '71. Then change the RTC address to '70. Change the paper tape reader's device address to '01 as follows:

1. Connect jumper 35D pin 13 to pin 01.

2. Connect jumper 37D pin 13 to pin 02.

Change the paper tape punch's device address to '02, by doing the following:

1. Connect jumper 35D pin 14 to pin 01.

2. Connect jumper 37D pin 14 to pin 03.

Address changes are also necessary on the second SOC board. Change the paper tape reader's device address to '33 and the paper tape punch's device address to '34, as explained previously. Then, change the SOC's device address to '73:

1. Connect jumper 35D pin 12 to pin 09.

2. Connect jumper 37D pin 12 to pin 04.

Also change the RTC device address to'72:

1. Connect jumper 35D pin 15 to pin 09.

2. Connect jumper 37D pin 15 to pin 03.

2.8.10.8 ICS1 Configuration

The ICS1 consists of a single synchronous line and eight asynchronous lines per controller board. A maximum of two boards can be configured per system.

2.8.10.8.1 ICS1 Address Conversion

A DIP header at location 37D is used to select the device address. Table 2-27 shows the ICS1 address list. ICS1 boards shipped from the factory as expansions, upgrades, or spares, are addressed as the first board in the system ('36). To select another address, the address jumpers must be moved as indicated in Table 2-28.

NOTE

The ICS1 device address is dependent on the number of ICS2s configured on the system.

TABLE 2-27: ICS1 ADDRESSES

ICS1 Number	No ICS2s	One ICS2	Two ICS2s
1	'36	'36	'36
2	'37	'37	'37
3	'10	'11	'32
4	'11	'32	'17
5	'32	'17	'16
6	'17	'16	'15
7	'16	'15	'35
8	'15	'35	'52

TABLE 2-28: ICS1 ADDRESS JUMPERS

DEV. ADDR.	IC 37D PIN TO IC 37D PIN	IC 37D PIN TO IC 37D PIN
'36	15 to 12	16 to 7
'37	15 to 12	16 to 8
'10	15 to 14	16 to 1
'11	15 to 14	16 to 2
'32	15 to 12	16 to 3
'17	15 to 14	16 to 8
'16	15 to 14	16 to 7
'15	15 to 14	16 to 6
'35	15 to 12	16 to 6
'52	15 to 10	16 to 3

2.8.10.8.2 ICS1 Cabling

To cable the ICS1, refer to Figure 2-37 and Table 2-29.

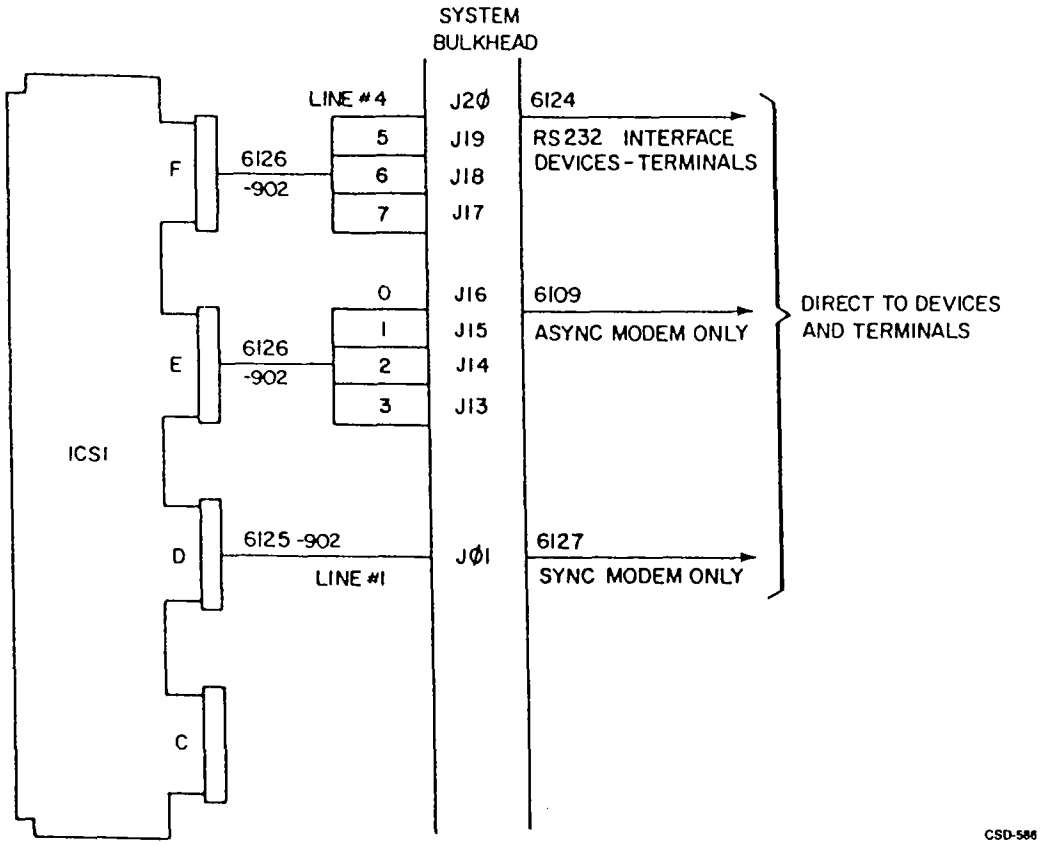


FIGURE 2-37: ICS1 BULKHEAD CABLING

TABLE 2-29: ICS1 CABLE TO BULKHEAD CONFIGURATION

ICS1 BOARD	CONNECTOR	ICS1 LINE #	BULKHEAD SLOT
1 Device Address = 36	C	LEDs	Not Used
	D	Synchronous	J01
	E	4	J13
		3	J14
		2	J15
		1	J16
	F	8	J17
		7	J18
		6	J19
		5	J20

TABLE 2-29: ICS1 CABLE TO BULKHEAD CONFIGURATION (Cont.)

ICS1 BOARD	CONNECTOR	ICS1 LINE #	BULKHEAD SLOT
2 Device Address = 37	C	LEDs	Not Used
	D	Synchronous	J02
	E	12	J24
		11	J25
		10	J26
		9	J27
	F	16	J28
		15	J29
		14	J30
		13	J31

2.8.10.9 ICS2 Configuration

The ICS2 controller board has two configurable options:

- Device address
- Microprocessor RAM size

The device address is the I/O bus address that the controller responds to during Programmed I/O (PIO) instructions from the system CPU. The ICS2 controller can be configured to one of two possible device addresses: '10 or '11. A system with two ICS2 controllers must be configured with one board at '10 and the other at '11.

The ICS2 controller device address is selected by using the proper header dip at location 49B. To select a device address of '10, header dip ADA1820-917 must be inserted into location 49B. To select device address '11, header dip ADA1820-918 must be inserted at location 49B.

With the microprocessor RAM size option, the ICS2 controller can be configured to have either 64K words or 128K words of microprocessor RAM. A board with 64K words of RAM is configured with 18 dynamic RAM parts residing in board locations 03F-17F and 03H-17H. A board with 128K words of RAM is configured with 36 dynamic RAM parts residing in board locations 03E-17E, 03F-17F, 03G-17G and 03H-17H. There are no other differences between the 64K and 128K word board options.

Table 2-30 shows the available ICS2 controller board options and their distinguishing characteristics.

TABLE 2-30: ICS2 CONTROLLER BOARD OPTIONS

BOARD #	DEVICE ADDRESS	RAM SIZE
2034-901	'10	64K words
2034-902	'11	64K words
2034-903	'10	128K words
2034-904	'11	128K words

2.8.10.9.1 ICS2 Controller to Buffer Board Cabling

Figure 2-38 shows the proper controller to bulkhead cabling. An ICS2 controller is connected to a buffer board as follows:

- From the controller to the system bulkhead (CBL6268-901)
- From the system bulkhead to the ICS2 card cage bulkhead (CBL6796-001 (ten-foot) or CBL6796-002 (thirty-foot))
- From the card cage bulkhead to the buffer board(s) (Single buffer board: CBL6268-901 or Double buffer board: CBL6267-901)

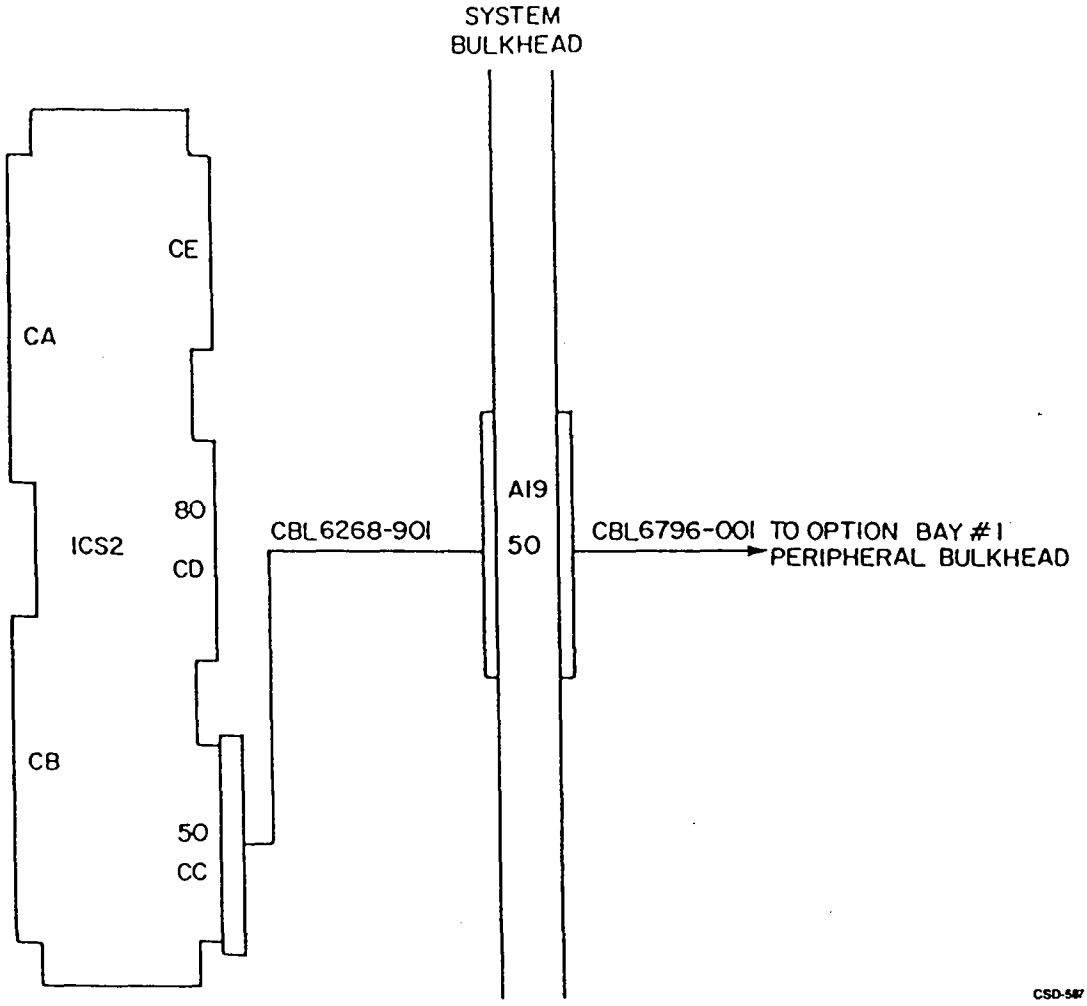


FIGURE 2-38: ICS2 BULKHEAD CABLING

2.8.10.9.2 ICS2 Buffer Board Configuration

The ICS2 buffer board, which is located in the ICS2 card cage, is available in two configurations:

- Terminated (ESA5238-901)
- Nonterminated (ESA5238-902)

A terminated buffer board has two cable terminating resistor dips at board locations 09A and 11A. The nonterminated board has nothing at these dip locations. A terminated buffer board must be used if it is the only, or the last, buffer board connected to a controller board to buffer board cable.

2.8.10.9.3 ICS2 LAC Bus Backplane Configuration

Each Line Adapter Card (LAC) bus backplane supports one power supply, one buffer board and from one to eight LACs. Looking at the backplane from the front of the card cage, the power supply is always plugged into the left-most slot. Moving to the right, the buffer board is in the next slot. The remaining eight slots are for LAC cards.

There are two possible ways in which the LAC bus backplanes are configured in manufacturing. The first configuration has no jumpers on the backplane. This configuration sets the slot addresses of the eight LAC slots to $0 through $7. The other configuration requires a jumper wire on the buffer board slot of the backplane connecting pin CA-07 with pin CA-44. Providing this jumper wire causes the 'FIRST-' signal on the backplane to be hard-wired to a high state. Without the jumper, the 'FIRST-' signal will be hard-wired to a low state. With this configuration, the slot addresses of the eight LAC slots will be set to $8 to $F. Whenever two LAC bus backplanes are connected together using the double cable (CBL6267-901), their LAC slot addresses must be different. That is, one backplane must have the jumper present and the other must not. The two versions of the LAC bus backplane are presented in Table 2-31.

TABLE 2-31: LAC BUS BACKPLANES

LAC BUS BACKPLANE #	ADDRESSING
ESA4939-901	Slots $0 - $7 (no jumper wire)
ESA4939-902	Slots $8 - $F (jumper wire required)

2.8.10.9.4 ICS2 LAC Bus Power Supply Configuration

The LAC bus power supply, which is located in the ICS2 card cage, has no configuration options. It is available in only one version.

2.8.10.9.5 ICS2 Asynchronous RS232 LAC Configuration

The asynchronous RS232 LAC, which is located in the ICS2 card cage, has no configuration options. There is only one version of this board.

2.8.10.10 Asynchronous Multi-Line Controller (AMLC) Configuration

The 50 Series system can support a maximum of four AMLCs. These allow a total of 64 directly connected users. The Asynchronous Multi-Line Controller (AMLC) is offered in two models:

- Model 5054
- Model 5154

Model 5054 transmits data on a character basis. Model 5154 transmits data on a block basis via the DMQ. Model 5154 is referred to as a QAMLC. The system can be configured with a maximum of four boards.

Instructions for AMLC address conversion, baud rate conversion and cabling are provided below.

2.8.10.10.1 AMLC Address Conversion

Boards shipped from the factory as spares or add-ons have an address of '54. To change the address, you must change one end of the address jumpers at locations 37B and 39B as shown in Table 2-32. IC 37B selects the high order address bits 50 and 30. IC 39B selects low order address bits 02, 03, 04, and 05.

NOTE

The wires on 37B and 39B should go to the etch pad associated with the desired pin. Do not solder the wire to the dip lead. Use new 24 gauge insulated wire.

TABLE 2-32: AMLC ADDRESS JUMPERS

AMLC#	DEVICE ADDR.	IC 37B TO 31D PIN	IC 39B TO 31D PIN
1	'54	6 to 5	5 to 9
2	'53	6 to 5	4 to 9
3	'52	6 to 5	3 to 9
4	'35	4 to 5	6 to 9
5	'15	2 to 5	6 to 9
6	'16	2 to 5	7 to 9
7	'17	2 to 5	9 to 9
8	'32	4 to 5	3 to 9

2.8.10.10.2 AMLC Baud Rate Conversion

AMLC boards have eight different line speeds that are selectable by bits 8, 9 and 10 of the line configuration control word (OTA '0154). Four of these line speeds are fixed at 110, 134.5, 300, and 1200 Baud. One line is a programmable rate, and three lines are selectable via hardware jumpers. The factory presets the selectable rates at 75, 150, and 1800 baud.

These selectable clocks can be changed via the three jumpers on the header dip at location 1K (see Table 2-33). IC 1K pins 1-8 contain the available baud rates. Selectable baud rates are on IC 1K pins 15, 10, and 13. To change a selectable baud rate, control word bits 8, 9, and 10 must be set to '101, '110, and '111 respectively.

TABLE 2-33: AMLC BAUD RATE CONVERSION

PIN NO.	BAUD RATE
1	75
2	600
3	150
4	19200
5	9600
6	4800
7	2400
8	1800

Standard baud rate selections are jumpered:

75 baud = IC 1K pin 1 to 15
150 baud = IC 1K pin 3 to 10
1800 baud = IC 1K pin 8 to 13

After jumpering the selected baud rate, the baud rate can be assigned using the PRIMOS AMLC command CONFIG parameter (refer to #80 Service Manual).

2.8.10.10.3 AMLC Cabling

Refer to Table 2-34 and Figure 2-39 for proper cabling procedures. Each AMLC cable should be marked with the actual AMLC (octal) line numbers connected to it.

TABLE 2-34: AMLC CABLE TO BULKHEAD CONFIGURATION

AMLC BOARD #	CONNECTOR	PHYSICAL BOARD LINE	AMLC LINE #	BULKHEAD PORT-CABLE CONNECTOR	USER #
1 Device Address= 54	C	1	0	J20	2
		2	1	J19	3
		3	2	J18	4
		4	3	J17	5

TABLE 2-34: AMLC CABLE TO BULKHEAD CONFIGURATION (Cont.)

AMLC BOARD #	CONNECTOR	PHYSICAL BOARD LINE	AMLC LINE #	BULKHEAD PORT-CABLE CONNECTOR	USER #
		5	4	J16	6
		6	5	J15	7
	D	7	6	J14	8
		8	7*	J13	9
		9	10	J12	10
		10	11	J11	11
	E	11	12	J10	12
		12	13	J21	13
		13	14	J31	14
		14	15	J30	15
	F	15	16	J29	16
		16	17*	J28	17
2 Device Address= 53		1	20	J27	18
		2	21	J26	19
	C	3	22	J25	20
		4	23	J24	21
		5	24	J23	22
		6	25	J22	23
	D	7	26	J32	24
		8	27*	J33	25
		9	30	J41	26
		10	31	J40	27
	E	11	32	J39	28
		12	33	J38	29
		13	34	J37	30
		14	35	J36	31
	F	15	36	J35	32
		16	37*	J34	33
3 Device Address= 52		1	40	J104	34
		2	41	J103	35
	C	3	42	J102	36
		4	43	J101	37
		5	44	J100	38
		6	45	J99	39
	D	7	46	J98	40
		8	47*	J97	41
		9	50	J96	42
		10	51	J95	43
	E	11	52	J94	44
		12	53	J105	45

TABLE 2-34: AMLC CABLE TO BULKHEAD CONFIGURATION (Cont.)

AMLC BOARD #	CONNECTOR	PHYSICAL BOARD LINE	AMLC LINE #	BULKHEAD PORT-CABLE CONNECTOR	USER #
		13	54	J115	46
		14	55	J114	47
	F	15	56	J113	48
		16	57*	J112	49
4		1	60	J111	50
Device		2	61	J110	51
Address=	C	3	62	J109	52
35		4	63	J108	53
		5	64	J107	54
		6	65	J106	55
	D	7	66	J116	56
		8	67*	J117	57
		9	70	J125	58
		10	71	J124	59
	E	11	72	J123	60
		12	73	J122	61
		13	74	J121	62
		14	75	J120	63
	F	15	76	J119	64
		16	77*	J118	65

* The last available line on the last AMLC board in a PRIMOS system must be set to 110 baud or 300 baud. This would be the eighth line on an eight-line AMLC or the 16th line on a 16-line AMLC. This line is the group 1 line and is used by the system to process input characters. All other lines on the system are designated the "group zero" lines. The last ACTIVE group zero line determines the maximum effective output baud rate of ALL active lines on the system (except those using high-speed protocol).

2.8.10.11 Synchronous Controller (MDLC) Configuration

The Multi-Line Data Link Controller (MDLC), Model 5602, is available with either two or four data lines. A maximum of two MDLCs may be configured per system; PRIMOS must be at Rev. 16 or higher. Address conversion and cabling information is presented in the following subsections.

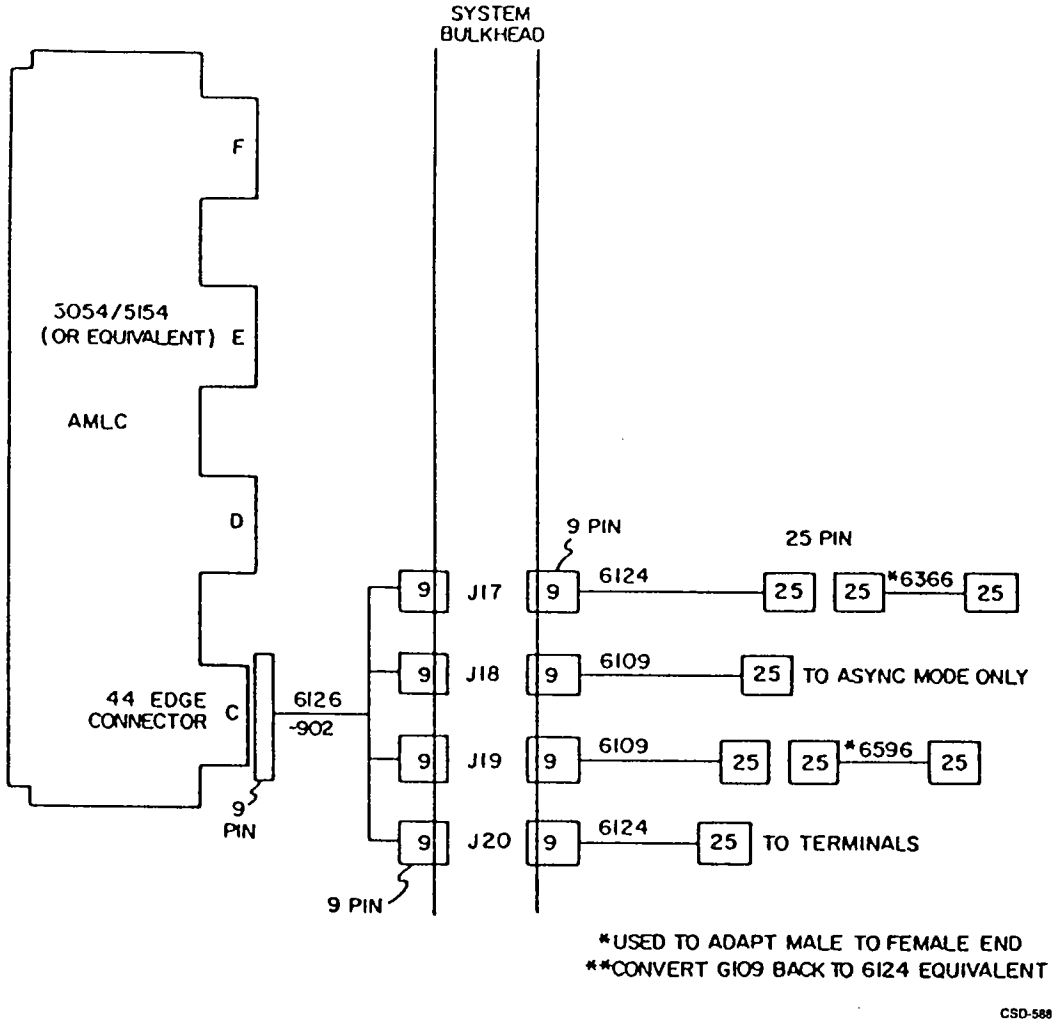


FIGURE 2-39: AMLC BULKHEAD CABLING

2.8.10.11.1 MDLC Address Conversion

The device address and MDLC protocol are configured at the factory. Jumper dip 49B controls the device address. For device address '50, jumper dip 49B pin 15 is connected to pin 11, and pin 16 is connected to pin 8. If two MDLCs are installed in a system, the second MDLC's device address must be changed from '50 to '51. To do this, connect jumper dip 49B pin 16 to pin 7. Leave the pin 15 connection as it is.

2.8.10.11.2 MDLC Cabling

Refer to Figure 2-40 and Table 2-35 to properly cable the controller to the system bulkhead.

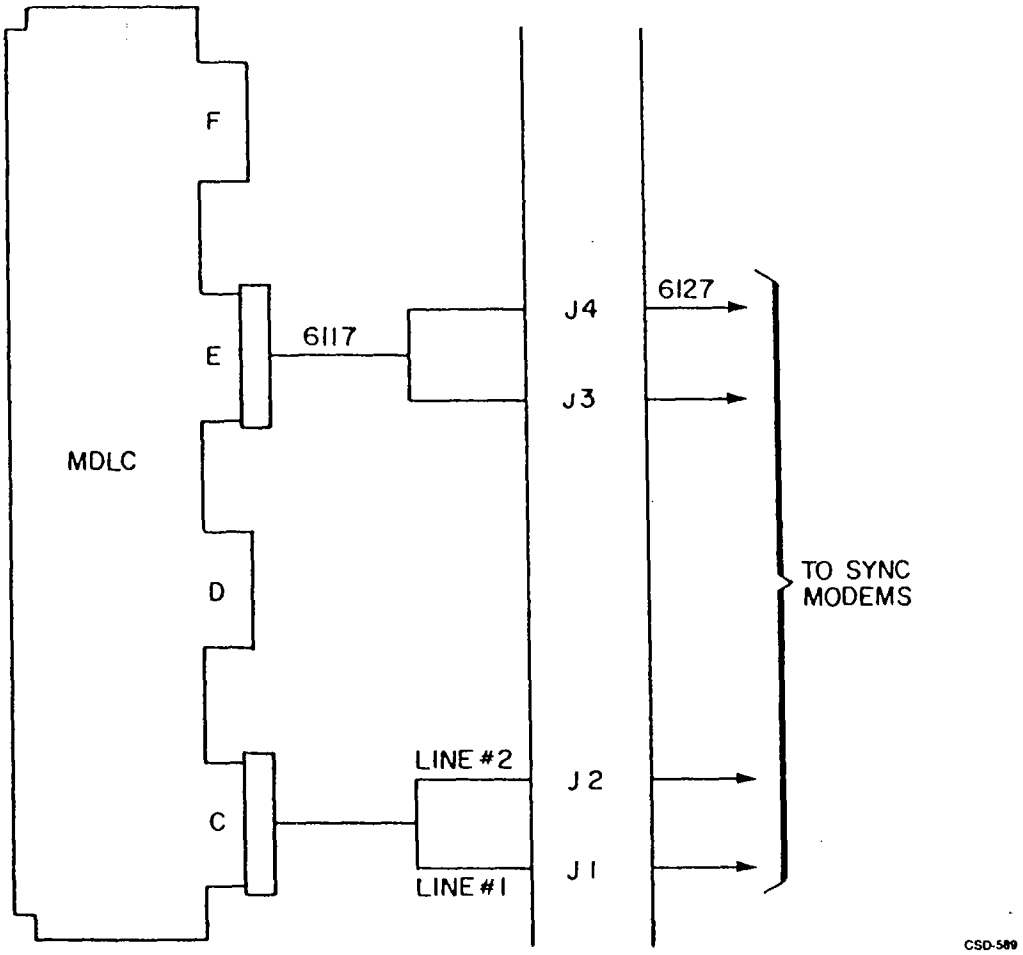


FIGURE 2-40: MDLC BULKHEAD CABLING

TABLE 2-35: MDLC CABLE TO BULKHEAD CONFIGURATION

MDLC BOARD #	CONNECTOR	PHYSICAL BOARD LINE	MDLC LINE #	BULKHEAD USER PORT #
1		0	1	J9 1
Device Address= 50*	C	1	2	J8 2
	D		NOT USED	
		2	3	J7 3
	E	3	4	J6 4
	F		NOT USED	
2		4	5	J5 5
	C	5	6	J4 6

TABLE 2-35: MDLC CABLE TO BULKHEAD CONFIGURATION (Cont.)

MDLC BOARD #	CONNECTOR	PHYSICAL BOARD LINE	MDLC LINE #	BULKHEAD USER PORT #
Device Address 51	D		NOT USED	
		6	7	J3 7
	E	7	8	J2 8
	F		NOT USED	

2.8.10.12 PRIMENET Node Controller (PNC) System Configuration

The PNC and PRIMENET software support local ring networks of up to 15 systems. Systems must be no further than 750 feet apart and each system must have a PNC installed. PRIMENET requires at least Rev. 16.4 PRIMOS. At Rev. 18.3 PRIMOS, PRIMENET supports ring networks with PRIME and non-PRIME systems. Refer to Figures 2-41 and 2-42 while following the installation procedure below.

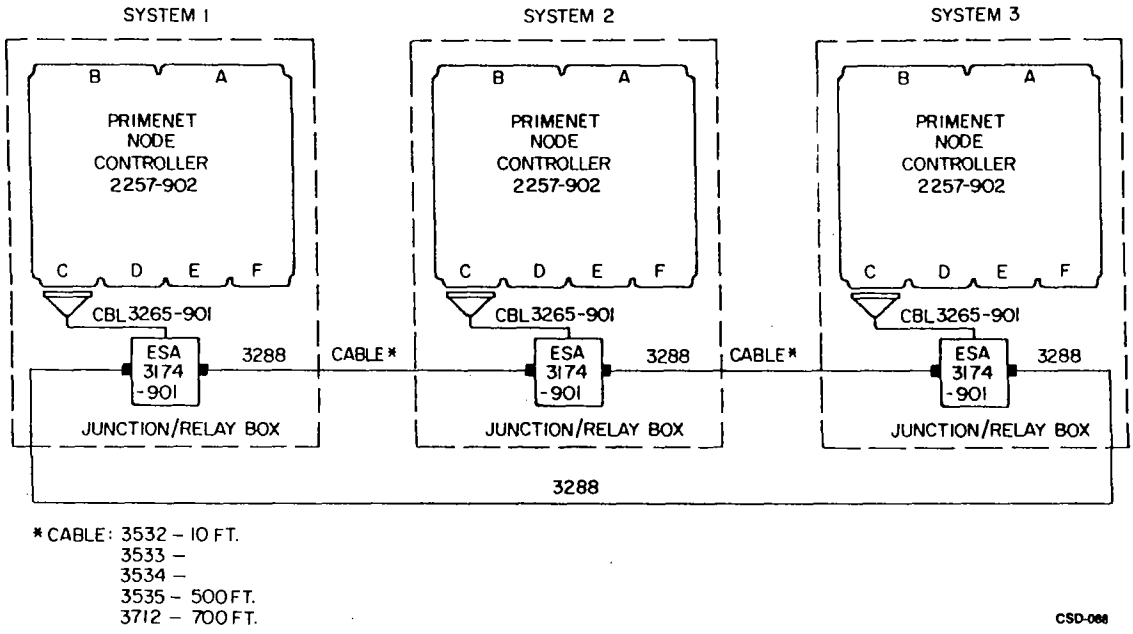
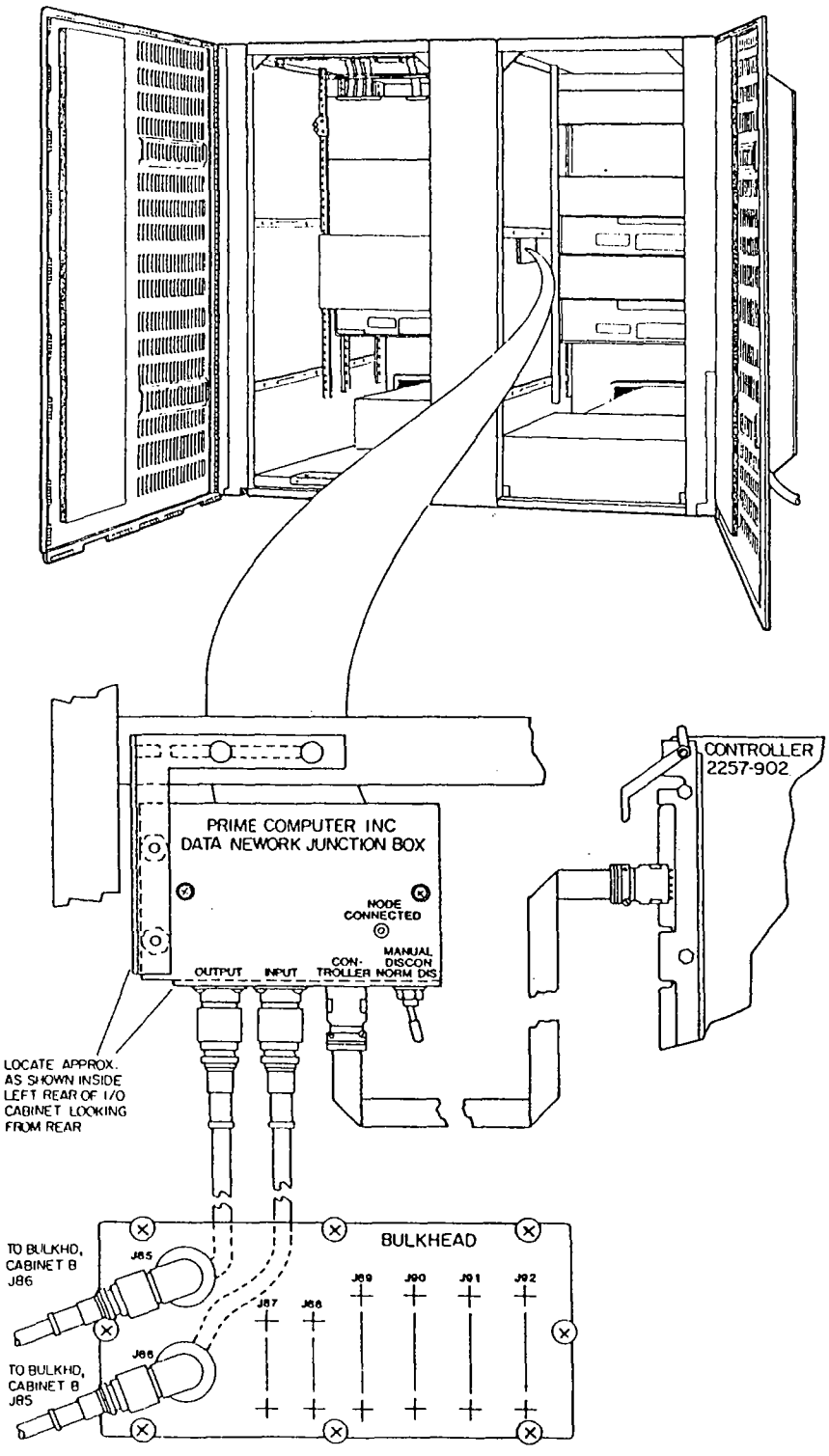


FIGURE 2-41: PNC INTERCABLING

1. Each PRIMENET node controller board (2257) should be installed in its respective system of the proposed network, according to the configuration sheet on the side door of the cabinet. If no slot assignment has been made for the board, consult your Senior Customer Service Representative for aid in making the assignment. Install the PRIMENET Node Controller (PNC) board in the proper slot of each system.



NOTES:

FOR EXTERNAL BULKHEAD CABLES, SELECT LENGTH PER FOLLOWING PRIME PART NUMBERS:

CBL3532-901=10FT. CBL3535-901=500FT.
CBL3533-901=50FT. CBL3712-901=750FT.
CBL3534-901=200FT.

CSD-089

FIGURE 2-42: PNC 50 SERIES CABLING

2. Install the junction/relay boxes in each system's mainframe cabinet at the right side of the cabinet.

3. Connect the flat cable 3265 to connector (44 pin) C on the PNC board. A yellow dot must face up when the cable is placed on the board. Connect the other end of the cable to the junction box (10 pin). The red dot faces upwards when the cable is inserted into the box.

4. Connect both 3533 cables to the In and Out connectors on the box and insert the other ends into bulkhead slots J85 and J86.

5. Ensure that each PNC is properly seated in the backplane.

6. The standard address is 07. There should not be a need to change this address. If two controllers are in a system, an unused address ('70 through '76) should be allocated.

2.8.10.13 Main OR I/O Cabinet To Peripheral Cabinet Cabling

To cable the Main or I/O Cabinet to the 53-inch Peripheral cabinet, refer to Figure 2-43.

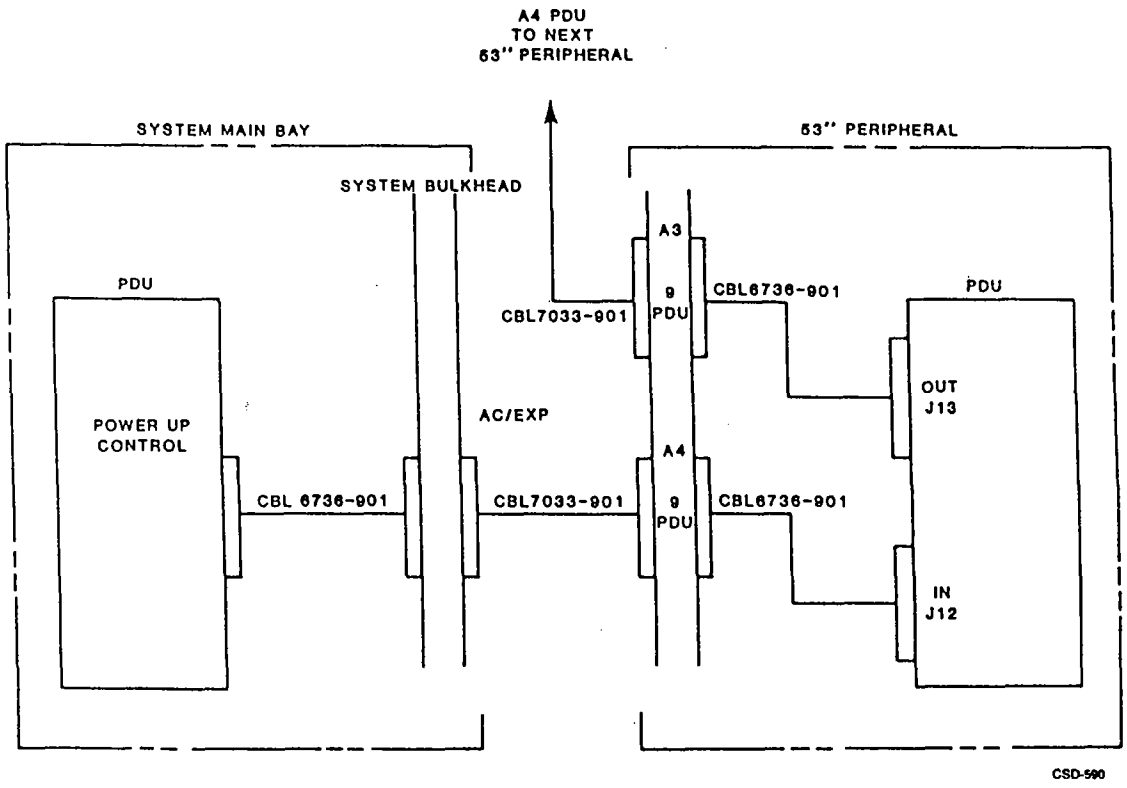


FIGURE 2-43: MAIN CABINET TO PERIPHERAL CABINET CABLING

2.8.10.14 Air Baffle Assembly Configuration

Air baffle assemblies (baffle boards) must be inserted into all empty slots of the CPU/memory chassis and I/O chassis to ensure that the air flow will circulate properly throughout the system. Failure to do so may result in the system overheating and triggering the environmental sensors which will cause the system to automatically shut down.

2.8.11 FREE-STANDING PERIPHERALS CABLING

To properly cable free-standing peripherals refer to the individual Service Manual for each peripheral and:

1. Connect the plug-end of each cable to its respective peripheral mating connector.

2. Using cable ties, coil excess lengths of cable wherever there is the most room: under the raised floor, in the cabinet or in the peripheral device.

2.8.12 PERIPHERAL EQUIPMENT GROUNDING

If any free-standing peripherals (excluding terminals) are to be connected to the 50 Series computer system, adequate grounding will be provided from peripheral frame to green earthing wire in the ac power cord. External green grounding cables should not be installed, as they may introduce ground loops. All free-standing peripherals should be connected to their ac power source according to the procedures in the appropriate Service Manual.

2.9 INSTALLATION CHECKOUT

Perform an installation checkout procedure for the 50 Series system to determine whether a system has been properly installed and functioning correctly. This procedure consists of:

- Power-Up
- Loading Operating System Software
- Final Checkout

2.9.1 POWER-UP

If any problems are encountered during the preliminary or operational checkout procedures, refer to Chapter 6, Corrective Maintenance, to solve the problem.

CAUTION

Before cycle-up, thoroughly clean the storage module and other disk devices. Perform installation checkout procedures per the appropriate Service Manual. Allow the unit(s) to purge while checking out the peripheral devices on the system.

1. Throw the main ac circuit breakers on all main and option cabinet PDUs to the "on" position. Each PDU's red light should light up and the blowers in each cabinet should start operating.

2. Power up the system terminal or CRT. Set the console for full duplex and 300 baud. Verify that the console is set for "online" and "uppercase". If the console is a Terminet and the INTERRUPT light is on, clear the error by pressing the INTERRUPT button.

3. Press the POWER button on the VCP status panel. This message will appear at the console:

```
VCP   version #   version date

*** CPU VERIFIED ***
CP>
```

If the CPU does not verify, an error message will appear or an LED fault light will light on the back edge of the VCP board. Refer to Chapter 6 for troubleshooting procedures if the VCP does not verify.

4. Power up all peripheral devices. Verify that normal power-on indications are present. If indications are abnormal, consult the Service Manual for the device.

5. Install a scratch pack in each disk device. Verify that each device cycles up normally.

6. Install scratch media on all other peripherals (mag-tape drive, printers, paper tape devices). Verify that the devices cycle up and operate normally. (Perform the installation checkout procedures as specified in appropriate Service Manuals.)

7. Install the master pack on SMD unit#0 (disk device 0) and cycle up the device. (A PRIMOS master pack is supplied with each system.) Verify that the device is in its READY condition.

2.9.2 LOADING OPERATING SYSTEM SOFTWARE

Determine whether the system contains a Storage Module Drive (SMD). If the system contains an SMD, the operating system is contained on the removable disk pack. If the system contains an FMD rather than a SMD device, the operating system must be loaded from the two logical tapes which have been provided. Select the appropriate procedure.

2.9.2.1 SMD Present: Loading OS From A Disk Pack

To load the operating system from a disk pack:

1. Configure the system so that the SMD device is on the first line of the first controller. Perform the installation checkout procedures for that device by referring to the appropriate Service Manual.

2. Place the system disk pack into the drive.

3. Cold Start and allow the system to AUTOBOOT the software. (Refer to Chapter 3, Power-up procedure.)

4. To configure the system software, refer to Chapter 2 (Installation) of the #80 Service Manual.

5. Run the MAKE utility on all other disk devices (refer to the MAKE section in the 300MB FMD Service Manual, TEAMAN320).

6. Check all other devices on the system using the PRIMOS utilities.

7. Check as many asynchronous terminal lines as posible by entering LOGIN and LOGOUT on each user terminal.

8. Continue with the Final Checkout procedure located at the end of this chapter.

2.9.2.2 No SMD: Loading OS From Tape

To load the operating system from tape:

1. Attach the disk device that will contain the operating system to the first line of the first controller.

2. Mount the Boot tape on Tape Drive 0. Load the tape to its load point.

3. Boot PRIMOS II (entries are underlined):

```
<ESC><ESC>
STOP
DPM400: CPU halted at XXXXXX:XXXXXX
        <Date and Time>

CP> SYSCLR
DPM006: Central Processor initialization completed.
        <Date and Time>
CP> BOOT 15
DPM007: System booting, please wait.

TREENAME = *DOS64
PRIMOS II REV 19.2 <Date> (AT 170000)

OK:
```

4. If a remake and restore is needed on the master disk, proceed to step 5.

   If a MAKE is not needed on the master disk, proceed to step 9.

5. Return to control panel mode:

```
OK:  <ESC><ESC>
CP>
```

6. Load MAKE:

```
CP> STOP
DPM400: CPU halted at XXXXXX:XXXXXX
        <Date and Time>

CP> SYSCLR
DPM006: Central Processor initialization completed.
        <Date and Time>
CP> BOOT 505
DPM007: System booting, please wait.
```

```
TREENAME = MAKE

DPM400: CPU halted at XXXXXX:000001
        <Date and Time>

CP>
```

NOTE

The halt location 000001 indicates that the load is successful.

7. Restart PRIMOS II:

```
CP> DOS
DPM006: Central Processor initialization completed.
        <Date and Time>

OK:
```

8. When the PRIMOS II prompt appears, start MAKE and enter physical device number (pdev) and partition name:

```
OK: START 1000 -DISK pdev -PARTITION name -BADSPOT LEVEL 4
GO
**** MAKE <REV. 19.2>

MAKING <#> HEAD PARTITION name
PARTITION SIZE IN DECIMAL RECORDS:  rrrrr

CHECKING FOR BADSPOTS
          .
          .
          .
DONE CHECKING FOR BADSPOTS
DISK CREATED

OK:
```

9. Load MAGRST:

```
OK: <ESC><ESC>
CP> STOP
DPM400: CPU halted at XXXXXX:XXXXXX
        <Date and Time>
CP> BOOT 505
DPM007: System booting, please wait.

TREENAME = MAGRST

DPM400: CPU halted at XXXXXX:XXXXXX
        <Date and Time>

CP>
```

10. Restart PRIMOS II:

```
CP> DOS
DPM006: Central Processor initialization completed.
        <Date and Time>

OK:
```

11. Start MAGRST:

```
OK:  STARTUP pdev
OK:  ATTACH MFD XXXXXX
OK:  START 1000
GO
[MAGRST REV.  19.2]
Tape unit (9 Tik):  0
(Tape not at load point)
Enter logical tape number:  1
Name:  PRIMOS REV.  19.3
Date:  xxxxxx
Rev no:  0
Reel no:  1
Ready to restore:  YES
*** starting restore ***
*** end of logical tape ***
*** restore complete

OK:
```

12. Restore the operating system from the tape onto the disk.

13. Configure the system software as detailed in Service Manual TEAMAN80, Chapter 2.

14. Cold start the system.

15. Check all other devices, using utilities on the system, are working.

16. Run MAKE on all other disk devices.

17. Check as many asynchronous lines as possible by going through a LOGIN - LOGOUT procedure on each user terminal.

2.9.3 FINAL CHECKOUT

The final checkout procedure is listed below. Refer to Chapter 6 of this manual if any problems occur.

1. Enter Control Panel mode by pressing the ESCAPE key twice. Run all microdiagnostic routines as outlined in Chapter 6 of this manual.

2. REBOOT system to bring up PRIMOS.

3. Complete all Customer Service and installation reports.

CHAPTER 3
OPERATING INSTRUCTIONS

PRELIMINARY

The contents of this chapter have not been updated. Do not use this chapter as the sole source of 50 Series operating procedure information. An update to this chapter containing complete and up-to-date material will be distributed in the near future.

3.1 INTRODUCTION

This chapter includes general operating instructions for 50 Series processors. Operating instructions for any peripherals attached to the 50 Series systems can be found in the appropriate Service Manual. System operating procedures and information are presented in the following order:

- Controls and Indicators
- System Power-Up
- System Power-Down
- AUTOBOOT to PRIMOS
- Virtual Control Panel (VCP) Operation
- 50 Series Basic Operations
- T&M Operation

NOTE

This manual is designed to be used with the Customer Service System Software Manual 080 (TEAMAN080). PRIMOS and related software commands are defined in CS Manual 080.

3.2 CONTROLS & INDICATORS

This section details the controls and indicators of the 50 Series systems. The controls and indicators are located on the:

- System Status Panel
- Power Distribution Unit (PDU)

3.2.1 SYSTEM STATUS PANEL CONTROLS AND INDICATORS

Controls on the system status panel, also referred to as the VCP Status Panel, provide system operating mode information. This section describes status panels associated with both non-FCC and FCC style cabinets.

3.2.1.1 Non-FCC Cabinet Status Panel

There are two types of Non-FCC status panels associated with the 50 Series systems:

- 150-II/250-II/550-II Status Panel
- 750/850 Status Panel

These status panels are illustrated in Figure 3-1. The controls are described in Table 3-1 and status panel indicators are described in Table 3-2.

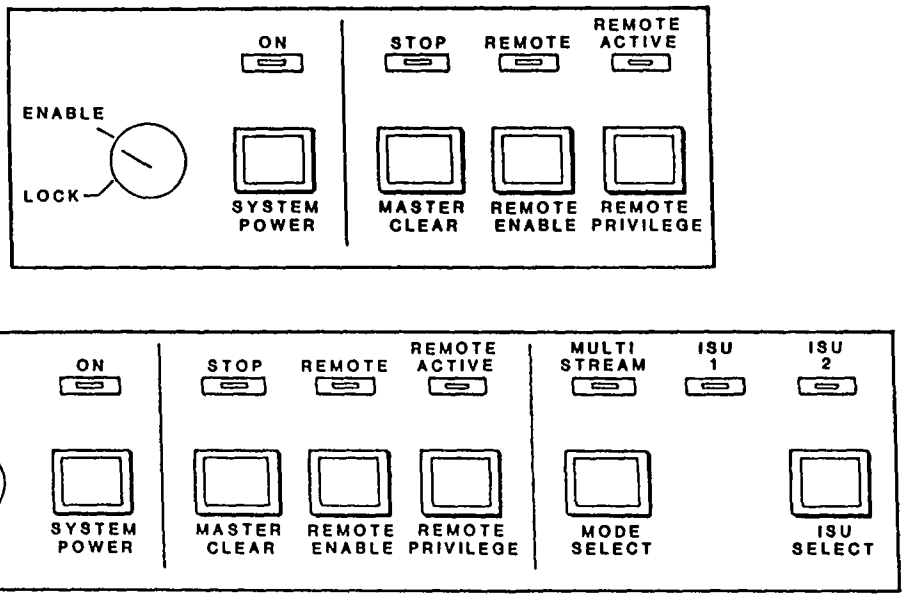


FIGURE 3-1: NON-FCC CABINET STATUS PANELS

TABLE 3-1: SYSTEM STATUS PANEL CONTROLS

CONTROL	FUNCTION
LOCK/ENABLE	Locks or enables the three function selection push-buttons (MASTER CLEAR, REMOTE ENABLE and REMOTE PRIVILEGE).
SYSTEM POWER	Starts the system power and AUTOBOOT TO PRIMOS sequence.
MASTER CLEAR	Initializes the system.
REMOTE ENABLE	Permits remote access to the system via the VCP.
REMOTE PRIVILEGE	Determines whether a remote operator has "full" or "monitor" access privileges. Full privileges are equivalent to the system console. With monitor priveleges, anything typed by the remote operator is displayed at the local system console, but does not affect the machine or VCP state.

TABEL 3-1: SYSTEM STATUS PANEL CONTROLS (Cont.)

CONTROL	FUNCTION
MODE SELECT*	Allows selection of either multi or uni-mode.
ISU SELECT*	Allows selection of one of two instruction stream units, each of which is similar in power to a 750 CPU.

*Located on 750/850 system non-FCC status panels only.

TABLE 3-2: SYSTEM STATUS PANEL INDICATORS

INDICATOR	DESCRIPTION
ON	When lit indicates that the power is on.
STOP	When lit indicates the CPU is halted.
REMOTE	When lit indicates that remote access is enabled.
REMOTE ACTIVE	When lit indicates that remote access with monitor privilege is in progress. When inidicator blinks continuously, indicates that full remote privilege is enabled.
MULTI STREAM*	When lit indicates the 850 is operating in multi-stream mode (both CPUs are active). When unlit, indicates the 850 is operating in uni-mode (one CPU active).**
ISU 1*	When lit indicates that the master (top CPU) is in use.
ISU 2*	When lit indicates that the slave (bottom CPU) is in use.

*Located on 750/850 system non-FCC status panels only.
**The 850 can run in uni-mode but is not meant to. When running in uni-mode, the 850 runs approximately 10

3.2.1.2 FCC Cabinet Status Panels

The system status panel on FCC cabinets, contains controls and indicators that provide system operating mode information. These controls and indicators are illustrated in Figure 3-2.

The status panel's controls are four pushbutton switches and a two-position key switch. The controls' functions are described in Table 3-3.

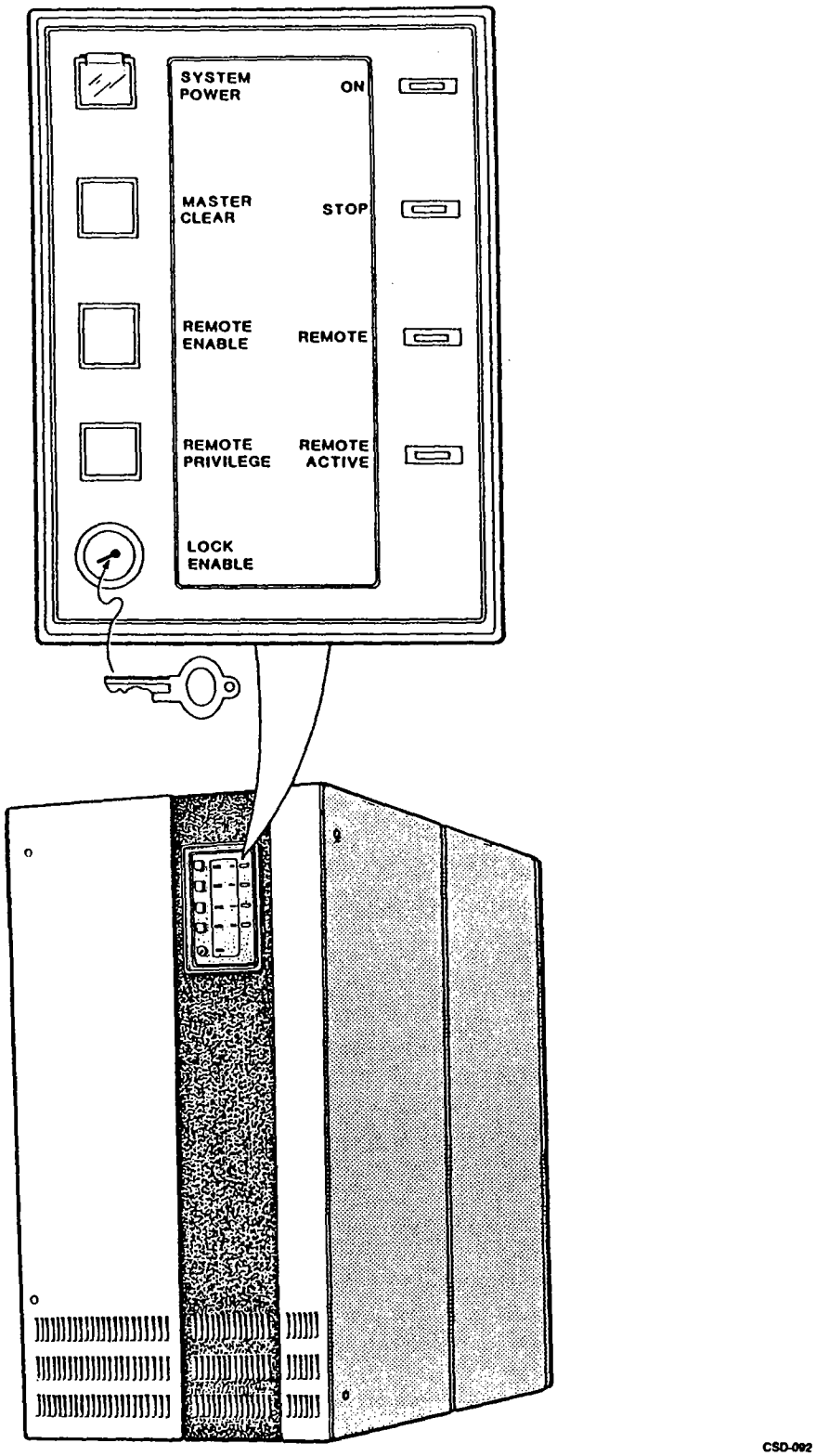


FIGURE 3-2: FCC CABINET STATUS PANEL

TABLE 3-3: SYSTEM STATUS PANEL CONTROLS

CONTROL	FUNCTION
SYSTEM POWER	A locking pushbutton switch. Depressing the switch starts the system power and AUTOBOOT TO PRIMOS sequence.
MASTER CLEAR	A momentary pushbutton switch. Depressing the switch starts the system.
REMOTE ENABLE	A locking pushbutton switch. Depressing the switch allows remote terminal access and system monitoring.
REMOTE PRIVILEGE	A locking pushbutton switch. Depressing the switch allows remote user privileges on the system.
LOCK/ENABLE	A two-position key switch. Keying the switch to ENABLE allows the above pushbutton switches to be used. The LOCK position disables the pushbutton switches.

Four LED indicators are located on the status panel. These indicators are described in Table 3-4.

TABLE 3-4: STATUS PANEL INDICATORS

INDICATOR	DESCRIPTION
ON	A green LED. The illuminated LED indicates system power is on.
STOP	A red LED. The illuminated LED indicates the CPU has halted.
REMOTE ENABLE	A yellow LED. The illuminated LED indicates the REMOTE ENABLE is on.
REMOTE ACTIVE	A yellow LED. The illuminated LED indicates a remote user is monitoring the system. The blinking LED indicates REMOTE PRIVILAGE is active. A stable LED indicates only REMOTE ENABLE is active.

3.2.2 POWER DISTRIBUTION UNIT CONTROLS AND INDICATORS

The 50 series computers utilize two types of PDUs:

- Non-FCC Cabinet PDU
- FCC Cabinet PDU

Non-FCC style PDUs have only one control, the AC main circuit breaker. This is an ON/OFF switch that either applies or discontinues power to the system. A POWER ON indicator is lit when the switch is in the ON position.

All 50 series processors housed in the FCC cabinets, utilize FCC style PDUs (Figure 3-3). The PDU contains three switch controls that are described in Table 3-5. The PDU has a single indicator, the FAULT INDICATOR. Under normal conditions, the indicator is white. The indicator becomes red when the PDU circuit breakers are tripped.

TABLE 3-5: FCC PDU CONTROLS

CONTROL	DESCRIPTION
MAIN CIRCUIT	An OFF and ON switch. This switch applies or discontinuous power to the system.
ECL POWER CIRCUIT (CB2)	An OFF and ON switch. This switch applies or discontinues power to the ECL-CPU power supply. Always OFF for 50 series systems.
REMOTE/LOCAL ON/LOCAL OFF	A three-position switch. The switch position selects either remote, local on, or local off system power.

3.3 SYSTEM POWER-UP

To power up a 50 series processor:

1. Switch the ac main circuit breaker on each cabinet's power distribution unit (PDU) to its "ON" position. The cabinet blowers should start up.

2. Apply ac power to the system console and set the baud rate to 300.

3. Lift the protective cover from the SYSTEM POWER switch and depress the switch. The POWER, REMOTE ENABLE AND REMOTE PRIVILEGE indicators should light momentarily. Only the POWER ON and STOP indicators remain lit. The system is initialized (Master cleared and microverified) and the VCP is set to 300 baud.

4. Cycle-up the remaining peripheral devices in the following order:

   A) Disk drives, beginning with the drive to be booted from (typically Drive 0 on the first controller)
   B) Magnetic tape drives
   C) Dataphone sets
   D) Printers

NOTE

Cycle up the command device (normally Drive 0 on the first controller) immediately after system power is on. This allows the AUTOBOOT to PRIMOS sequence to proceed smoothly.

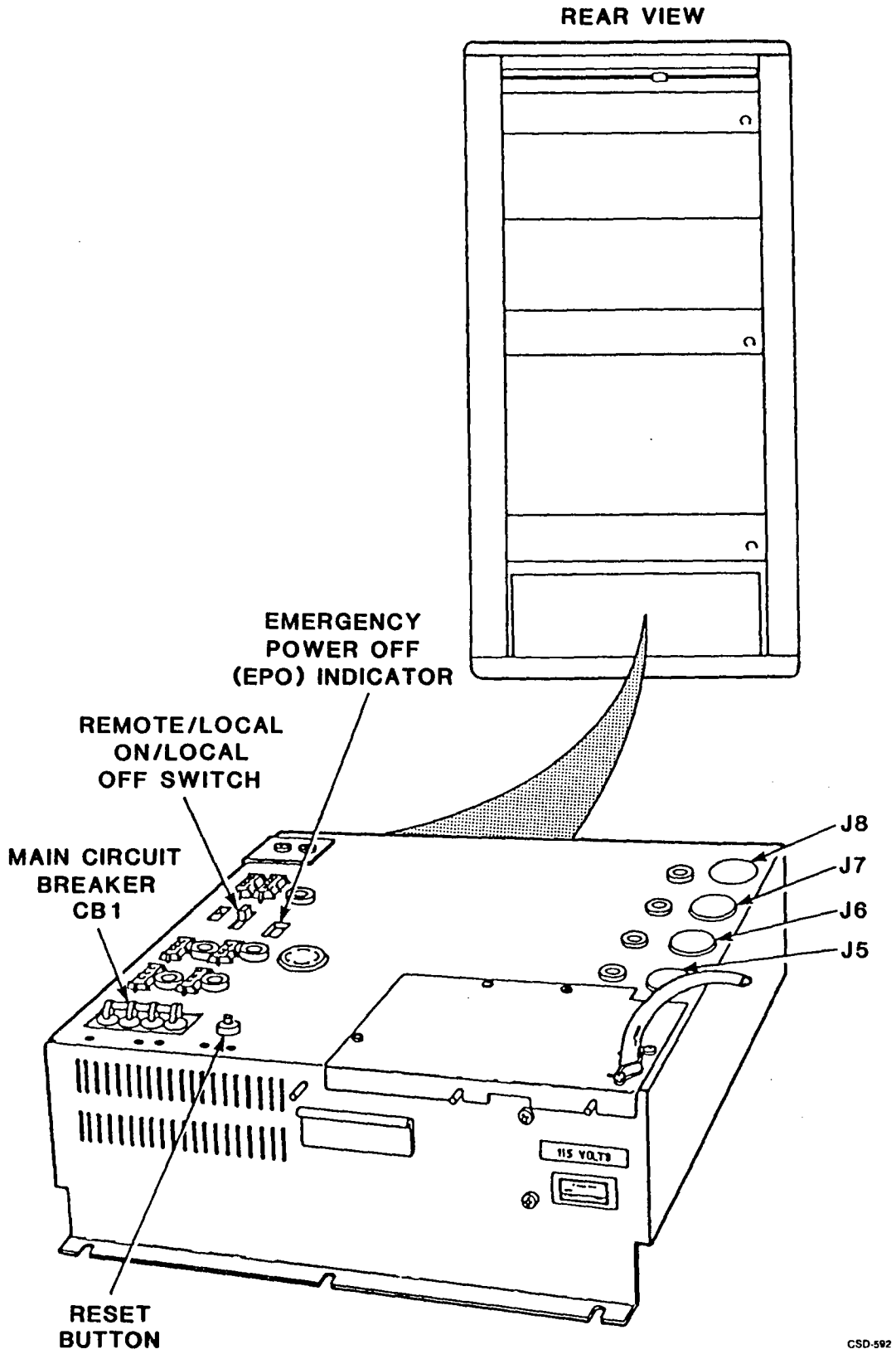


FIGURE 3-3: FCC CABINET PDU

3.4 SYSTEM POWER-DOWN

The system operator or administrator is responsible for the system's power-down. The CSR can use the following procedure if either the system administrator and operator are not available during an emergency situation or they give their approval. Power-down 50 series systems as follows:

- Shut down the operating system
- Remove the system's power

These procedures are outlined in the following sections.

3.4.1 OPERATING SYSTEM SHUT-DOWN

The operating system shut-down procedure is dependent upon whether PRIMOS or PRIMOS II is running. These shut-down procedures are outlined in the following sections.

3.4.1.1 PRIMOS Shut-down Procedure

Before shutting down PRIMOS:

1. Warn the system and remote system users that the system will be shut down. Messages are sent to the users from the system console. The local users are contacted by the following command:

```
OK, MESSAGE ALL -NOW
SYSTEM GOING DOWN IN 5 MINUTES.  PLEASE LOGOUT (Control G)
```

   To identify the system names on the network, use the command:

```
OK, STAT NET
Ring Network

    Node State
    SYSD ****
    SYSA UP
    SYSN DOWN
    SYST UP
```

   The remote system users are contacted by the following command format:

```
OK, MESSAGE -1 -NOW -ON <nodename>
System <name> is going down in 5 minutes.
```

2. Prevent new users from logging onto the system by using the command:

```
OK, MAXUSR 0
```

   Setting MAXUSR to zero does not interfere with users currently on the system.

3. Prevent subsystems from starting new jobs by shutting down the spooler phantoms and File Transfer Service (FTS) servers after finishing their current jobs.

NOTE

Insufficient time for the spool phantoms and FTS servers to log themselves out may result in database problems.

Identify the printers by using the command:

```
OK, PROP -STATUS
```

To shut-down the spool phantoms, use the command:

```
OK, PROP <printer name> -STOP
[PROP rev 19.2]

Wait...  Acknowledged
OK,
*** SYSTEM (user nnn on system name) at hh:mm
*SPOOL* <printer name> -STOPPING
```

To shut-down the FTS server, use the command:

```
OK, FTOP -STOP SRVR FTP
[FTOP rev 1.0]
Server notified to stop.
```

4. Send the warning to all users:

```
OK, MESSAGE ALL -NOW
SYSTEM GOING DOWN IN 1 MINUTE. (Control G)
```

5. Stop the Batch subsystem by the command:

```
OK, BATCH -STOP
[BATCH rev 19.0]
Stop request issued.

OK,
*** BATCH_SERVICE (user nnn on sysname) at hh:mm
Operator stop.
```

The 'Operator stop.' message indicates that the Batch monitor has logged out and the Batch subsystem is no longer running. The Batch jobs running when the BATCH -STOP command is given are completed.

6. Stop the FTS manager phantom by:

A) Determining the YTSMAN's user number by using the command:

```
OK, STATUS USERS
```

B) Then type the command line:

```
OK, LOGOUT -<YTSMAN's user number>
Phantom nn:  Normal logout at hh:mm
Time used:  xxh xxm connect, xxm xxs CPU, xxm xxs I/O
```

7. Send a final warning to all users:

```
OK, MESSAGE ALL-NOW
SYSTEM GOING DOWN.  PLEASE LOGOUT. (Control G)
```

8. Log out all users with the command line:

```
OK, LOGOUT ALL
```

9. Verify that all users and subsystems have been logged out by using the command, STATUS ALL.

10. Shut down the system by using the command:

```
OK, SHUTDN ALL
REALLY?  YES
WAIT,
PRIMOS NOT IN OPERATION

DPM400:  CPU HALTED AT 000006/003525:  003776
```

After completing the operating system shut-down procedure, remove the system's power as described in the section, REMOVING SYSTEM POWER.

3.4.1.2 PRIMOS II Shut-down Procedure

To shut-down PRIMOS II, use the command:

```
OK:  SHUTDN
OK:
```

This command does not halt the CPU, however it is 'shut down'. To halt the CPU, press the MASTER CLEAR button on the system status panel. Then remove the system power as described in the following section.

3.4.2 REMOVING SYSTEM POWER

Remove power from the system's equipment in the reverse order of system startup:

- Line printers
- Modems
- Magnetic tape drives
- Disk drives
- System CPU

3.5 AUTOBOOT TO PRIMOS

A successful power-up and AUTOBOOT sequence is completed in about two minutes. The AUTOBOOT to PRIMOS sequence can be initiated via one of two ways:

- At system power-up
- An operator command during Control Panel Mode

The AUTOBOOT sequence consists of thirteen steps. Some of these steps are accompanied by status messages from the Diagnostic Processor. If an error is encountered during the AUTOBOOT to PRIMOS sequence an appropriate error message is displayed and the VCP enters CP mode (see the VCP CP Mode subsection in this manual for details). Refer to the Troubleshooting section, Chapter 6 of this manual for AUTOBOOT to PRIMOS error message information.

3.6 VIRTUAL CONTROL PANEL (VCP) OPERATION

The VCP replaces the System Option Controller (SOC). It provides an asynchronous interface for the system console, as well as a serial printer interface. Through the system console, the VCP controls system operations such as automatic program loading (BOOT), power failure sequencing, and timing. In addition, the VCP is the asynchronous interface for the system console; thus replacing the old System Option Controller (SOC). Because the VCP can function in local or remote mode, the system console can be connected directly to the VCP or remotely, via a modem.

Three operating modes are available on the VCP: System Terminal (ST), Control Panel (CP), and Z80 micro-processor microcode Debugger (ZCD). In ST mode, the VCP performs all the functions of the system console, such as:

- Bringing up PRIMOS
- Sending messages
- Logging out users

In CP mode, the VCP performs control panel functions such as:

- Booting PRIMOS
- Reading register set locations
- Loading and running programs

ZCD mode is used to debug the VCP board at the Repair Center.

CAUTION

ZCD must NEVER be used while PRIMOS is operating. ZCD should only be used when debugging the VCP board at a Repair Center.

3.6.1 CONTROL PANEL (CP) MODE

In Control Panel (CP) mode, the VCP has all the capabilities of a system control panel, plus the flexibility to accept and display data from a terminal. Commands are entered with keywords, instead of pressing switches and turning a knob. Data may be accepted and displayed in hexadecimal, ASCII, binary, decimal, and octal.

On power up and Master clear, the VCP executes self-verify routines to ensure its own integrity. If an error occurs, the VCP may hang or an error message may be printed on the system console. Upon successful completion of VCP internal verify routines, CPU verification begins. If the CPU fails micro-verify, the message "$$$CPU DID NOT VERIFY$$$$" appears at the console. To determine the cause, you must examine DSWSTAT (see Chapter 6). If the CPU passed its integrity test, the VCP informs the operator by printing on the console:

```
VCP.04  11-09-79

*** CPU VERIFIED ***

CP>
```

The control panel mode prompt character, CP>, indicates that the VCP is ready to accept command input. To enter Control Panel mode, typethe following at the system console:

```
ESC ESC (2 escapes)
```

3.6.1.1 Controlling Supervisor Terminal Output

While the VCP is in Control Panel mode, the system supervisor terminal output (login messages, etc.) may be either ignored (lost), buffered, or interleaved with control panel output. The following three commands determine which will be done:

- SYSOUT BUFF - Buffers supervisor terminal output and then prints it when System Terminal mode is reentered. This is the default mode.
- SYSOUT IGN - Ignores supervisor terminal output while in control panel mode.
- SYSOUT INT - Interleaves supervisor terminal output with control panel mode output.

3.6.1.2 Halting the System

The "STOP" command halts the system.

```
ESC ESC
CP> STOP
CP> HALTED AT 010000: 0000011
CP>
```

3.6.1.3 Master Clearing the System

The "SYSCLR" command places the CPU in a known starting position. The CPU and I/O controllers are initialized, all CPU high speed register file locations are reset to 0, and the CPU is set to 16S addressing mode.

The "VIRY" command runs diagnostics to verify the VCP and then performs a SYSCLR. The following is an example:

```
ESC ESC
CP> STOP
CP> SYSCLR

*** CPU VERIFIED ***
CP>
```

3.6.1.4 Booting the System

"Boot" or "bootstrap" automatically loads in pre-boot and loader routines which then load the desired software. Booting is usually done from disk. This method is outlined below. Refer to Service Manual 80 for instructions on booting from a magtape device.

1. Install the appropriate media on the disk device you wish to boot from. The media must be formatted with BOOT on its first record (record 0). Wait until the device is cycled-up and ready (on CDC drives, READY light does not blink).

2. Determine the sense switch settings for the device you wish to boot from (see Table 3-6). Determine the partition's physical device number (from FESM #80).

TABLE 3-6: SENSE SWITCH SETTINGS FOR BOOT

Sense Switches: (1=set) 10 11 12 13 14 15 16g	OCT.	DEVICE	DISK CONTR.	DISK PLATTER	DEV. ADD.	1/2nd CONTR.	NOTE
							1
0 0 0 0 0 0 0	000						
0 0 0 0 0 0 1	001	ASR			'04	1st	
0 0 0 0 0 1 0	002	HSR			'02	1st	
0 0 0 0 0 1 1	003	FHD	4000		'22	1st	
0 0 0 0 1 0 0	004	MHD	4000	1st	'25	1st	
0 0 0 0 1 0 1	005	MAG,9-trk			'14	1st	
0 0 0 0 1 1 0	006	Diskette	4030/31		'12	1st	
0 0 0 1 0 1 1	013	FHD	4002/3		'21	1st	
0 0 0 1 1 0 0	014	MHD	4001/2/3	1st	'21	1st	2
0 0 1 0 1 0 1	025	MAG,7-trk			'14	1st	3
0 0 1 1 0 1 1	033	FHD	4002/3		'23	2nd	
0 0 1 1 1 0 0	034	MHD	4001/2/3	1st	'23	2nd	
0 1 0 0 1 0 0	044	MHD	4000	2nd	'25	2nd	
0 1 0 1 1 0 0	054	MHD	4001/2/3	2nd	'21	1st	
0 1 1 1 1 0 0	074	MHD	4001/2/3	2nd	'23	2nd	
1 0 0 1 1 0 0	114	SMD/CMD	4004/5/6	1st	'26	1st	4
1 0 1 1 1 0 0	134	SMD/CMD	4004/5/6	1st	'27	2nd	

SEE NOTES NEXT PAGE

NOTES : 1. Start program at location in SS1-SS9
2. Standard MHD selection
3. Unit 0
4. Standard SMD/CMD setting

NOTE

Controller device address assignments are listed in Appendix D. The octal device address indicates the controller address that BOOT uses, if the sense switches are set as indicated. This table is applicable for control panel prom rev. F through J.

It is also possible to boot from SMD/CMD first controller (address '26) drives 1, 2 and 3. Booting from these devices automatically loads a first-level BOOT from drive #0 and a second-level BOOT routine from the respective drive. Sense switches are set as follows:

SENSE SWITCHES										
08	09	10	11	12	13	14	15	16	OCTAL	
		1	0	0	1	1	0	0	'114	SMD/CMD #0
	1	1	0	0	1	1	0	0	'314	SMD/CMD #1
1	0	1	0	0	1	1	0	0	'514	SMD/CMD #2
1	1	1	0	0	1	1	0	0	'714	SMD/CMD #3

3. Enter the following commands at the system terminal:

```
CP> SYSCLR
*** CPU VERIFIED ***
CP> BOOT number
```

The "number" is the sense switch settings for the device. If you are booting from any partition of the first SMD, CMD, MMD, or FMD, enter '114'.

4. Enter the specific physical device number after the system's "PHYSICAL DEV=" prompt. The prompt indicates that the BOOT was successful.

```
PHYSICAL DEV= 460
PRIMOSII REV. 16.8 07/02/79(AT 170000)
STARTING UP DISK 000460
OK:
```

If the physical device is '000', PRIMOS will boot from the address in sense switch locations 1-9. Use the 'SS' CP mode command to set the sense switch values before entering the 'BOOT' command.

NOTE

An attempt to BOOT in PRIMOS II before the disk drive is ready may fail (no message will be printed at the system terminal). If this happens, wait for the drive to become ready and repeat the BOOT procedure.

If the baud rate of the system console is not set the same as the BOOT program, the 'PHYSICAL DEV=' prompt will not be printed. The baud rate on a Master disk is 300.

3.6.1.5 Accessing Memory and Register Files

3.6.1.5.1 Memory Addresses

Virtual memory is divided into segments, which are like chapters in a book. Each of these segments is subdivided into pages. Each page is then divided into words. There are 1024 words on a page and a maximum of 64 pages in a segment.

When entering VCP commands, anywhere an address is required, either "Segno/Wordno" or simply "Wordno" may be used. "Segno" is the segment number; "Wordno" is the word number in the segment. The VCP remembers the last segment number referenced as the current segment; it will use this current segment if "Segno" is omitted. The initial value of the current segment is zero (0).

To display the contents of word 12 in segment 3 and then the contents of word 14 in the same segment, use this command sequence:

```
DISPLAY 000003/000012
DISPLAY 000014
```

The VCP uses mnemonics, instead of addreses, to identify certain register locations. Register file locations are explained in Table 3-7. Two of the most important registers are "Keys" and "Modals". A bit-by-bit description of these appears in Tables 3-8 and 3-9. VCP mnemonics are explained in Table 3-10.

3.6.1.5.2 Data Representation

Data may be represented in any of 5 formats as follows:

```
:O :H :B :D :A
```

Data is displayed in octal, hexadecimal, binary, decimal or ASCII, respectively. If two indicators are used (for example, :B :H), the first refers to data, the second to address display. ":B :H" means display data in binary and addresses in hexadecimal. These indicators are also valid after the DUMP and ACCESS commands. Note, however, that the address mode indication will not take effect until the next command. For example, the command:

```
D 1000 1010 :A :O
```

dumps, in ASCII, from the locations '1000 to '1010 in the address mode at the time the DUMP command was given. The address could be octal,

hexadecimal, decimal, or binary, because ":A" is not valid for address display. The default is :0 :0.

3.6.1.5.3 Control Panel Commands

The following commands enable the VCP to perform the operations of a control panel:

- BOOT - Places VCP in auto-boot condition.
- BOOT <number> - Boots with sense switches set to "number". "BOOT 114" bootstraps from a SMD, CMD, MMD, or FMD.
- DISPLAY <address> - Displays contents of "address". This command only operates when multi-user PRIMOS is running.
- DISPLAYC <address> - Continuously displays contents of "address". The value is displayed each time it changes. This command only operates when multi-user PRIMOS is running. To end display, enter CONTROL-P.
- FETCH - Fetches data according to the previously set sense and data switches.
- LIGHTS - Displays the current lights.
- LIGHTSC - Displays current lights continuously. The lights are displayed each time they change. To end display, enter CONTROL-P.
- RCP <location> - Identical to RUN (see below), except that the VCP stays in CP mode. The "location" may be a virtual address if the CPU is running in segmented mode.
- RUN <location> - Clears the sense switches and places the CPU in RUN mode at "location". (This causes a problem when running T&Ms.)

  If location is not supplied, the current value of RP (program counter) is used. (After a "SYSCLR", the current value is '1000.)

  This command automatically puts the VCP in ST mode (see RCP).
- SD <number> - Sets the DATA switches to the value of "number" for one INA instruction only.
- SS <number> - Sets the SENSE switches to the value of "number".
- SSTEP <n> - Single steps "n" locations. The value of "n" depends upon the data representation. For example, if the data specification is octal, "SSTEP 10" steps 8 locations.
- STEPU <n> - Steps until address is equal to "n".
- STORE <n> - Stores the value of "n" into the location specified by the previously set sense and data switches.

3.6.1.5.4 Memory Display Commands

These commands display/modify the CPU registers and memory locations.

- MO ABS - Sets VCP to reference absolute (physical) memory locations.
- MO MAP - References mapped memory (default) locations.
- MO RFABS - References register file absolute locations.
- MO RFCRS - References register file current register set (CRS) locations.
- MO RFH - Displays/modifies high side of register file.
- MO RFL - Displays/modifies low side of register file.

NOTE

When register file mnemonics are used, both high and low sides are displayed. The high-low mode determines which side is modified by the "Access" command.

TABLE 3-7: REGISTER FILE LOCATIONS

SCRATCH RF0 ADR	HIGH	LOW	DMX* RF1 ADR	HIGH	LOW	LOC ADR	RF2 ADR	RF3 ADR	CURRENT REGISTER SETS HIGH/LOW
0	TR0		40			00	100	140	GR0:OLT2
1	TR1		41			01	101	141	GR1:PTS
2	TR2		42			02	102	142	GR2(1,A)** /LH(2,B,LL)
3	TR3		43			03	103	143	GR3 (EH)/(EL)
4	TR4		44			04	104	144	GR4
5	TR5		45			05	105	145	GR5(3,S,Y)
6	TR6		46			06	106	146	GR6
7	TR7		47			07	107	147	GR7(0,X)
10	RDMX1		50			10	110	150	FAR1(13)/FR0
11	RDMX2		51			11	111	151	FLR1
12	USCADDR	REOIV	52			12	112	152	FAR2(4)(5)/FR1
13	RSGT1		53			13	113	153	FLR2:VSC(6)/FAC
14	RSGT2		54			14	114	154	PB
15	RECC1		55			15	115	155	SB(14) (15)
16	RECC2		56			16	116	156	LB(16) (17)
17		RATMPL	57			17	117	157	XB
20	ZERO	ONE	60	(20)	(21)	20	120	160	DTAR3(10)
21	PBSAVE		61			21	121	161	DTAR2
22	RDMX3		62	(22)	(23)	22	122	162	DTAR1
23	RDMX4		63			23	123	163	DTAR0
24	C377	C377	64	(24)	(25)	24	124	164	KEYS (MODALS)
25	MINUS1	MINUS2	65			25	125	165	OWNER
26	WWADTRH***	WWADTRL***	66	(26)	(27)	26	126	166	FCODE(11)
27	DSWPARITY		67			27	127	167	FADDR (12)

TABLE 3-7: REGISTER FILE LOCATIONS (Cont.)

SCRATCH RF0 ADR HIGH	LOW	DMX* RF1 ADR	HIGH	LOW	LOC ADR	RF2 ADR	RF3 ADR	CURRENT REGISTER SETS HIGH/LOW
30 PSWPB		70	(30)	(31)	30	130	170	TIMER
31 PSWKEYS		71			31	131	171	(CR31)
32 PPA: PLA PCBA		72	(32)	(33)	32	132	172	(CR32)
33 APADR*** (PPB: PLB PCBB)		73			33	133	173	CPUNUM***
34 DSWRMA		74	(34)	(35)	34	134	174	TPB
35 DSWSTAT		75			35	135	175	TSB
36 DSWPB		76	(36)	(37)	36	136	176	TLB
37 RSAVPTR		77			37	137	177	XEQPBH XEQPBL

NOTES

Registers are defined in Chapter 6.
VCP Register Mnemonics appear in Table 3-10.

* Only even DMX channel numbers (20-36) are available to the P350 (8 channels total), hence there are only 72 usable register file locations on the P350.

** Numbers in parenthesis are Memory/Register locations, and Mnemonics accessed when in basic Sectored and Relative modes (P300). For example, (1,A) is memory location 000001, the A Register.

*** Registers used by the Multi-Stream Processor (850)

TABLE 3-8: KEYS AND MODALS

KEYS: (KEYS HIGH) BITS															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
C BIT	D P	L I N K	ADR. MODE			F L E X	I E X	C L T	C E Q	D E X			I C	I D	S D

- CBIT: Carry bit, set by an arithmetic error condition.
- DP: Double Precision Floating Point operation.
- LINK: Indicates a Carry out from an arithmetic or shift operation.
- ADR. MODE: 0=16S, 1=32S, 2=64R, 3=32R, 4=32I, 6=64V.
- FLEX: Floating Point Exception fault enable.

  0= Set the C-Bit if exception.
  1= Take the fault.

TABLE 3-8: KEYS AND MODALS (Cont.)

- IEX: Integer Exception Fault enable.

  0= Set the C-Bit if exception.
  1= Take the fault.

- CCLT: Condition Code less than 0.

- CCEQ: Condition Code Equal to 0.

- DEX: Decimal Exception fault enable.

  0= Set the C-Bit if exception.
  1= Take the fault.

- IC: In CHECK - Check has been encountered. Check reporting is determined by MCM in "Modals".

- ID: In Dispatcher - Operation is in the Process Exchange dispatcher. Is set/cleared only by the Process Exchange u-code.

- SD: Save Done. If set, register save is done if in dispatcher (ID). Is set/cleared only by the Process Exchange u-code.

TABLE 3-9: MODALS

MODALS: (KEYS LOW) BITS															
1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
E	V	N	N	NOT				CRS			M	P	S	MCM	
N	I	O	I	USED							I	X	E		
B	M	V	N								O	M	G		
		L	D												
		P													

- ENB: Enable Interrupts.

- VIM: Vectored Interrupt Mode.

- NOVLP: Disable Prefetch Overlap (P750).

- NIND: Disable Indirect Overlap (P750).

- CRS: Current Reg. Set in use. It is set/cleared only by the Process Exchange u-code.

- MIO: Mapped I/O mode.

- PXM: Process Exchange mode.

- SEG: Segmentation mode.

- MCM: Machine Check mode.

TABLE 3-9: MODALS (Cont.)

0= Report no errors.
1= Report uncorrectable memory parity errors only.
2= Report all unrecovered errors (all but ECCC).
3= Report all errors.

TABLE 3-10: VCP REGISTER FILE MNEMONICS

MNEMONIC	REGISTER DESCRIPTION
A	Accumulator
B	Double-precision and long accumulator extension
DSWPARITY	Diagnostic Status Word Parity (750/850 only)
DSWPB	Diagnostic Status Word Procedure Base
DSWRMA	Diagnostic Status Word RMA
DSWSTAT	Diagnostic Status Word Status
DTAR0	Descriptor table address: segments 0 to '1777
DTAR1	Descriptor table address: segments '2000 to '3777
DTAR2	Descriptor table address: segments '4000 to '5777
DTAR3	Descriptor table address: segments '6000 to '7777
E	Accumulator exten. for MPL, DVL
FADDR	Fault address
FAR0	Field Address Register 0
FAR1	Field Address Register 1
FCODE	Fault Code
FLR0	Field Length Register 0
FLR1	Field Length Register 1
GR0	General Register 0
GR1	General Register 1
GR2	General Register 2
GR3	General Register 3
GR4	General Register 4
GR5	General Register 5
GR6	General Register 6
GR7	General Register 7
KEYS	Process status information
L	Combined A and B registers
LB	Link Base
MODALS	Process status information
OWNER	Address of PCB of process owning register contents
PB	Procedure base
PBSAVE	Saved return pointer when return pointer used elsewhere

TABLE 3-10: VCP REGISTER FILE MNEMONICS (Cont.)

MNEMONIC	REGISTER DESCRIPTION
PPA	Pointer to process A
PPB	Pointer to process B
PSWPB	Process Status Word Procedure Base
RECC1	ECC error register 1
RECC2	ECC error register 2
REOIV	Register End of Instruction Vector
RSAVPTR	Register Save Pointer: location of Register Save after Halt
RSGT1	Register Segmentation Trap: SWD2/Address of page map
RSGT2	Register Segmentation Trap: Contents of page map/DSW2
S	Stack
SB	Stack base
TIMER	1-millisecond process timer (used for time slice)
VSC	Visible shift counter
X	Index
XB	Temporary (auxiliary) base
Y	Alternate index

3.6.1.5.5 Memory Access Commands

- A <n> - Access address "n". The address may be followed by data display specifiers; "A 000004/000306 :O".

- A <register-name> - Access <register-name>. The current high-low mode determines which side of the register is modified. The name may be followed by data display specifiers.

  The access command may be followed by:

CR (Car. return)	Access next location.
↑ (Up-arrow)	Access previous location.
Number	Modify location to value of "number".
/ (Slash)	Exit and return to CP mode.

- C <start> <end> <to> - Copy the block beginning at <start> and ending at <end>, to the block beginning at the <to> address. Overlapping blocks, where <start><to><<end>, are not allowed.

- D <start> <end> - Dumps from <start> to <end>. Data display specifiers may follow (e.g., D 100 200 :H :O).

- D <register-name> - Dumps both high and low sides of "register-name". Data display specifiers may follow the name.

Long dumps may be terminated with a CONTROL-P.

- F <start> <end> <number> - Fill the block from <start" address to <end> address with <number>.

3.6.1.6 Accessing Physical (Unmapped) Memory

Master Clearing the system sets the CPU to 16S (sectored, real memory) addressing. If the system has not been cleared, access to physical memory is possible by setting the VCP's Memory Access mode.

```
CP> MO ABS
CP> A 1000 :O
     1000:  001004 /
CP>
```

3.6.1.7 Accessing Virtual (Mapped) Memory

The "MO MAP" command allows the CPU to access virtual memory (default). Virtual addresses (28 bit) are mapped through the CPU's Segment Table Lookaside Buffer (STLB) or tables located within memory itself. The tables will give the CPU the real (22 bit) address, which it will access and display.

1. Verify that the CPU is in segmentation mode. (See "Changing Processor Modes".)

```
CP> A MODALS
    XXXXXXXXXXXXXXXX /
```

2. Put the VCP in virtual accessing mode and access the address.

```
CP> MO MAP
CP> A 000004/100011 :O
    000004/100011: 00000012 cr
    000004/100012: 00110540 /
CP>
```

If no segment number is entered, the VCP uses the current segment. The real memory address is never displayed, only data from it or to it is displayed. If the virtual address is for a page not located in memory, the data display is unpredictable, since the CPU can not access the paging disk for the page.

3.6.1.8 Accessing Physical Register Files

Every 50 Series processor, except the 850, has 128 registers divided into 4 sets. Because the 850 has 2 CPUs, it has 256 registers divided into 8 sets. The four register sets are: RF0 (u-code scratch and system registers), RF1 (DMX), RF2 (Current Register Set), and RF3 (Current Register Set). The DMX register is 32 DMA channels. One Current Register Set (CRS) contains the keys and modals for the currently running or most recently run process. The other register set (Other Register Set) contains the keys and modals for some other process.

The high side, low side, or entire register can be dumped, depending on the mode of the VCP.

```
CP> MO RFABS
CP> D PPA
    000014/000032: 000011 000115 /
CF> MO RPH
CP> A PPA
    000014/000032: 000011 /
CP> MO RFL
CP> A PPA
    000014/000032: 000115 /
CP>
```

3.6.1.9 Accessing CRS Register Files

Current Register Sets (CRS) are based on logical addresses (see "CRS LOC ADR" column in Table 3-7). The CPU u-code converts the logical address to the correct physical address, depending on Modals bits 9-11 (see Table 3-9). Modals bit 9 is always 0 and bit 10 is always 1, so bit 11 actually determines the CRS. If Modals bit 11 is reset (0), CRS is RF2. If Modals bit 11 is set (1), CRS is RF3. For example, if PB (logical address '14) is accessed and Modals bit 11 is 0, physical address '114 is displayed. If PB is accessed and Modals bit 11 is 1, physical address '154 is displayed.

```
CP> MO RFCRS
CP> D KEYS :B
000014/000024: 1001100000100000
1100000001111111 /
CP> MO RFH
CP> A KEYS
000014/000024: 1001100000100000/
CP> MO RFL
CP> A KEYS
000014/000024: 1100000001111111/
CP>
```

3.6.1.10 Single-Stepping Instructions

"Single step" means executing a program in memory, one instruction at a time. Before starting, ensure that the proper Keys and Modals are set (see "Changing Processor Modes").

The registers and memory may be examined and modified freely between singe-steps, as long as the program counter is not altered. The current setting of the Keys and Modals in Current Register Set location 24 will take affect each time a step is executed. Interrupt and DMX operations are disabled in single-step mode.

3.6.1.11 Changing Processor Modes

"SYSCLR" resets (to 0) the CPU Keys and Modals and puts the CPU in 16S addressing mode. The Current Register Set is in location 24. The high side of the register (KEYSH) contains the "Keys" and the low side (KEYSL) contains the "Modals" (modes). Each time the CPU executes the fetch cycle of a new instruction, it sets its addressing modes according to the Keys and Modals settings.

Determine the appropriate bit settings using Tables 3-8 and 3-9. Then, to change the Keys settings:

```
CP> MO RFCRS
CP> A KEYS
CP> current setting new setting
    new setting /
CP> RCP address
```

To change the Modals settings:

```
CP> MO RFCRS
CP> A MODALS
CP> current setting new setting
    new setting /
CP> RCP address
```

The processor will execute the instruction in the address specified and set the CPU modes to those entered.

NOTE

DO NOT Master Clear the system after setting the Keys and Modals. "SYSCLR" puts the CPU in basic mode (16S) and resets all other modes.

3.6.1.12 Starting a Program (Placing it in "RUN")

Refer to "Booting the System" for another way to begin execution.

1. Enter "SYSCLR" if the machine must be initialized.

2. Set the program counter with the desired starting address.

```
CP> A RP
    current setting new setting
    new setting /
```

NOTE

"SYSCLR" leaves the program counter set to '1000.

3. Set any other registers or memory locations to their initial values.

```
CP> A register-name
    current value new value
    new value /

CP> A segno/wordno
    segno/wordno: value new value
    segno/wordno: new value /
```

4. Type "RUN", to start the program and put the VCP in ST mode. Type "RCP" to start the program and keep the VCP in CP mode.

3.6.1.13 Stopping Execution of a Program

1. Enter CP mode and stop the process.

```
ESC ESC
CP> STOP
```

2. Type "RUN" or "RCP" to continue execution of the program at the point of halt (provided you did not change the program counter).

3.6.1.14 Exiting Control Panel Mode

The following commands are used to exit CP mode:

- MO ST - Enters Supervisor Terminal (ST) mode from CP mode.
- MO ZCD - Enters the Z80 debugger. The debugger is a troubleshooting tool; this command should not be used by non-trained personnel.

3.6.2 SYSTEM TERMINAL (ST) MODE

This mode is the standard system (supervisor) terminal operation. After the system has successfully Master-cleared and a BOOT command is issued, the VCP awaits the standard PRIMOS commands. To exit from System Terminal Mode and enter CP mode, type ESC ESC.

3.6.3 ZCD MODE

ZCD mode is intended to be used ONLY by Prime hardware/software specialists or trained personnel to debug the VCP at the Repair Center.

3.7 MULTI-STREAM PROCESSOR MULTI/UNI OPERATION

The 850 processor is two 750 CPUs managed by a Stream Synchronization Unit (SSU) board. A set of DIP switches and four LED's are mounted on the rear of the SSU. Two of these switches control MULTI/UNI operation, and are duplicated on the front bezel panel of the system.

Switch #2 controls MULTI/UNI mode logic. When this switch is on, the system is forced into UNI mode (only one CPU operating). The active CPU is selected by switch #3. If switch #3 is off, the bottom CPU is active; if on, the top CPU is active.

Switch #4 selects the type of memory the SSU should respond as. If this switch is off, the SSU responds as an extended E6 memory which forces a short memory cycle on the system. The SSU may be debugged by a 750/850 CPU using APT1. To run in this mode switch #4 can be set, which forces the SSU to respond as an E6 memory.

Switch #5 should normally be off to allow normal operation or testing of the SSU. When this switch is on, the SSU is disabled and will not respond to any memory references.

Table 3-11 shows a summary of these switch settings.

TABLE 3-11: SSU SWITCH SETTINGS

FUNCTION	SWITCH SETTINGS 2	3	4	5
Normal, multi-mode	off	off	off	off
UNI0 (top CPU only)	on	on	off	off
UNI1 (bottom CPU only)	on	off	off	off
SSU debug on P850 (APT2 execution)	off	off	off	off
SSU debug on P750/850 (APT1 execution)	on	on	on	off
Disable SSU	xx	xx	xx	on

The four LEDs from left to right are: Parity error, MULTI mode, top CPU and bottom CPU.

If one of the CPU's is suspected to have component failure, the system can be reconfigured to run in UNI mode with only the good CPU.

To run in UNI mode:

1. Halt the system.
2. Set the MULTI/UNI switch (switch #3 or #4) for the CPU you wish to run.
3. Master Clear the system.
4. Cold Start PRIMOS.

The failing CPU may have to be removed from the backplane, depending on the type of failure. In ALL cases the SSU must be operational.

3.8 CHANGING I/O MASTERSHIP (MULTI-STREAM PROCESSOR)

The Master CPU (ISU-1) normally controls all system I/O functions. To switch I/O mastership to the Slave CPU (ISU-2), write '000015 into the CONTROL register at location '4/176400. Original mastership may be restored by writing a '000014 into the CONTROL register or master clearing the CPU.

NOTE

I/O mastership should only be changed when both CPU's are halted. Changing the CONTROL register at any other time may cause disturbing effects. I/O mastership should only be changed to allow the VCP to examine the Slave CPU. Multi-user PRIMOS will not operate in the event that I/O mastership has been changed in this manner. In order to bring up multi-user PRIMOS with the ISU-2 (Slave) as I/O master, the CPUs must be physically swapped.

Remember that under default conditions, the ISU-1 (top CPU) is the only ISU that will talk to the VCP. The SWITIO+ bit (#16) in the CONTROL register (AP_CTRL) was created to allow examination of the Slave's registers after a HALT. An example of swapping I/O mastership is listed below:

```
CP>SYSCLR

*** CPU VERIFIED ***

CP>A 4/176400
 000004/176400: 000014 000015
 000004/176401: 000000 /
CP>
```

I/O mastership has now been swapped to ISU-2 (Slave). To restore original ownership, either hit Master Clear or reset bit #16 of the AP_CTRL register in the following manner:

```
CP>A 4/176400
 000004/176400: 000015 000014
 000004/176401: 000000 /
CP>
```

3.9 CHANGING SUPERVISOR TERMINAL BAUD RATE

Master packs from the factory have the supervisor terminal baud rate set at 300 baud. This speed may not be desirable to the customer. In order to change the baud rate, three BOOT program parameters must be changed. These are the B- Register, X- Register, and KEYS, which appear following the PM command as:

```
OK, PM

SA,EA,P,A,B,X,K=
3011 5103 0 0 1010 76 34006
PB,SB,LB,XB=
64000/0 64000/170012 4000/21400 6/107203
```

They are defined as:

Word 0. Start address (SA= 3011)
Word 1. End address (EA= 5103)
Word 2. Program counter (PC= 0)
Word 3. A-reg. (A= 0)
Word 4. B-reg. (B= 1010)
Word 5. X-reg. (X= 76)
Word 6. Keys (Keys= 34006)

(All addresses are in octal.)

CHAPTER 4
PRINCIPLES OF OPERATION

4.1 INTRODUCTION

The operations of the 50 Series system are represented by the following major functional blocks:

- Central Processing Unit (CPU)
- Main Memory
- Chassis and Backplane
- Peripheral Controllers
- Communication Controllers
- Virtual Control Panel (VCP)
- Power Supplies
- Power Distribution Unit (PDU)

4.2 CENTRAL PROCESSOR UNIT (CPU)

Two and three board 50 Series Central Processing Units (CPUs) have the basic central processor logic implemented on an A and B board (Figures 4-1 and 4-2). The three board processors (P550-II, 500, 650) in addition to the A and B boards, have an extended instruction set (XIS) board with additional hardware implemented arithmetic functions (Figure 4-3). The 750 (Figure 4-4) is a five board processor made up of:

- A Board (execution unit): Performs the same functions as the A board in the two and three board processors. Includes microcode, register files, PIO logic, major data buses and ALUs.
- XIS Board: Expands the functions of the XIS board found in earlier processors. Contains ALUs for binary, decimal, fractional and exponential operations, plus a shifter to speed up arithmetic operations.
- C Board: Contains some of the same functions as the B board of earlier processors. Functions include, cache memory, Segment Table Lookaside Buffer (STLB), and memory timer.
- CS Board (Burst Mode Processor): Holds control store PROM which supplies microcode words to all boards.

  With wide-word memories and burst mode controllers, the burst mode processor performs four DMA transfers in the time it used to take to perform one transfer.

The baud rate parameters are:

SPEED	B- REG.	X- REG.	KEYS
110	110	27	74006
300	1010	76	34006
1200	2010	373	34006
9600	3410	3735	34006

NOTE

All parameters must be saved properly. It is possible that the Master Pack will have to be rebuilt, if parameters are entered incorrectly. To avoid this, it is a good policy to write the BOOT parameters on a piece of paper after doing the first PM. Then after the parameters have been changed and saved, do another PM to verify that the SA, EA, P, and A settings have not been changed. Do not halt the system until you are satisfied that the new parameters are correct. If they are incorrect, perform the following procedure.

3.10 CHANGING BAUD RATE OF BOOT

Three commands are used to change the parameters; RESTORE, SAVE and PM. RESTORE brings BOOT into memory, PM displays the parameters, SAVE saves BOOT back on disk. It will only be necessary to change three parameters, so a '4/' prior to the new parameters will start the changes at word 4 (1st parameter is 0). The following procedure will change the baud rate from 300 to 110:

```
OK, A MFD XXXXXX 0
OK, REST BOOT
OK, PM
SA,EA,P,A,B,X,K=
3011 5103 0 0 1010 76 34006
OK, SAVE BOOT 4/110 27 74006
OK,
```

3.11 T&MS

The 50 Series Test and Maintenance programs will be provided in a future update.

- J Board (prefetch unit): Contains the microcontrol unit and the Instruction Preprocessor Unit (IPU). The IPU looks ahead in the software instruction stream and fetches instructions from cache while the A board is executing microinstructions. The IPU decodes and forms the partial effective address of the next instruction to be executed by the A board. When the A board is finished executing, the J board may be able to initiate the microcode sequence to execute the next logical software instruction without the need for a microcode step to fetch the instruction.

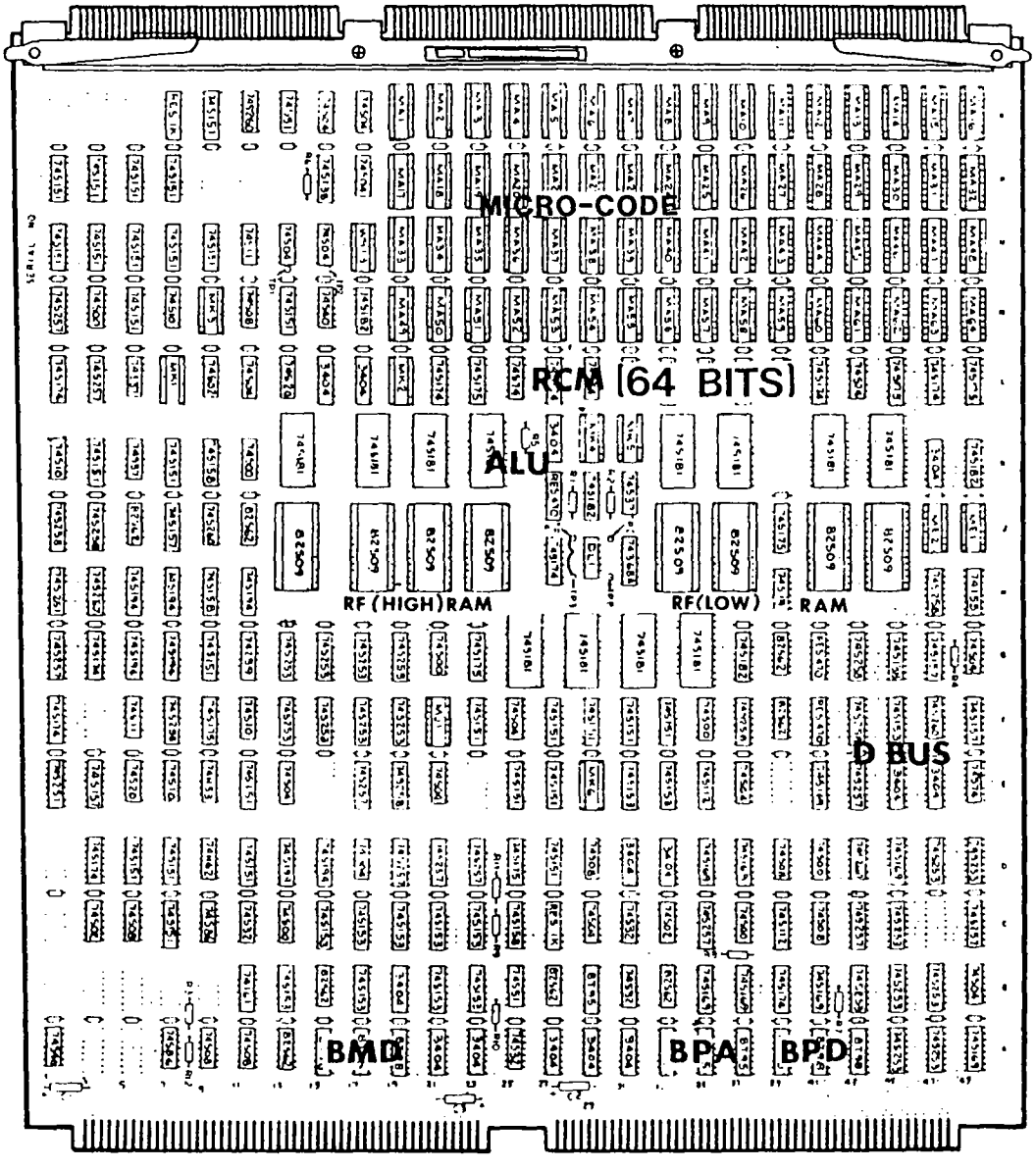


FIGURE 4-1: TWO AND THREE BOARD CPUS: A BOARD

The 850, multi-stream processor, contains two modified 750 CPUs and a Stream Synchronization Unit (SSU). The SSU coordinates the dual processor operation using the following instructions:

- Memory access synchronization
- Automatic cache invalidation
- Processor to processor communication
- I/O bus (stream) switching
- Diagnostic modes for debugging

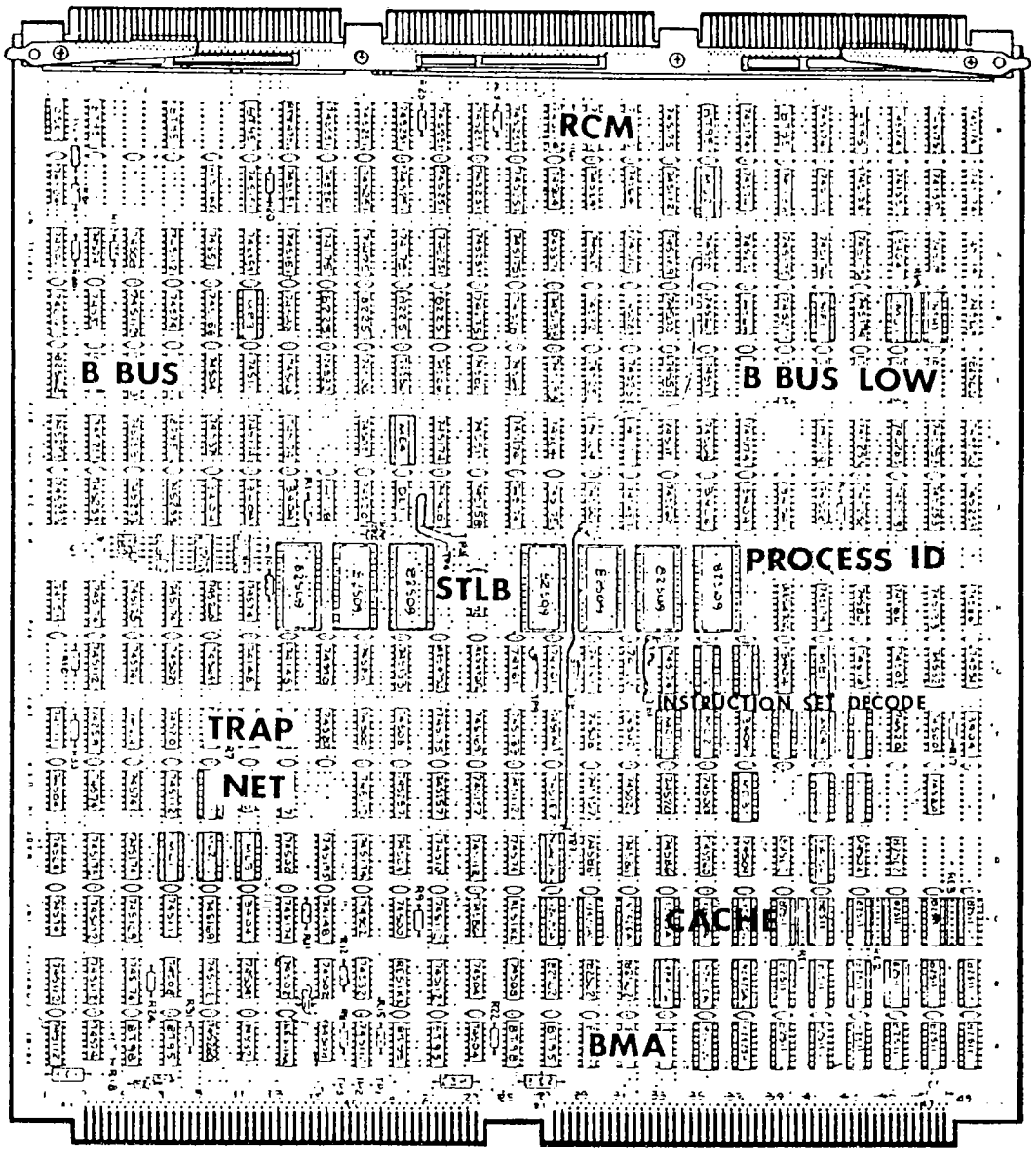


FIGURE 4-2: TWO AND THREE BOARD CPUS: B BOARD

The CPU boards are inserted into the backplane and connected by top hat connectors at the C, D, and E rear edge connectors (Figure 4-1). The top hats carry the internal CPU bus, timing, and miscellaneous signals between the CPU boards. External I/O and memory bus signals are carried over backplane connectors A and B.

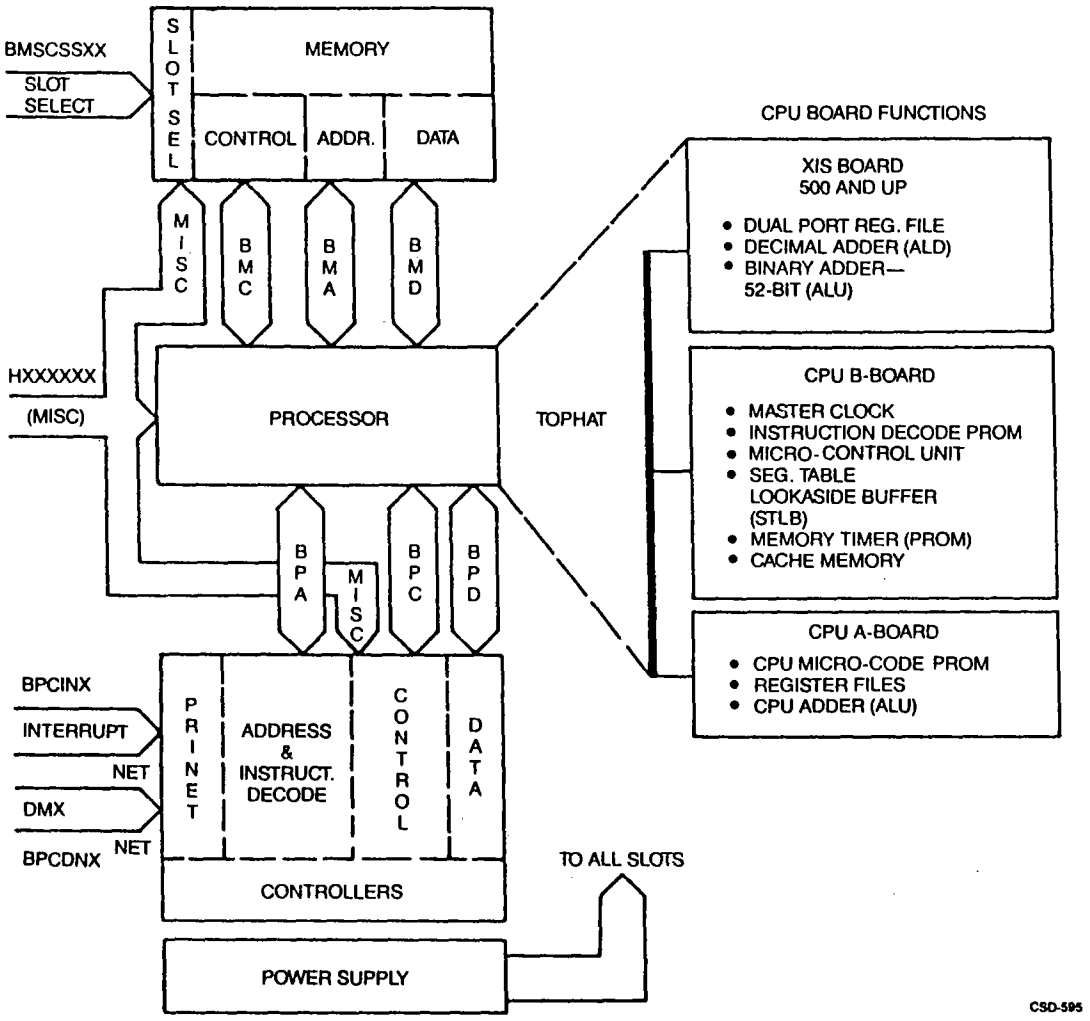


FIGURE 4-3: P550-II, 500, 650, SYSTEMS: CPU BLOCK DIAGRAM

Discussed in the next subsections is the following CPU information:

- Functional Description
- Timing and Control Unit
- Arithmetic Unit
- Memory Management
- Operating Modes
- Segment Table Lookaside Buffer (STLB)
- Cache Memory
- Refresh
- Processor Management

- Error Management
- Peripheral I/O Management
- Additional Processor Features

4.2.1 CPU FUNCTIONAL DESCRIPTION

The Prime CPU is a microprogrammed computer (Figure 4-5). The outer processor controls main memory, I/O logic and the Arithmetic Logic Unit (ALU). The inner processor controls the outer processor. This inner processor (or microcontrol unit) controls memory and I/O logic.

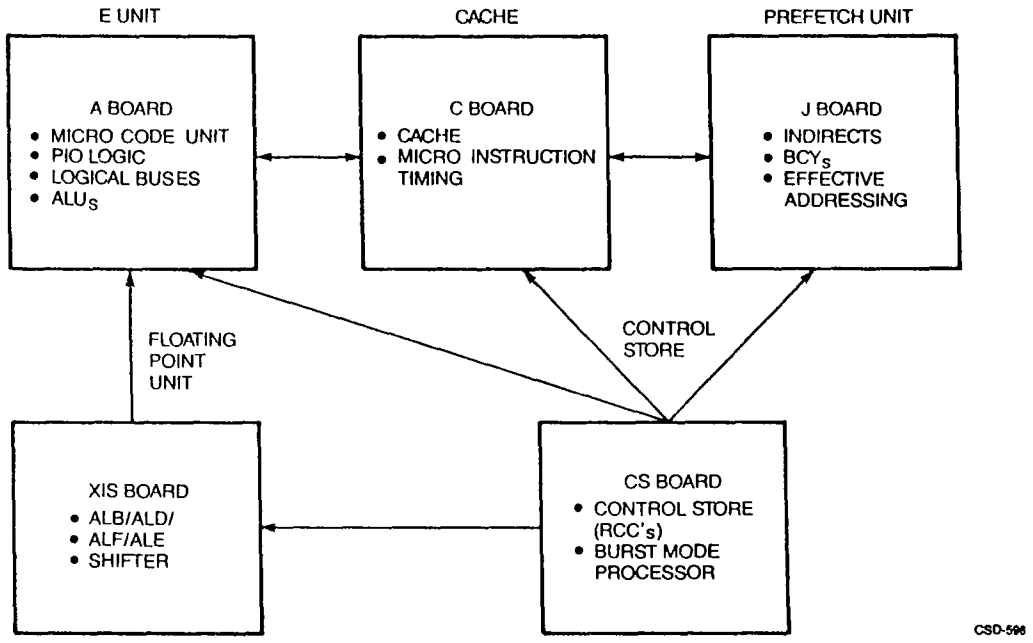


FIGURE 4-4: 750 CPU: FUNCTIONAL BLOCK DIAGRAM

For each instruction requested by the outer processor, the inner processor executes a series of microinstructions (microprogram). These outer processor functions include:

- Fetching user level instructions from memory
- Incrementing the program address register
- Executing the instruction

Microinstructions are stored in Read Only Memory (ROM). ROM, also called CPU microcode, is located on the A board (CS board on 750/850).

To achieve speed in executing user level instructions and to minimize random discrete logic, the PROM microinstruction word is 52 bits wide and is expandable to 64 bits. Each microinstruction is divided into 13 major fields. Each field controls a portion of the processor's operation. These fields are the inner processor's instruction set. Once the machine is master cleared, the inner processor is continually fetching and executing these instructions. When the machine is

stopped, the inner processor is still running, even if it is just scanning for a SYSCLR instruction.

The inner processor's control unit contains registers which keep track of the addresses of microinstructions that have been or will be executed. The Bused Control Unit Address Multiplexer (BCY) determines which register's address (microcode instruction) will be executed next. The BCY can interrupt normal microcode execution sequences in order to handle DMX, power fail, machine checks, and memory parity. Each time a microinstruction is executed, the Register Control Memory (RCM) is updated. RCM updates the outer processor. Microprocessor PROM (CPU microcode) may be expanded by using Writable Control Store PROM and RAM (750 CS board).

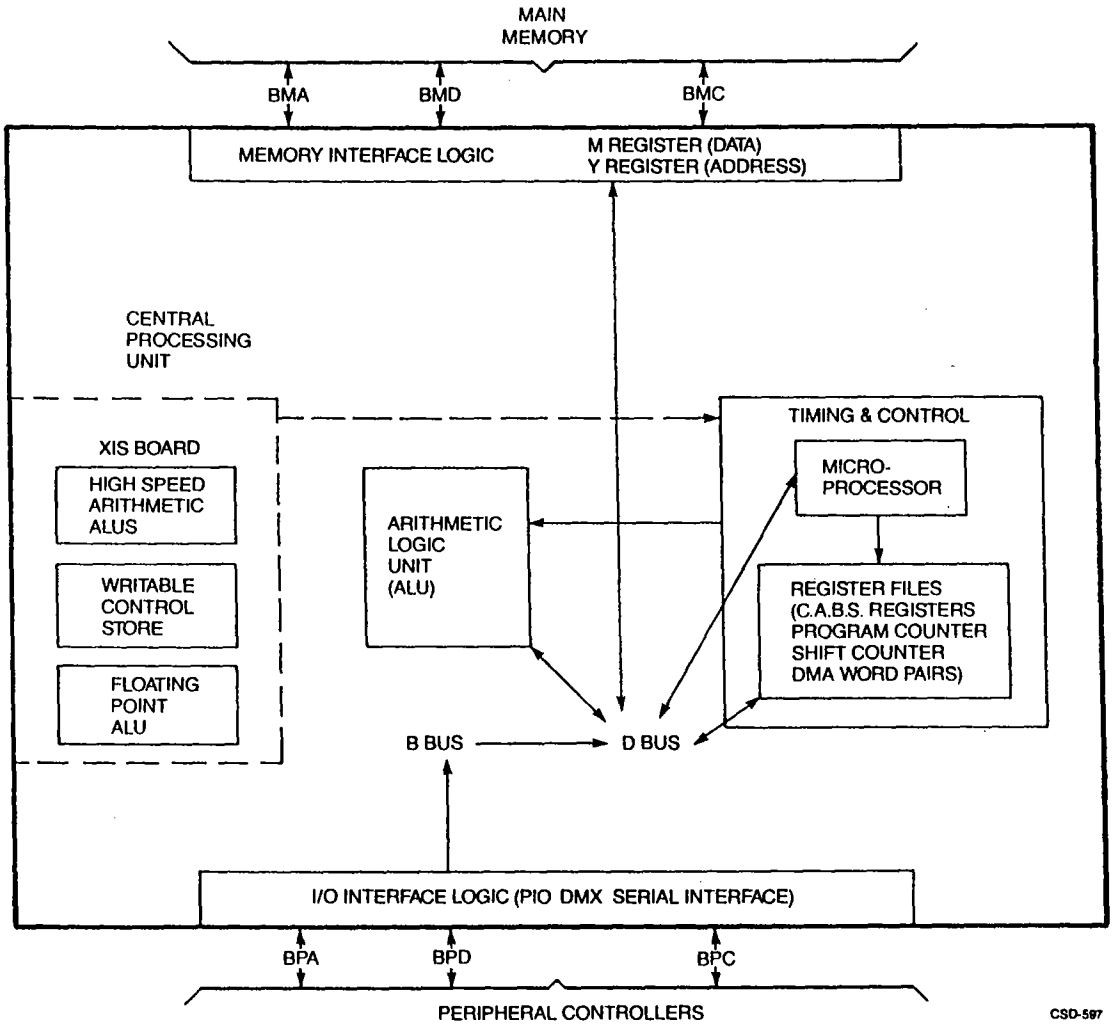


FIGURE 4-5: GENERAL CPU: FUNCTIONAL BLOCK DIAGRAM

4.2.2 TIMING AND CONTROL UNIT

The microprocessor interacts with a number of outer processor hardware control registers to form the control unit. The 128 32-bit register files, located on the A board, include: program counter (P Register), effective address register, and the memory address register. The D and B buses carry data between the control unit and memory and I/O.

Since nearly all control unit registers and buses are 32 bits wide, the CPU is considered to have 32-bit internal architecture.

Microprocessor logic is divided between the A and B board (A and C on the 750 and 850). Timing is developed from a 25 MHz oscillator on the B board (C) and is transferred to the other boards via the Top hat connectors.

4.2.3 ARITHMETIC UNIT

All arithmetic functions are performed using the ALU and the arithmetic or A register. The control unit moves data between memory and the A register via the D bus and the M register. Data can be moved between peripherals and the A register via the programmed I/O bus, D bus, and B bus. The B register serves as a right extension of the A register for double length operations. The C register (carry bit) is a single-bit register that is set on overflow in arithmetic operations. It is loaded with the last bit dropped out of the A or B register in shift operations.

In review, the control unit moves data to the ALU; instructs the ALU to operate arithmetically or logically on the data; then, instructs the ALU to store the result in the A register (and B and C registers if needed). The control unit can then store the result in memory, via the D bus and M register. Or, the control unit can fetch new data from memory to add to the contents of the A register.

Standard ALUs, capable of operating on 16-bit or 32-bit fields, are located on the A board. Additional ALUs for binary, decimal, fractional, and exponential operations are located on the XIS board.

4.2.4 MEMORY MANAGEMENT

The CPU has several memory management functions:

- Accesses memory in either absolute addressing mode (physical memory), or virtual addressing mode (segmented/paging).
- Manages CPU cache memory. Cache temporarily stores a section of main memory, to save time and reduce the number of accesses to main memory.
- Checks the integrity of memory addresses and data buses, in conjunction with the memories.
- Refreshes memory when specific locations are not in use.

4.2.5 OPERATING MODES

CPU operating modes determine how instruction op codes are interpreted and in turn, how memory addresses are formed. Sectored and relative operating modes are based on 16-bit internal registers and the concept of real memory divided into sectors, each 512 words long.

In sectored addressing (S mode), instructions access memory addresses directly. An instruction can access memory addresses in its own sector or in the first sector of memory (sector 0). An instruction located in sector 3, then, can access any location in sector 3

(addresses '2000 - '2777) or sector 0 (addresses '0000 - '0777). A machine that uses 16S mode can access the first 16k words of memory in this way; 32S means the machine can access the first 32K words in this manner.

Relative addressing (R mode) is an extension of S mode. Instructions can access memory addresses in sector 0 directly, as in S mode. In addition, instructions can access addresses in other sectors, based on 16-bit address codes stored in the program counter (P register). An instruction can access any memory address in any sector. In 64R mode a machine can access any address in the first 64K words of real memory.

Virtual (V mode) and Identity (I mode) addressing are based on the concept of segmented virtual memory, and 32-bit internal registers. In V mode, instructions reference 28-bit virtual memory addresses, instead of 22-bit real memory addresses. Instructions can access 64k words of virtual memory (8M' real memory) in 64V mode.

In I mode (32-bit Identity mode), each memory word is 32 bits, instead of 16 bits used in S, R, and V modes. Instructions can access the first 64K words of memory directly, plus 64K words of virtual memory (8Mb real memory).

4.2.5.1 Absolute Addressing

The CPU has many operating modes, but only two memory addressing modes. In absolute memory addressing mode, real memory addresses are generated by and for all program instructions. If the CPU is operating in S or R (sectored or relative) modes, only the first 64K words of real memory are addressable in the absolute memory accessing mode. However, 64V or 32I modes of operation, taking advantage of the CPU's 32-bit internal registers, may use all 22 real memory address bits (BMA95- BMA16) to access up to 4 million words of real memory (8 Mb).

4.2.5.2 Virtual (Segmented/Paging) Addressing

In this mode of memory accessing, memory addresses generated by and for the computer program are virtual. That is, the addresses do not point directly to physical memory.

Virtual memory is also called mapped memory. Prime divides virtual memory into segments. Think of the segments as chapters in a book. Some segments are shared by all users ('0000 to '3777) and contain PRIMOS, compilers, shared libraries, etc. The rest of the segments ('4000 to '7777) are divided between individual users.

Each segment (or chapter) contains up to 64 pages. Each page contains 1024 words (2Kbytes) and is equal to one physical disk record.

The 28-bit virtual address contains the segment number (12-bit), page number within the segment (6-bit), and the word number within the page (10-bit). Through a series of hardware and software mapping tables, the segment number and page number are translated into the 12-bit physical page number (PPN). Appending the PPN to the 10-bit virtual word number gives the 22-bit physical memory address, as illustrated in Figure 4-6. Once the physical address is determined, it can be

sent to memory on the Memory Address Bus (BMA) lines BMA95 - BMA16.

Virtual address translation would be unacceptably slow if the system had to access the tables every time it wanted to access a location in memory. To eliminate this bottleneck, the CPU has two high speed buffers to hold physical addresses and data. The address buffer is the STLB and the data buffer is cache.

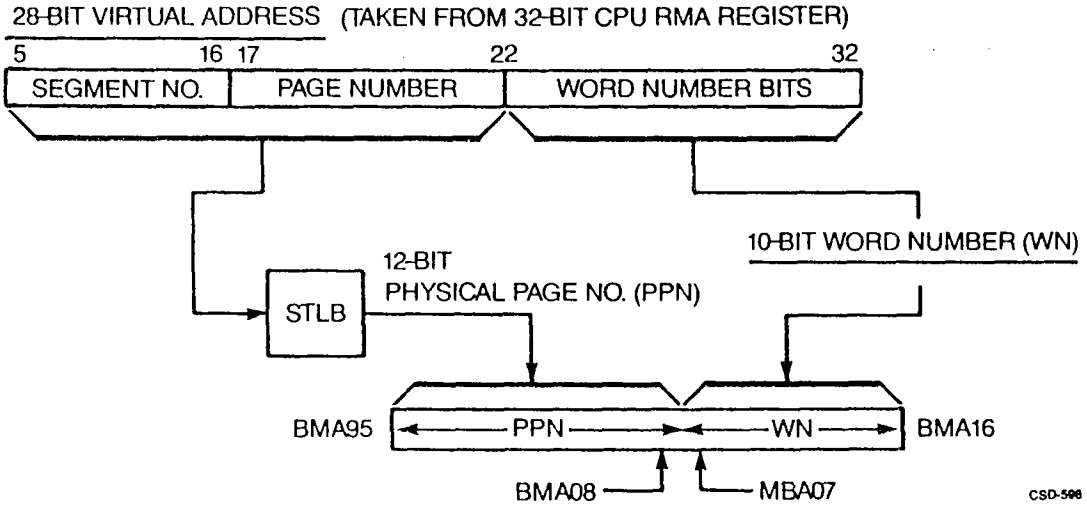


FIGURE 4-6: MEMORY ADDRESS TRANSLATION

4.2.6 SEGMENT TABLE LOOKASIDE BUFFER (STLB)

The Segment Table Lookaside Buffer is located on the CPU B board (C on 750/850). It contains memory addresses likely to be referenced by the processor. The segment number/page number pairs, and the PPNs of the last 64 virtual pages accessed, are stored in the STLB (see Figure 4-6). Because programs can use the same virtual addresses, the STLB index also contains the Process ID of the requesting process. That is, the STLB identifies the stored virtual/physical address pairs for a particular user's program.

When an instruction refers to memory, the CPU consults the STLB and compares the memory location referenced (current address) to the address in the STLB (last address referenced). If the addresses and the process ID match (STLB hit), the translated physical address in the STLB is output directly to the memory address bus.

If the addresses do not match (STLB miss), a segment trap takes place on the CPU. CPU microcode scans the segment and page tables in real memory to determine if the page is in memory. If the page is found in memory, the CPU loads the physical page number into the STLB, replacing what was previously in that STLB location. The microcode then restarts the instruction that caused the segment trap. The CPU again accesses the STLB. This time the STLB contains the correct page

number, so the CPU passes the translated address from the STLB to the memory address bus.

If the addresses do not match and the page is not found in memory the CPU microcode generates a page fault to the operating system. PRIMOS accesses the paging device and reads in the requested page. Then PRIMOS reexecutes the instruction that caused the page fault. The STLB is updated, the address is found on the STLB, and the address is passed on the memory bus.

A segment trap is generated if the STLB process ID does not match the user ID. The CPU microcode must access physical memory and update the STLB. This is because the translated physical address in the STLB refers to another user's data.

4.2.7 CACHE MEMORY

Cache, located on the CPU B board (C on 750/850), is a small amount of very fast memory which increases the effective speed of main memory. In a Prime 750 system, access to cache memory takes 80 nanoseconds. Access to main memory takes 600 nanoseconds. The system can do almost eight cache accesses in the time it takes to do one main memory access.

Since programs tend to access the same memory locations over and over, the system uses cache as an area to store data and instructions likely to be used by the processor. If the system can keep everything used by a program in cache instead of main memory, the program will execute much more rapidly. But because of the cost, cache memory is limited.

When a memory location is accessed, the contents are moved into cache in a specific location determined by the virtual address word number. Therefore, each access to that location in the future will find the information in cache, until the information is replaced by something else. As a further aid, information is always moved into cache in two word pairs, so any access to the other word of the pair will also be in cache.

Think of cache as a table of ordered pairs. Each cache entry consists of a physical page number (PPN), a piece of data and a validation bit. Sequential cache locations correspond to sequential physical word locations, so the seventh cache entry for PPN 12 is the seventh word on physical page 12.

4.2.7.1 CPU Cache Reads

All memory reads by the CPU are via cache. When an instruction refers to a memory location, the CPU microcode compares the virtual address word number to the corresponding location in cache. If the two match (cache hit), the data is passed from cache to the appropriate data bus. If the two do not match (cache miss), the CPU microcode generates a trap which causes the system to access the specified location in main memory. The CPU microcode loads the data from main memory into the correct cache location. Then the microcode restarts the interrupted instruction. Cache is accessed again and the correct data is output to the appropriate bus.

4.2.7.2 CPU Cache Writes

Whenever the CPU writes into memory it also checks cache. If the memory write location is also in cache, the CPU updates memory and cache simultaneously. If the location is not in cache, only memory is updated.

4.2.7.3 DMX Cache Cycles

Direct Memory Access (DMX) read cycles by peripheral devices do not reference cache. Peripheral controllers access main memory directly. However, DMX write cycles check cache. If the write location is in cache, CPU microcode sets an invalid bit in the cache entry, to indicate that the cache data is invalid. Since cache data is not updated during the DMX write, the next reference to that location will cause a microcode trap, so main memory can be referenced and cache updated.

4.2.7.4 Cache/STLB Summary

When an instruction references a memory location, the word number part of the reference is sent to cache and simultaneously, the segment number/page number part is sent to the STLB.

A cache hit and STLB miss means that the data is valid, but it belongs to someone else.

A cache miss and STLB hit means that the data is invalid, but the physical address is good. In this case the CPU must access real memory to obtain the correct data and update cache.

A cache miss and STLB miss means that both the data and address are invalid. In this case, the CPU must access real memory and update both cache and STLB.

4.2.8 REFRESH

Since Prime's main memory uses MOS technology, the memory chips must be accessed periodically, in order to maintain the neccessary electrical charge to represent 1's and 0's. This refreshing is done by the CPU. The memory chips specify a time of 2 microseconds before data can be lost. In order to meet this time limit, one part of each chip in the system is refreshed at a time. The refresh cycles are generated often enough (16 microseconds) so that by the end of 2 microseconds (for 16k chips) all parts of each chip are refreshed. The refresh addresses are produced by the CPU refresh counter and sent to the memory via address lines BMA10-16. The refresh memory cycle is requested just like any other memory task. Signal BMCRFSH initiates the refresh request on the memory board.

4.2.9 PROCESSOR MANAGEMENT

The CPU processes instructions in several different ways. So far, we have discussed sequential execution of instructions. Two other processing techniques, process exchange and procedure call, are part of the microcode.

4.2.9.1 Process Exchange

A process is an executing procedure, a logical continously executing sequence of code, such as a user program. Processes may be halted for indefinite lengths of time by interrupts, faults, and I/O transfers. When a process is halted, a microcode function called process exchange saves the state of the halted process, then schedules or activates a new one. Because process exchange is part of the microcode and not the software, the entire process exchange can take as little as 6 microseconds.

Process exchange has several elements. Each process has its own Process Control Block (PCB) which provides information about the process:

- Priority of this process
- Instruction to be executed next
- Register values
- Timer

The Ready List is the priority scheduler and dispatcher. The PCBs of all processes which are currently running or in queue to run, are on the Ready List. The Wait List keeps track of all processes which can be started only when some system condition is true. For example, an instruction may be on the Wait List until a DMX transfer or another instruction is completed. Once the system condition is true, the process is moved from the Wait List to the Ready List.

There are also four register sets. One set is microcode scratch, one is DMA channels, and two are user registers. The User Current Register Set (CRS) contains the register values for the currently running or most currently run process. The Other Register Set (ORS) contains the register values for some already run process. Think of the CRS as the active register set and the ORS as the inactive register set.

These process exchange elements work together as follows:

1. The microcode activates the highest priority PCB on the Ready List (Process A).
2. Process A's values are stored in the CRS.
3. When Process A is finished, the microcode stops the process.
4. The microcode checks to see if any PCBs on the Wait List may now be moved to the Ready List.
5. Any PCBs that can be, are moved.
6. Then the microcode activates the highest priority PCB on the Ready List (Process B) and switches register sets.
7. Values for Process B are stored in what was the ORS.

8. Process A's CRS has become the ORS (inactive register set) and its ORS has become Process B's CRS (active register set).

If Process A had not finished, but was interrupted because Process B had a higher priority:

1. The microcode:

   A) Stops Process A
   B) Checks the Wait List
   C) Switches register sets
   D) Starts Process B

2. Process A remains on the Ready List.

When Process B is finished:

1. The microcode:

   A) Stops the process
   B) Checks the Wait List and switches register sets

2 Process A, the highest priority PCB on the Ready List, is now resumed at the point of interrupt with its original register set intact. Process A's CRS becomes the ORS while Process B is running, then becomes the CRS when Process A is resumed.

4.2.9.2 Procedure Call

Procedure call allows processes to execute the same set of instructions (procedure) simultaneously. This set of instructions is often called shared reentrant code, since it is used by many processes.

Procedure call is a number of unrelated routines (calling procedures) which perform a certain subroutine (called procedure) as part of their tasks. It would waste space to have a copy of the subroutine within each of the main routines, so one copy is shared by all routines. Each routine performs specific tasks, executes the subroutine, and then performs more of its own tasks.

The called procedure contains an Entry Control Block (ECB). The called procedure's ECB contains:

- Information about the called procedure
- Its initial keys and register values
- Variables it will use
- Information necessary to perform stack segment management

Stack segment management is stored information about the calling procedure, such as the:

- Point-of-call in the calling procedure

- Calling procedure's keys and register values at point of call
- Variables shared by the calling and called procedures

When the microcode executes the Procedure Call Instruction (PCL), several things happen.

1. The microcode determines the called procedure's location in memory and verifies that the calling procedure has access rights to it.
2. The microcode allocates memory space (stack frame) for the called procedure.
3. The microcode stores the calling procedure's point of call, keys and register values, in the called procedure stack frame.
4. The microcode loads variables, keys and register values from the ECB into its registers.
5. The microcode stores the memory addresses of the called procedure's computation results in the called procedure stack frame.

Once the called procedure is executed, the microcode restarts the interrupted calling procedure. All keys, register values and computational results are reloaded from the stack frame.

4.2.10 ERROR MANAGEMENT

Error management for the 50 Series is provided by traps, faults, checks and interrupts. These means of error management are presented in detail in the next subsections.

4.2.10.1 Traps

Traps are breaks in microcode execution. Some, but not all traps, cause breaks in software execution (page not in memory, for example). There are two basic types of traps:

- G1 Traps - These traps are the direct result of a cache access. They are considered live, because the trap condition is detected and handled in the same microcode step.
- G2 Traps - These traps are used for static conditions and are generally caused by a preexisting machine condition.

When any trap condition is detected, the present microcode step is aborted and the trap logic causes a branch to the appropriate trap vector address. After the trap has been handled, the aborted step is usually reexecuted.

4.2.10.2 Faults

Faults are breaks in currently executing software, which must be serviced by the software. Faults are vectored through the software to microcode fault handler routines. These routines suspend current software operation, handle the fault and resume operation.

The following are three classes of faults defined by the CPU:

- Restricted Instruction
- Unimplemented Instruction
- Illegal Instruction

These three classes are described in detail in the following subsections.

4.2.10.2.1 Restricted Instruction

A restricted instruction is an op code which is not part of a user's access rights. For example, to execute instructions to halt the machine, change the CPU's operating mode, or shut down a disk drive, the user must have RING0 access rights. If an executing program contains an instruction outside of its access rights, a restricted instruction fault results. Restricted instructions are only found in systems with virtual memory.

4.2.10.2.2 Unimplemented Instruction

Unimplemented instructions are op codes defined, but not implemented in the CPU. These instructions are often hardware features on higher processors, implemented in software on lower processors (UII package). For example, multiplication and division were unimplemented instructions on the P100 and 200. An unimplemented instruction causes a fault to fetch the routine from software.

4.2.10.2.3 Illegal Instruction

An op code that is not implemented on any Prime processor is called an illegal instruction. Attempts to execute illegal instructions cause faults.

4.2.10.3 Checks

Checks are not caused by executing software. Instead they are processor execution errors. The microcode check handler stores the current value of the PB, KEYS and MODALS registers, then updates the diagnostic status word.

Checks discussed in this chapter are:

- Machine Checks
- Power Fail
- Memory Parity
- I/O Parity

4.2.10.3.1 Machine Checks

The Machine Check mode is determined by the last two bits of the MODALS, set with the microcode LPSW instruction. The four modes are:

00- NONE. The processor is not in an error reporting mode. Errors set a program testable flag but no check is signalled. The diagnostic status word is not set.

01- MEMORY PARITY. The processor sets the diagnostic status word and generates a check signal for all memory parity errors and all uncorrectable memory errors, during both instruction execution and DMX. Correctable memory errors are ignored and processor parity failures set a program testable flag in this mode.

10- QUIET. The processor sets the diagnostic status word and generates a check signal for all detected errors, other than correctable memory errors. Correctable memory errors are ignored in this mode.

11- RECORD. The processor sets the diagnostic status word and generates a check signal for all detected errors. In the case of a correctable memory error, the check signal is delayed until the instruction in progress is completed. This allows the software the option of resuming the computation following servicing of the check. Correctable memory errors which occur during DMX are always ignored, even in this mode, to allow the I/O transfer to complete successfully with the correction, whenever possible.

When the processor is in Quiet or Record modes, uncorrectable parity errors generate a Machine Check error and modify the diagnostic status word. In the other two modes, CPU parity errors do not cause Machine Check signals or set the diagnostic status word.

If the CPU is in Quiet or Record modes and detects a parity error on a processor internal register or an external bus (BMA, BMD, etc.), a machine check is generated and the diagnostic status word is set. If the CPU is in None or Memory Parity modes, a machine check is not generated and the diagnostic status word is not set. Instead, a program testable flag is set.

4.2.10.3.2 Power Fail

Power failures are detected by the hardware. The power supply produces signal PFL, the VCP in turn develops HPWRFL, and passes it to the backplane. The software has one millisecond to close all files, stop all I/O transfers, etc. before the power fail check causes the system to halt.

4.2.10.3.3 Memory Parity

Byte parity and error correcting memory are standard on all 50 Series processors. Main memory boards have an error detecting and correcting code on each memory word which is capable of correcting all single bit errors and detecting double bit errors. Correctable errors during DMX transfers are simply corrected and do not cause a check.

The following memory parity operations are discussed in this subsection:

- Write Parity Operation
- Read Parity Operation
- Memory Parity Checks

WRITE PARITY OPERATION

When the CPU is writing data to a location in memory, it generates byte parity on the data and the memory address. Data parity is sent to the memory on the BMDLP and BMDRP lines. Parity on the six high order bits of the address (BMA95-00) is generated and sent to the memory board as BMAAP. Parity on low order bits (BMA01-16) is generated and sent as lines BMALP and BMARP. The memory board then checks the parity on the address and data. If an error is detected, the memory board sends the appropriate parity error signal to the CPU: BMAPER, BMAPER, BMDPEL, or BMDPER.

READ PARITY OPERATION

The CPU also generates memory address parity whenever it reads data from memory. Data parity is generated by the memory board. The memory board generates parity and sends error signals to the CPU on the BMDLP and BMDRP lines. The CPU checks the parity on the received data. Error correcting memory corrects the error (if correctable), sends it as good data to the CPU, signals the CPU of the correction via signal BMDECCC (error correction cycle correctable). If the error is not correctable, memory notifies the CPU via signal BMDECCU (error correction cycle uncorrectable).

MEMORY PARITY CHECKS

The CPU generates a memory parity error check, if:

- Main memory parity check is detected during instruction execution when the CPU is in Memory Parity, Quiet or Record modes.
- Correctable main memory parity error is detected during instruction execution when the CPU is in Record mode.
- Main memory parity error is detected during DMX when the processor is in Memory Parity, Quiet or Record modes. Corrected I/O errors during DMX are always ignored, never set the diagnostic status word and never signal a check.

The error handling software routine sets the Machine Check Mode to None, performs the appropriate handling routine, clears the diagnostic status word, then returns control to the microprocessor.

4.2.10.3.4 I/O Parity

Just as the system generates parity on data transfers between the CPU and memory, it also generates parity on transfers between the CPU and the controllers. Parity is illustrated in Figure 4-7. Both output and input parity generation and checking operations are presented in the following paragraphs.

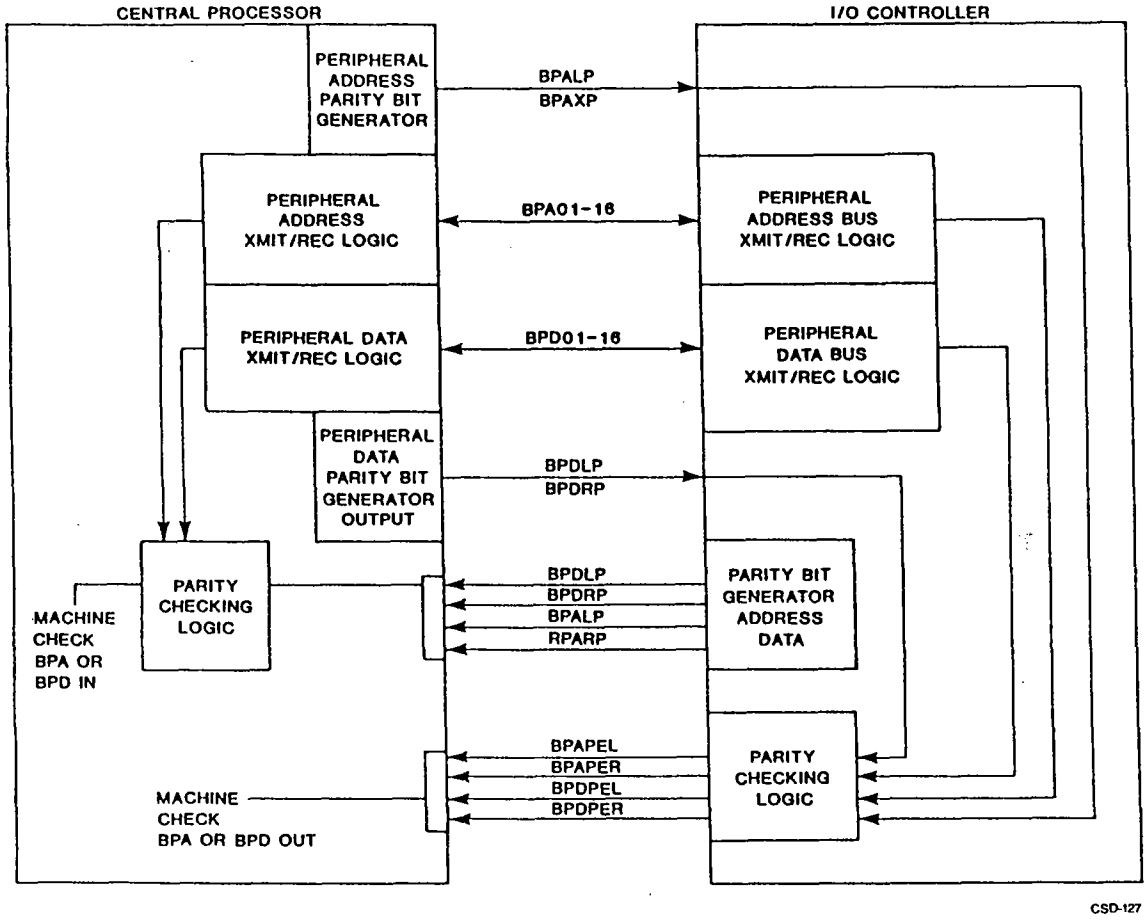


FIGURE 4-7: PARITY GENERATION AND CHECKING

OUTPUT PARITY GENERATION AND CHECKING

The CPU generates byte parity on each instruction it sends on the BPA. Signals BPALP and BPARP carry the parity. Each controller checks the BPA parity as it receives it. The CPU generates byte parity on each data word it sends on the BPD. Signals BPDLP and BPDRP are checked by the receiving controller. If bad parity is detected by the controller, it reports this to the CPU on lines BPAPEL, BPAPER, BPDPEL, or BPDPER (parity error left or right).

However, only the VCP can report an error on these lines, because all other controllers have these lines disabled. If the CPU senses one of the parity error lines from the VCP, a machine check error will occur if the CPU is in machine check mode 10 Quiet or 11 Record. If the CPU is in machine check mode 00 None or 01 Memory Parity, a program testable flag is set.

NOTE

All I/O controllers, except the VCP, must have BPAPEL, BPAPER, BPDPEL, and BPDPER lines disabled on them, due to a timing discrepancy between the CPU and the controller in reporting this error. The VCP is the only one with proper timing.

INPUT PARITY GENERATION AND CHECKING

The controller generates byte parity on each address it sends on the BPA. The CPU receives the parity as signals BPALP and BPARP, then checks it. The controller also generates byte parity on each data word it sends on the BPD. Signals BPDLP and BPDRP carry the parity to the CPU which checks it again. If the CPU detects bad parity, a machine check occurs, subject to the same conditions as above.

4.2.10.4 Interrupts

While the central processor is running a program, it monitors a signal (BPCIRQ) from the controllers in the backplane. When the signal goes true, the central processor is notified. The CPU interrupts its present job to service the controller. After servicing the controller, the processor returns to what it was doing.

When large amounts of data need to be transferred, a series of PIO instructions is sent to the controller to set up the operation. The controller then supervises the operation, requesting a DMX transfer as needed. This frees the processor to do other tasks. Interrupts inform the central processor when controller service is needed and when an operation is completed.

The following aspects of interrupts are discussed in the next subsections:

- Device Driver Programs
- Program Vectoring
- Interrupt Modes
- Interrupts in Process Exchange Mode
- Memory Increment Interrupts
- Interrupt Inhibits/Enables
- Override Inhibits
- Interrupt Priority Network
- Highest Priority Active Interrupt

4.2.10.4.1 Device Driver Programs

Each controller can perform a limited number of operations. For example, the disk controller can seek, read a record or write a record. The line printer controller, however, can only write data to a printer and control the line spacing. Each controller in the system

has a program associated with it, called a device driver. The device driver for the disk contains the PIO instructions for the controller to seek, read a record and write a record. The device driver for the line printer includes the PIO instructions that set up the controller to print a record.

Once the CPU sets up the controller to perform an I/O operation using the DMX channels for handling the data, the device driver can be invoked to complete the transfer. This means the CPU does not have to wait idly while the transfers take place. Instead, it can go back to its primary computations and wait for the controller to notify it that the transfer has been completed. The steps in the following example detail this process.

When a user does a SPOOL, PRIMOS invokes the disk driver to search the disk and get the record to be spooled. During setup, the CPU:

1. Gives the controller an instruction which contains the main memory location of the device driver program

2. Transfers control to that address.

When the driver has executed the instructions to initiate the transfer, the CPU goes back to servicing other users. When the disk controller completes the transfer, it interrupts. If another disk operation is pending, the CPU again executes the device driver program. If another disk operation is not pending, the CPU makes the controller available for use.

After the record is in the machine, the CPU invokes the line printer driver to let the line printer controller print the data. When the operation is complete, the printer controller interrupts.

PRIMOS supervises this ongoing process of invoking drivers and handling interrupts. As a device is to be used, its driver is executed to set up the operation. As the operation is completed, the controller interrupts to inform PRIMOS of its availability to do another task. Invoking a controller's device driver as a result of an interrupt is called Program Vectoring.

4.2.10.4.2 Program Vectoring

Program vectoring is the process of invoking a controller's device driver as the result of an interrupt. A simplified interrupt cycle can be described as follows:

1. The controller requests an interrupt and places the driver address on the address bus.

2. The processor vectors to the driver's address and a return address is stored in the DAC (Dedicated Address Cell).

3. The processor executes the driver to completion, then returns to the interrupted routine, using the return address stored in the DAC (JMP* DAC).

Figure 4-8 illustrates an example of interrupt program vectoring. A user's program had just finished executing the instruction at location '2041 when the disk controller interrupted. The central processor forms the starting address of the disk driver as '5010. The user program will be completed eventually, so the processor jumps to '5010, stores a return address there and starts executing the instruction in '5011.

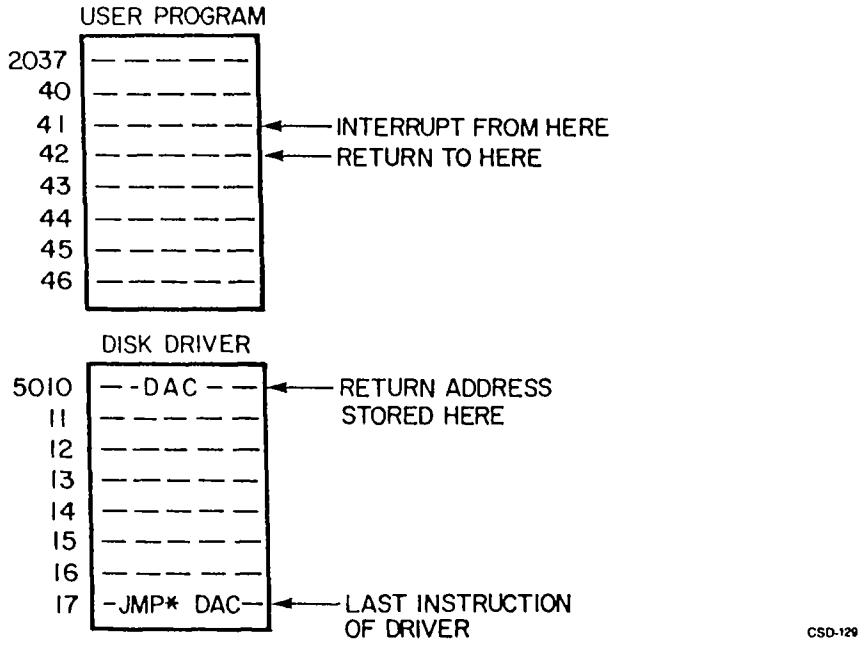


FIGURE 4-8: INTERRUPT PROGRAM NETWORK

Location '5010 is called a DAC or Dedicated Address Cell. When the driver has finished executing, the last instruction is a jump to the return address in the DAC. This is accomplished by JMP indirect through the DAC. The user program then resumes executing where it was interrupted.

4.2.10.4.3 Interrupt Modes

Software selects one of two interrupt modes for the CPU: standard or vectored. The mode is changed back and forth by the instructions ESIM (Enter Standard Interrupt Mode) and EVIM (Enter Vectored Interrupt Mode). The major difference between the two modes is how the processor determines the starting address of the controller's driver (where to vector to). Standard and vectored interrupt modes are discussed in detail below.

STANDARD INTERRUPT MODE

When the machine is master cleared, it is initialized to standard interrupt mode. In standard interrupt mode, location 63 of main memory holds a 16-bit pointer, which points to a software routine that determines which controller is interrupting. The software routine inhibits all subsequent interrupts, then determines the interrupting controller through a series of SKS instructions. Each controller has an SKS, if the controller is not interrupting.

The loop is similar to the following:

```
SKS IF URC NOT INTERRUPTING

JUMP TO URC device driver

SKS IF DISK IS NOT INTERRUPTING

JUMP TO disk driver
```

If the controller does not have an SKS, the processor jumps to the appropriate driver. An instruction must then be executed to enable interrupts again.

VECTORED INTERRUPT MODE

In this mode, the vectored address is not in location '63. Instead, the controller supplies the vectored address on the BPA. Each controller then may have its own pointer pointing to its own device driver.

The vectored address can be in one of two formats. Some controllers have vectored address registers, loaded by an OTA instruction. If no register is present, the vectored address is hard wired as the controller's device address plus '100. For example, a controller with a device address of '4 would have a vectored address of '104.

Just as in standard interrupt mode, all subsequent interrupts are inhibited until the device driver is finished and an interrupt enable instruction is given. In addition, the interrupting controller and all lower priority controllers are inhibited until the Clear Active Interrupt (CAI) instruction is issued.

4.2.10.4.4 Interrupts in Process Exchange Mode

If the CPU is in process exchange mode, neither standard nor vectored interrupt modes are used. As in vectored mode, the controller sends the vector address on the BPA. The vector address sent in process exchange mode is different than the one sent in vectored mode. First, the vector address refers to an address in segment 4, not segment 0. Second, the vector address is the address of the first driver instruction, not a pointer to the driver.

During a process exchange mode interrupt, execution is controlled by the microcode. All other interrupts are inhibited until the interrupt is completed and the driver issues the proper wait or notify instructions.

4.2.10.4.5 Memory Increment Interrupts

Memory increment interrupts are handled the same way for standard, vectored, or process-exchange mode. When the central processor responds to an interrupt, it examines mode line 2. If the line is a zero, a vectored or standard interrupt occurs. However, if it is a one, a memory increment is performed. This means the location pointed to by the vector address is incremented by one. If the location overflows from minus one to zero, a standard interrupt through

location '63 is performed. If the location doesn't overflow, the central processor returns to the task from which it was interrupted with no further action.

4.2.10.4.6 Interrupt Inhibits/Enables

Normally, interrupts are only allowed to happen when the central processor is enabled. Software instructions ENB (enable interrupts) and INH (inhibit interrupts) determine whether or not the CPU will respond to interrupts. When the machine is master cleared, interrupts are disabled. After this, interrupts are controlled by these two instructions, or in some cases, the CPU microcode (process exchange interrupts).

4.2.10.4.7 Override Inhibits

Certain interrupt functions must be implemented without waiting for the processor to be enabled. A special interrupt request line, when asserted, causes an interrupt regardless of whether or not the processor is enabled. Though generally not implemented, all controllers have this capability. At present, this function is used by the Real Time Clock (RTC on the VCP) which has to keep an accurate record of the time of day.

The RTC produces two types of interrupts: one to increment a memory location (location '61) to keep track of the time of day, and the other to interrupt the program flow when that location goes to zero. The RTC increments the memory location whether the CPU is in standard or vectored modes, but does not cause the JMP indirect. The other interrupt changes which user has control of the system.

4.2.10.4.8 Interrupt Priority Network

The interrupt priority network is a hardware mechanism used to prioritize the controllers. It consists of some logic on each of the individual controllers, connected by a backplane etch. When two or more controllers request an interrupt at the same time, the hardware in the priority network chooses which controller will be serviced. Priority is established by the physical position of the controllers in the backplane. The closer to the bottom of the configuration (slot 1), the higher the priority.

Five backplane signals are used to implement the PRIority NETwork (PRINET). They are noted in the lower right corner of Figure 4-9. The etch runs are actually angular, instead of vertical. In other words, the PRINET OUT signal (BPCIPNO) in slot one becomes PRINET A (BPCIPNA) in slot 2. It then becomes PRINET B in slot 3, PRINET C in slot 4, and terminates as PRINET D in slot 5. Each slot in the machine has a PRINET OUT line extending up the backplane for four slots. This means that the controller in slot 1 generates the interrupt lockout signals for the four slots above it in the backplane.

Any controller in slots 2 through 5 that senses the lockout signal regenerates that signal, passing the signal up four more slots in the backplane. Therefore, a controller requesting interrupt may lockout all lower priority controllers in the backplane, as long as there are no more than three empty slots between any two controllers. If there

are more than three empty slots, PRINET is broken and multiple requests may result.

In Figure 4-9, a controller is plugged into slots 4, 8 and 13. The controller in slot 4 has the highest priority, so it will get an interrupt if it requests one. The two input OR Gate senses the controller has been enabled to interrupt, so it sends the PRINET OUT signal (BPCIPNO) up the backplane. The controller in slot 8 in turn, does two things. First, the And Gate at the right is disabled, preventing the slot 8 controller from making a request. The signal also drives the slot 8 PRINET OUT signal low. This in turn propagates through the next four slots.

Because the controller in slot 13 is more than three slots away, it can never sense that a higher priority controller (slot 4) is already interrupting. The PRINET is broken. If the controller in slot 13 tries to interrupt at the same time as either of the other controllers, two controllers would be able to put vector addresses on the BPA. The result would be a parity error, causing the machine to halt. When the controller in slot 8 is interrupting, it prevents lower priority requests (slots 9 and up) from happening. Because higher priority controllers can't sense this (PRINET extends up the backplane, not down) they are allowed to interrupt at will.

4.2.10.4.9 Highest Priority Active Interrupt

Once a controller interrupts, any lower priority controllers are locked out until the higher priority interrupt has been cleared. When the central processor acknowledges an interrupt, it does two things. First the interrupt request is cleared from the backplane in a sequence known as Clearing the PRINET. Secondly, a flop on the highest priority interrupting controller is set. The flop drives the priority network low on all lower priority boards.

In standard-interrupt mode, the central processor clears the flop at the same time it clears the PRINET. There may be several highest priority flops set on the different controllers, when the Clear Flop instruction is issued. Only the controller that doesn't sense a higher interrupt is allowed to clear. The rest remain set.

In vectored and process-exchange modes, the device driver must issue a CAI instruction. The controller that doesn't sense a higher interrupt is allowed to clear. The rest remain set.

In vectored and process exchange modes, the device driver must issue a CAI instruction. Only the controller that doesn't sense a higher interrupt is allowed to clear. The rest remain set.

4.2.11 PERIPHERAL I/O MANAGEMENT

There are two types of peripheral I/O interface between the CPU and the system's I/O controllers. Programmed I/O (PIO) is used to transfer one data word at a time from the CPU to the controller. Multiple data words are transferred using DMX.

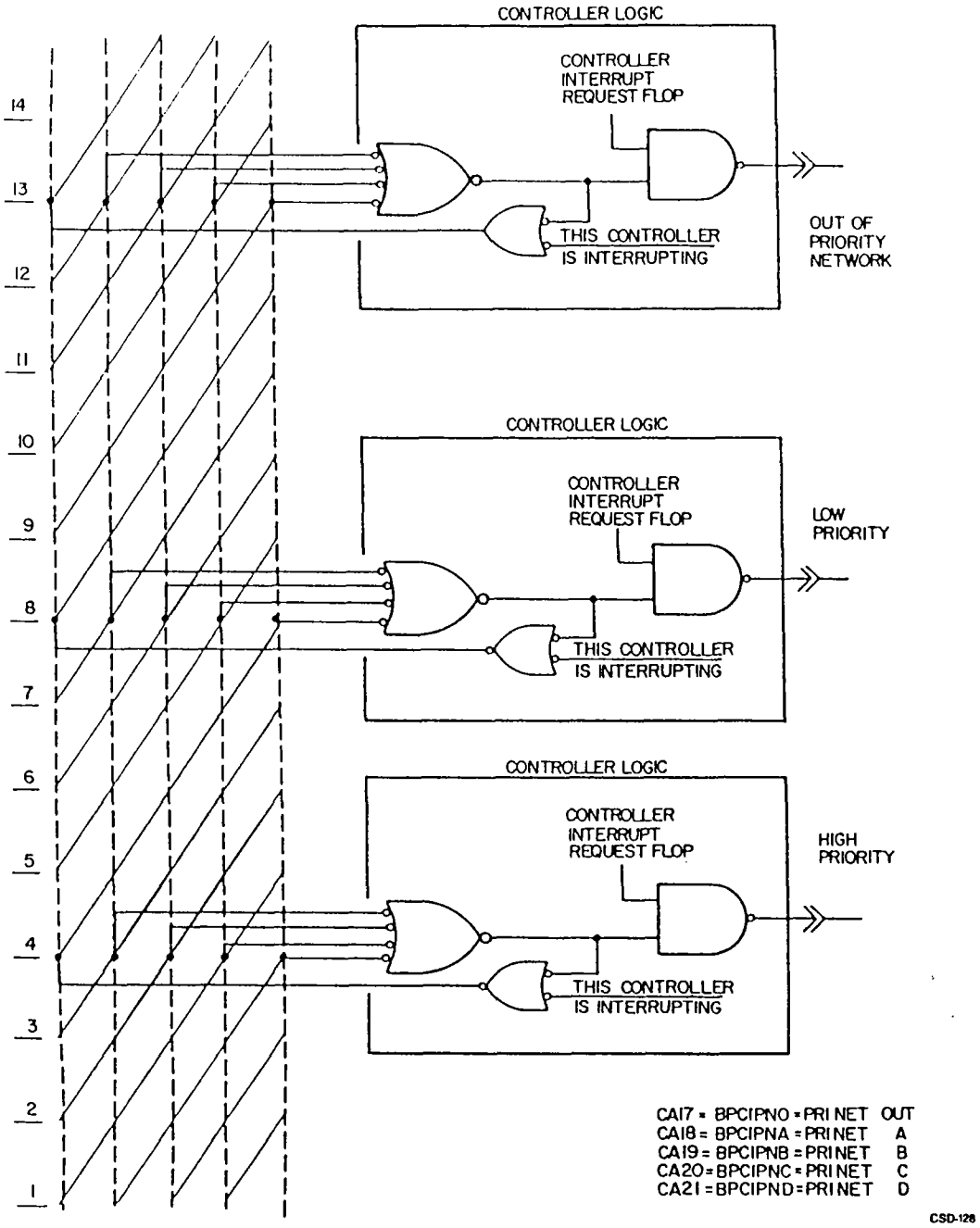


FIGURE 4-9: INTERRUPT PRIORITY NETWORK

4.2.11.1 Programmed I/O (PIO)

Data can be transferred to and from peripheral controllers with a set of software instructions called Programmed I/O (PIO). The data passed back and forth using these instructions can be either data or control words.

The PIO command has three parts (see Figure 4-10). The 6-bit op code identifies the type of transfer. The 4-bit function code further identifies what the controller is to do. The 6-bit device address identifies which controller will execute the transfer.

OP CODE	FUNCTION CODE	DEVICE ADDRESS
1 2 3 4 5 6	7 8 9 10	11 12 13 14 15 16

FIGURE 4-10: PIO INSTRUCTION FIELDS

The op codes, defined below, indicate what the controller is to do. The function code often specifies a certain device. If the PIO op code was OTA, the function code would identify the output destination (user terminal 1, 2, 3, or 4). For each type of op code, each controller has '20 (0- '17) possible function codes.

The PIO process is as follows:

1. The CPU places the entire 16-bit instruction directly from memory onto the BPA (Peripheral Address Bus).

2. The CPU asserts a control signal (BPCPIO, Enable PIO Mode) to inform all controllers in the backplane that there is a PIO instruction on the BPA.

3. The controller with the matching device address decodes the PIO op code and function code, then executes the instruction. All other controllers ignore the instruction.

PIO op codes in basic operating modes (16S, 32S, 32R, and 64R) are:

- OTA - Output data from CPU A Register to controller
- INA - Input data from controller to CPU A Register
- OCP - Command the controller to perform a function
- SKS - Test controller for a condition

PIO op code in the higher level operating modes (64V, and 32I) is: EIO. EIO encompasses all the above basic instructions into one, freeing up the I/O op codes for use as other instruction op codes in these modes.

4.2.11.1.1 Output/Input The A Register (OTA/INA)

OTA and INA PIO commands are quite similar. The OTA moves a data word from the A Register to a controller. The INA moves a data word from a controller to the A Register. The A Register is a high-speed register located in the central processor's high-speed register files.

For example, assume the program that the CPU is executing contains a command to output a character from memory to the teletype. The program would first move the character from memory to the A Register. Then, the CPU would send the OTA instruction to the controller on the BPA. The OTA's device address would be the device address of the teletype controller. The function code would be the code that instructs the controller to output the data word to the device. The CPU sends the character in the A Register to the controller on the BPD. The CPU sends the BPCPIO control signal on the BPC. All the controllers on the bus examine the device address of the instruction to see if it is theirs. The addresses controller accepts the information from the I/O Bus and instructs the teletype to print the character.

When an OTA or an INA is issued to a controller, the controller may not be ready to accept the command. To allow for such conditions, there is a control line (BPCREDY, controller ready) that tells the CPU whether the controller is ready to accept the command. If the controller is not ready, the CPU executes the next instruction in the program, without transferring the data. If the controller is ready, the CPU outputs the data and skips the next instruction in sequence.

It is common programming practice for the instruction following these commands to be a JUMP back. If the controller is not ready, the program re-executes the PIO command. If the controller can accept the data, the program is allowed to progress by skipping the JUMP back.

Once the instruction is decoded and accepted by the teletype controller, the character is sent through the controller to the device. If the operation is an INA, a data word is input to the CPU. The controller obtains the word from the teletype device and places it on the BPD. The CPU retrieves it and stores it in the A Register. The CPU then sends a strobe (BPCSTRB) to the controller indicating that the data has been received.

OTA and INA can be used to pass a variety of information between the CPU and the controllers depending on how the controller is designed to operate for the instruction being processed. When an OTA or an INA to device address '20 (Control Panel) is executed, the device is always ready, so the instruction never skips.

4.2.11.1.2 Skip On Condition Set (SKS)

The SKS instruction examines the controller's ready state, just like OTA/INA instructions. If the line is true, the program skips the next instruction. If the line is false, the program executes the next instruction.

Some controllers have more than one condition that may be tested by the SKS. When an SKS is executed on a controller, the function code portion of the instruction determines the specific condition to be tested.

4.2.11.1.3 Output Control Pulse (OCP)

The OCP differs from the other PIO instructions for two reasons:

- OCP forces the controller's ready line true
- OCP does not transfer any data to the controller.

The function code specifies some action to be taken by the controller. The controller accepts the command, regardless of whether it is busy or not. OCPs do not skip. An OCP causes a specific operation to be performed, such as initializing the controller or clearing a specific flip-flop.

4.2.11.2 Direct Memory Transfer (DMX)

Because peripheral controllers operate much slower than the CPU, PIO is very inefficient. If an OTA had to be issued every time a data word had to be transferred to a peripheral, the CPU would spend most of its time on I/O and never have time to perform other important operations, such as running user programs. To combat this problem, hardware was designed to automatically transfer data to and from peripheral controllers when the controller requests it. The CPU sends PIO instructions defining the operation to the controller. The controller then takes control of the operation. This process is called a "handshake". The CPU interrupts its normal operation and performs the transfer. Once the data transfer is complete, the CPU resumes its other tasks. The entire process of interrupting the CPU to perform a data transfer is called "Stealing a Cycle".

Another name for this data transfer process is DMX. DMX implies that data is transferred directly from the peripheral to memory, but this is not exactly true. No controller has control over the memory bus. As explained previously, normal CPU operation is momentarily suspended so the CPU can perform the memory transfer.

There are five types of DMX:

- Direct Memory Access (DMA)
- Direct Memory Transfer (DMT)
- Direct Memory Channel (DMC)
- Direct Memory Queue (DMQ)
- Burst Mode Direct Memory Access (BDMA)

The steps in the DMX process are:

- The controller sends control signal BPCDRQ (DMX cycle request) to the CPU on the BPC.

- The controller also sends the mode lines (BPCMOD0, BPCMOD1, BPCMOD2, BPCMOD3, BPCINMD).
  Mode lines is a five digit code which indicates the type of transfer (DMA, DMT, DMC, DMQ, BDMA) and whether the transfer will be to or from memory. Mode lines are illustrated in Table 4-1.

- The controller also sends the address lines (BPA01-16). Address lines indicate the number of words which will be transferred (word count), and the starting memory address of those words. Address lines are also called channel pairs.

The address lines are also used as counters by the CPU. Each time one word of data is transferred, the CPU decrements the word count and increments the starting memory address. When the word count equals zero, the transfer is complete.

The main difference between the five types of DMX transfers is where the CPU stores the address lines and how it interprets them.

TABLE 4-1: BPC MODE LINE SETTINGS

MODE	0	1	2	3	NMD	
DMA	0	1	0	0	A	A= data transfer direction: 1= into CPU 0= to contr.
DMC	1	1	0	0	A	
DMT	1	0	0	0	A	B= 1= clear A before INA 0= INA does logical OR of data to A
DMQ	0	0	0	0	A	
BDMA	0	1	0	1	A	
PIO	0	0	B	0	0	C= 1= RTC increment 0= interrupt
INTER-RUPT	0	0	C	0	0	

If the controller always uses DMA to write or read data, the mode lines can be hardwired on the controller. If the type of transfer can differ under program control, the CPU must load a mode line register on the controller with an OTA.

4.2.11.2.1 Direct Memory Access (DMA)

During a DMA transfer, word count and memory addresses are stored in the CPU high-speed register files. Two registers are required; one for the address, and one for the word count. Each set of registers is referred to as a channel pair. In a standard mode of operation, locations '20 to '37 of memory are used to implement 8 channel pairs. When the central processor accesses one of these locations it

automatically accesses its register files instead of memory. The address of the channel pair at '20 and '21 is '20.

Figure 4-11 shows the bit assignments for channel pairs. The even location holds the word count and is referred to as the range location.

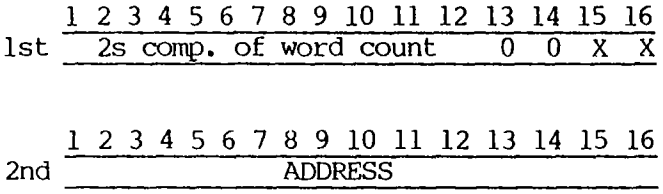


FIGURE 4-11: DMA CHANNEL PAIR FORMAT

The two's complement of the number of transfers is stored in bits one to twelve. Storing the word count in two's complement form allows both the word count and address to be incremented. This makes the transfer rate a little faster than if one were incremented and the other were decremented. Bits one to twelve get incremented. When 1 through 12 equal zero, the transfer is complete. Bits 13 and 14 are not used.

To set up a DMA transfer, the CPU sends the controller the address of the channel pair, the value of the mode lines, and whether the transfer will be input or output. This is done with PIO instructions. The CPU puts the address of the channel pair in the A register, then sends it to the controller with an OTA. The CPU sends a second OTA with the mode lines, if the controller is not hardwired to always perform the desired kind of transfer (see Figure 4-12). An OCP may be required to start the operation.

DMA INPUT

A DMA input (data goes from controller to memory) is accomplished by the following steps:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the address of the channel pair on the BPA. Because it is an input transfer, the controller also places the word to be transferred on the BPD.

4. The CPU determines from the mode lines that a DMA input transfer is to take place. It then uses the value on the BPA to address the appropriate channel pair.

5. Bits one to twelve of the range location are incremented and tested for a zero result. If they equal zero, the controller is informed with a control line that this will be the last transfer. If the incremented range bits do not equal zero, no action is taken; the incremented value is stored back into the range location.

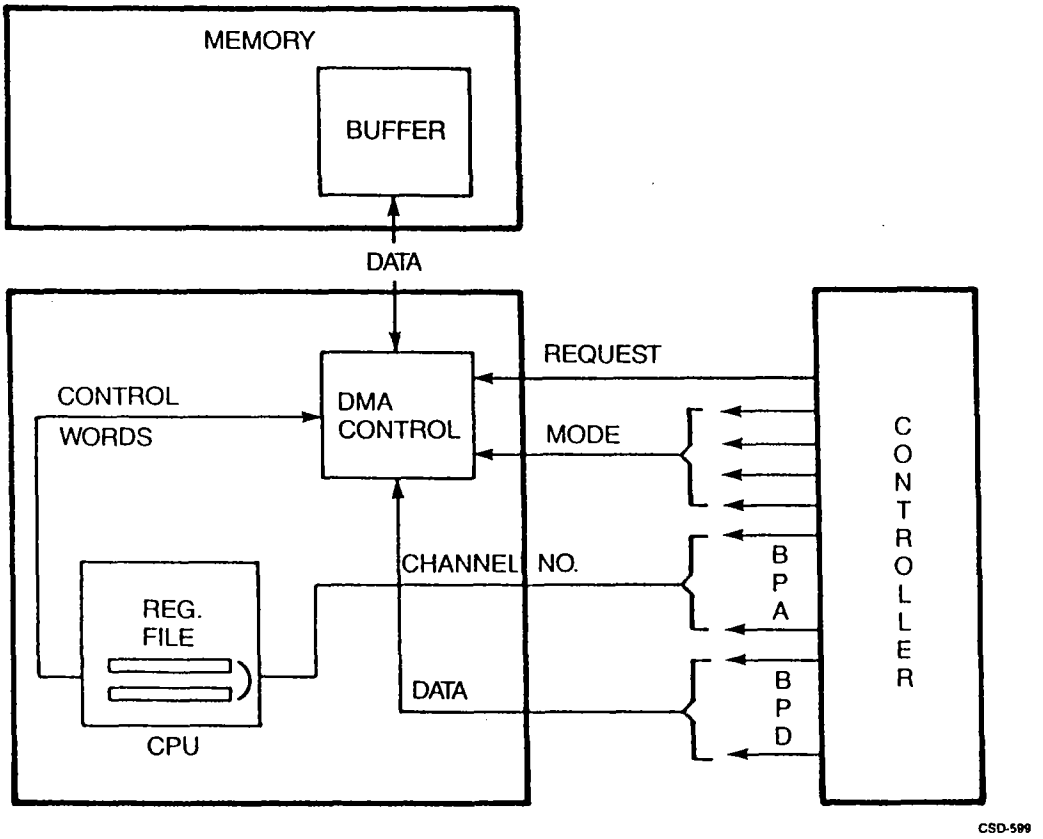


FIGURE 4-12: DMA TRANSFER

6. The CPU accesses the address location of the channel pair. These bits form the memory address (see Figure 4-11).

7. The CPU moves the data word on the BPD to the BMD, then initiates a memory write cycle.

8. The CPU increments the address (to point to the address of the next transfer), then restores it in the address location of the channel pair.

9. The CPU interrogates the BPC to determine if there are any more DMX transfers to be done. If so, it processes them. If not, it returns to the operation from which it was suspended.

DMA OUTPUT

A DMA output (data goes from memory to the controller) is accomplished as follows:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the address of the channel pair on the BPA.

4. The CPU determines from the mode lines that a DMA output transfer is to take place. It then uses the value on the BPA to address the appropriate channel pair.

5. Bits one to twelve of the range location are incremented and tested for a zero result. If they equal zero, the controller is informed with a control line that this will be the last transfer. If they do not equal zero, no action is taken; the incremented value is stored back into the range location.

6. The CPU accesses the address location of the channel pair. This location forms 16 bits of an 18 bit address (see Figure 4-11). Two flip/flops on the CPU are loaded from bits 15 and 16 of the range. The flops are then used to drive the extended memory address bits. The 18 bit address is placed on the memory address bus.

7. The CPU initiates a memory read of the just formed address. Then it moves the data to the BMD and then to the BPD. A control signal is asserted to indicate to the controller that the peripheral data bus holds a word for the controller to transfer to the peripheral device.

8. The CPU increments the address (to point to the address of the next transfer), then restores it in the address location of the channel pair.

9. The CPU interrogates the BPC to determine if there are any more DMX transfers to be done. If so, it processes them. If not, it returns to the operation from which it was suspended.

DMA HOG MODE TRANSFERS

Some controllers have the capability of requesting a group of transfers rather than just one. This is accomplished by simply leaving the DMX request on until the desired number of transfers has been completed. This is referred to as a "Hog Mode" transfer because the controller is "hogging" the bus.

4.2.11.2.2 Direct Memory Transfers (DMT)

With DMT transfers, word count and address information are maintained by the controller performing the transfer. That is, address and range information is stored in registers located on the controller. The setup for range and address is via OTA intructions to the controller. In some cases, the mode of operation can also be output by these OTAs.

Each time the controller does a transfer, it increments the address and word count. When the word count equals zero, the transfer is complete. DMT transfers are illustrated in Figure 4-13.

DMT INPUT

Because DMT does not have to access CPU registers, it is much faster than DMA. The memory address on the BPA indicates where the transfer will take place.

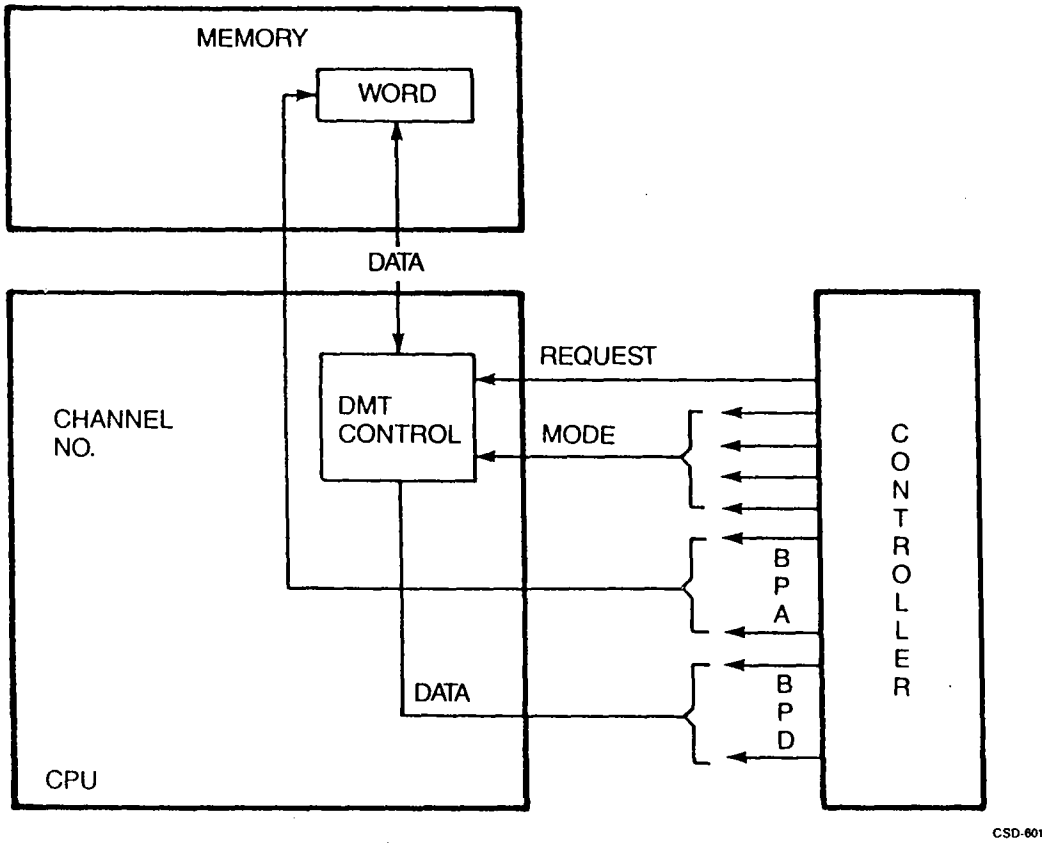


FIGURE 4-13: DMT TRANSFER

A DMT input transfer is done as follows:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the memory address where data is to be transferred, on the Peripheral Address Bus. Because this is an input transfer, the controller also places the data word to be transferred on the BPD.

4. The CPU determines from the mode lines that a DMT Input transfer is to be done. The CPU moves the value on the BPA to the BMA. It moves the data on the BPD to the BMD, then initiates a memory write.

5. The controller increments the address and range information stored in its registers and checks the range to see if any more transfers are to be done. If the range equals zero, the transfer is complete.

6. The CPU interrogates the BPC to determine if there are any more transfers to be done. If so, it processes them. If not, the CPU resumes its suspended operation.

DMT OUTPUT

A DMT output transfer is accomplished as follows:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the memory address where data is to be transferred from, on the Peripheral Address Bus. Because this is an output transfer, the controller will receive a data word from the BPD rather than supplying the Bus with a word.

4. The CPU determines from the mode lines that a DMT Output transfer is to be done. The CPU moves the value on the BPA to the BMA. It then starts a memory read to obtain the word to be transferred.

5. The CPU places the word just retrieved from memory, onto the BPD and asserts a Peripheral Control signal to inform the controller to accept the word. The controller accepts the word and writes it to the device.

6. The controller increments the address and range information stored in its registers, then checks the range to see if any more transfers are to be done. If the range equals zero, the transfer is complete.

7. The CPU interrogates the BPC to determine if there are any more transfers to be done. If so, it processes them. If not, the CPU resumes its suspended operation.

4.2.11.2.3 Direct Memory Channel (DMC)

During a DMC transfer, word count and address information is stored in memory locations. This requires two memory locations, starting with an even address. These two locations form a DMC channel pair, illustrated in Figure 4-14.

The first location of the pair holds the starting address of the transfer. The second location holds the address of the last transfer to be done. The channel address must fall between '40 and '3776. The transfer must be from within a 64K word boundary.

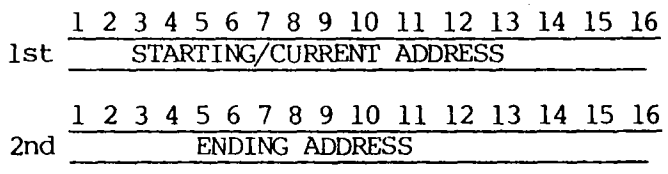


FIGURE 4-14: DMC CHANNEL PAIR FORMAT

DMC INPUT

A DMC input transfer is performed in the following manner:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the address of the DMC channel pair on the BPA. Because it is an input transfer, the controller also places the word to be transferred on the BPD.

4. The CPU determines from the mode lines that a DMC input transfer is to take place. The data from the first word of the pair becomes the address of the transfer; it is placed on the BMA. The CPU moves the word on the BPD on to the BMD and initiates a write to memory.

5. The CPU increments the first word of the channel pair and restores it back into memory. Then, the CPU accesses the second word of the channel pair and compares it to the first word of the pair. If they are equal, the transfer is complete; the CPU asserts a control line to indicate to the controller that the transfer is complete. If the locations are not equal, no action is taken.

6. The CPU interrogates the BPC to determine if there are any more DMX transfers to be done. If so, it processes them. If not, it returns to what it was doing.

DMC OUTPUT

A DMC output transfer is performed as follows:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the address of the DMC channel pair on the BPA.

4. The CPU determines from the mode lines that a DMC output transfer is to take place. The processor moves the address from the BPA to the BMA and initiates a read of the location.

5. The CPU places the data from the first word of the pair on to the BMA. (The first word becomes the address of the transfer.) The CPU then retrieves the word from memory and places it on the BPD. Next, the processor asserts a control line to inform the controller the word is on the bus and can be retrieved. The controller accepts the word and writes it to the peripheral device.

6. The CPU increments the first word of the channel pair and restores it back into memory. Then the processor accesses the second word of the pair and compares it to the first word. If the words are equal, the transfer is complete; the CPU asserts a control line to indicate to the controller that the transfer is complete. If the locations are not equal, no action is taken.

7. The CPU interrogates the BPC to determine if there are any more DMX transfers to be done. If so, it processes them. If not, it returns to what it was doing.

The DMC transfer is illustrated in Figure 4-15.

4.2.11.2.4 Direct Memory Queue (DMQ)

DMQ allows large amounts of data to be transferred without software intervention for each character (see Figure 4-16). To do this, DMQ stores data in a buffer in CPU memory. The CPU DMQ logic (microcode) updates the data in the buffer's control block at the same time as data is transmitted from the buffer by the AMLC. In this way, the entire output buffer is transmitted without intervention from the CPU.

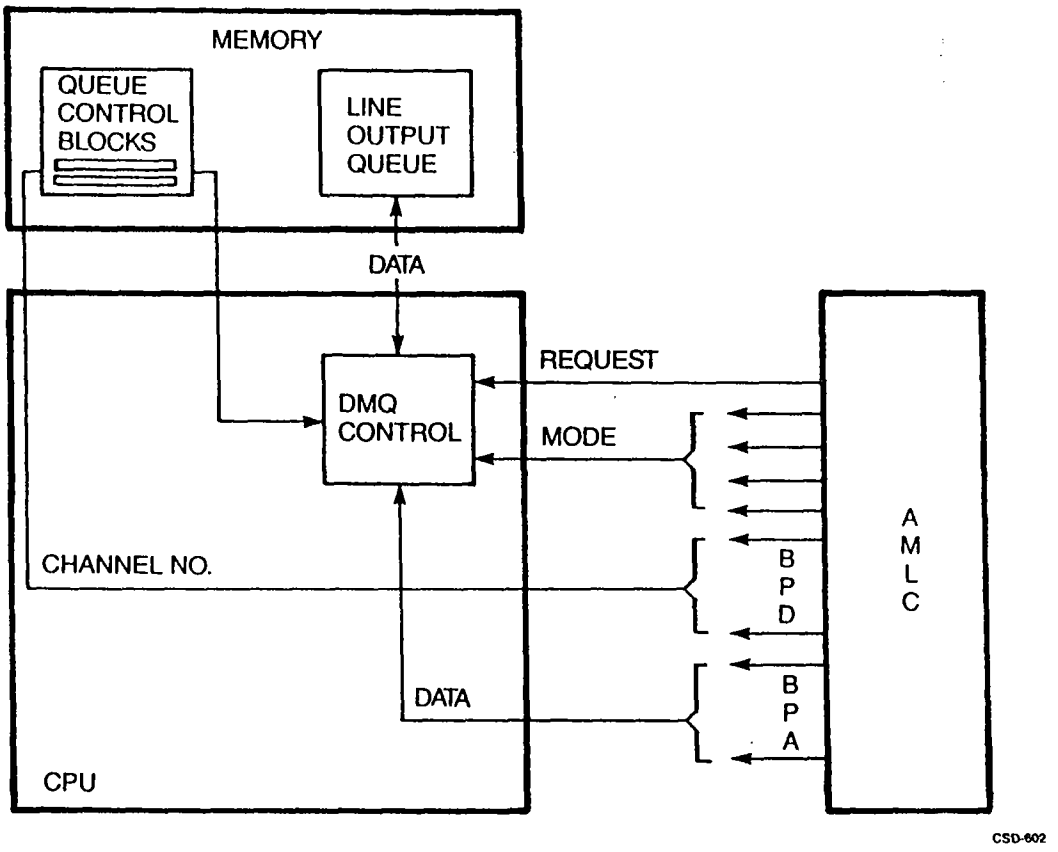


FIGURE 4-15: DMC TRANSFER

The Queue Control Block is a special group of memory locations that indicates the size and location of the buffer. It operates like a FIFO (first in first out) buffer; the CPU writes data to the buffer and the controller removes it. The Queue Control Block contains the segment where the buffer is located, the length of the buffer and the top and bottom pointers.

The Top-of-Queue Pointer contains the next buffer address of the data the controller will read. The controller references this pointer, fetches the data from the buffer and transfers it to the peripheral. The Bottom-of-Queue Pointer contains the next buffer address where the CPU will write data. The CPU fetches data from memory, references this pointer, and writes the data to the proper location in the buffer.

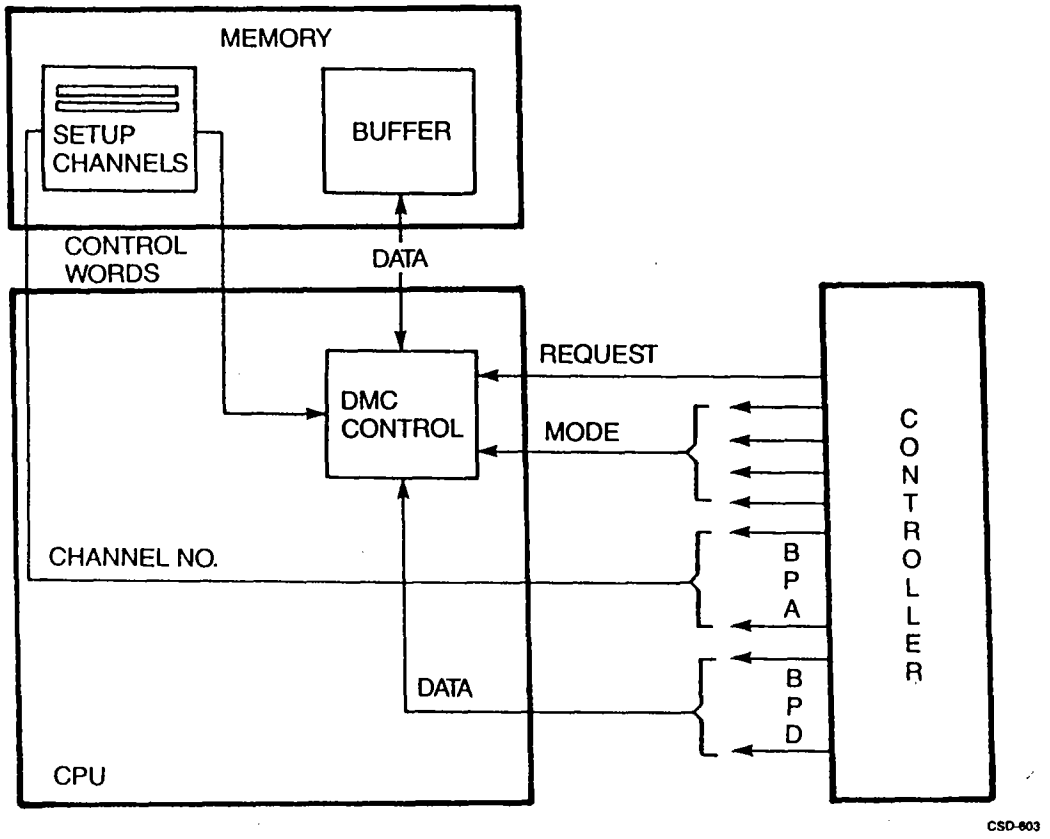


FIGURE 4-16: DMQ TRANSFER

The Mask indicates the length of the buffer. Consider a buffer '100 locations long (addresses '3000 to '3077). Each bit of the mask allows the corresponding address bit to be active within the buffer area, i.e., the mask for a buffer from '3000 to '3077 would be '77. By appending the mask bits to the start address, the buffer is limited to a high location of '3077. When the CPU reaches the bottom of the buffer and tries to address the next higher location ('3077 + 1 = '3100), the 1 falls outside the mask and is lost. Hence the next location to be addressed will be '3000.

DMQ is only used for output to AMLCs. Each AMLC line has a Queue Control Block and buffer located in memory.

A DMQ output transfer is accomplished as follows:

1. The controller requests a transfer.

2. The CPU acknowledges the request.

3. The controller places the mode lines on the BPC and the DMX memory address where data is to be transferred from, on the BPA. Because this is an output transfer, the controller will receive a data word from the BPD rather than supplying the Bus with a word.

4. The CPU determines from the mode lines that a DMQ Output transfer is to be done. The CPU microcode uses the DMQ address to access the first location in the Queue Control Block. This first

location is the Top-of-Queue Pointer. The CPU compares the Top-of-Queue Pointer with the Bottom-of-Queue Pointer. If they are equal, the buffer is empty and the transfer is complete.

5. The CPU retrieves the data word specified by the Top-of-Queue Pointer, places it on to the BPD and asserts a Peripheral Control signal to inform the controller to accept the word. The controller accepts the word and writes it to the device.

6. The CPU increments the Top-of-Queue Pointer and keeps its address within the bounds of the Mask. The CPU again compares the pointers. If they are not equal, the CPU outputs the next location to the BPD. If they are equal, the transfer is complete.

7. The CPU interrogates the BPC to determine if there are any more transfers to be done. If so, it processes them. If not, the CPU resumes its suspended operation.

4.2.11.2.5 Burst Mode DMA (BDMA)

During burst mode, the CPU sends a group of words over the I/O bus in a burst, instead of sending a single word. Burst mode requires 750/850 CPU, interleaved wide-word memories and a controller with burst mode logic. Burst mode utilizes the P750's ability to transfer four words of data to or from memory with a single memory access. This difference in CPU microcode is the only difference between BMDMA and standard DMA. Part of the burst mode microcode utilizes a FIFO (first in first out) buffer.

Once the central processor has determined a burst mode request is present, the CPU microcode verifies that:

1. The central processor is a P750/850.

2. There are at least two E6 memories in the system. They must be in wide-word mode with interleaving turned on.

3. There are at least four words remaining to be transferred, before an end-of-range condition is encountered. This is determined by checking the range location of the DMA channel pair.

4. The starting address for the transfer is on a zero module 4 boundary. This is determined by checking the address location of the DMA channel pair. Bits 15 and 16 of the address must be zero. If this requirement is not met, the wide-word memories will not be able to perform the required wide-word interleaved memory access.

Once the above criteria has been met, the CPU brings up BPC Strobe (connector B pin 95). Then it creates four burst strobe signals (connector A pin 41).

BURST MODE INPUT

During burst mode input transfers, four 16 bit words are transferred from the FIFO into main memory. As a burst strobe is received, a word is unloaded from stage 4 of the FIFO and placed on the BPD. It is then latched into one of the four intermediate registers located on the CS Board of the P750/850. The first word goes in register one.

The second word goes into register three. The third word goes into register two, and the fourth word goes into register four.

As soon as the first word of the transfer is latched onto the P750, a wide-word interleaved write cycle is started. Register one is sent to the first memory board of the pair, over the BMD. Register three is sent to the second memory board, over the BMA. Register two is then sent to the first board, and register four is sent to the second board. All this is done automatically as a part of the wide-word cycle.

BURST MODE OUTPUT

The output transfer is simply the input process reversed. A wide-word interleaved read cycle is started. The CPU takes the first word from the BMD and places it in register one. The second word from the BMA is placed in register three. The third word is then placed in register two, and the fourth word is placed in register four.

As soon as the first word is latched into register one, burst strobes are started. Register one is gated onto the BPD, where the first burst strobe causes it to be latched into the write register. The contents of the write register are then stored in the FIFO. Register three is then transferred in the same manner. Registers two and four then follow.

Burst mode controllers can handle both burst mode and normal DMA transfers. If the CPU determines that there are not at least four words left to transfer, or the address is not on an even boundary of four, burst mode cannot be used. Instead, normal DMA transfers are used until the boundary lines up, or end of range is encountered.

When requests are made, the controller's DMA logic assumes the transfer will be a normal DMA Cycle.

As soon as the controller detects a burst strobe, the DMA logic is initialized and placed in burst mode. From this point, until the FIFO is almost empty, Burst Mode is performed. The DMA logic counts 4 address phases (4 burst mode cycles), during which 16 words are transferred. This process continues until only 16 words are left to be transferred.

When only 16 words are left to be transferred, the DMA logic enters Clean Up Phase. During Clean Up, normal DMA transfers are executed.

In summary, the controller requests BMDMA. The CPU determines that BMDMA cannot be done, so normal DMA begins. Once BMDMA conditions are met, the CPU sends a Burst Strobe to the controller. The controller slips into Burst Mode and transfers most of the data. Then, the controller returns to normal DMA mode and transfers the last 16 data words.

4.2.11.2.6 DMX Priority Network

Priority networks are used to arbitrate simultaneous requests for system resources. If two controllers request a transfer at the same time, the priority network causes the board with highest priority to perform the transfer first. Priority is established by the physical

position of the board in the backplane (see Figure 4-17). The closer to the top of the configuration the board is placed, the lower the priority it has (i.e., slot 2 has higher priority than slot 4; 4 has higher priority than slot 6).

Whenever a controller requests a transfer, it sets a flip-flop. The flip flop in turn, drives a BPC signal that is connected by the backplane to any and all controllers located above the requesting board. This signal locks out any lower priority boards from requesting a transfer. When a controller wants to request a transfer, it first interrogates this control signal, to determine if a controller with higher priority is already making a request. If so, the controller waits until the signal is no longer asserted before requesting its transfer. The control signal is generated in slot one and is passed up the backplane. Lockout signal BPCDPN0 is generated in slot 1, which becomes BPCDPNA in slot 2, BPCDPNB in slot 3, through signal BPCDPNH in slot 9. Any controller in slots 2 through 9 that detects the signal, regenerates it through the next eight slots. If controllers are located seven or more slots away, the DMX priority network is broken. In this case, multiple controllers can request transfers at the same time.

Once the CPU has completed the tranfer, it clears the priority network by resetting the flip flop.

A priority network is also used to handle interrupts. Refer to Interrupt Priority Network for a more detailed explanation.

4.2.12 ADDITIONAL PROCESSOR FEATURES

All Prime processors, from the 2-board 150-II/250-II to the 11-board 850, share many of the same basic principles of operation. These include:

- Addressing modes
- Virtual memory
- STLB, cache
- Parity Generation
- DMX
- Interrupts

The following are the advanced features of the 3-board, 5-board and 11-board processors.

4.2.12.1 Extended Instruction Set (P500)

Decimal and Floating Point arithmetic operations are implemented in the microcode in 2-board processors. The 3-board processors implement these functions in the hardware, using the Extended Instruction Set (XIS) Board. The XIS Board, found on the P500 and up, has a 52-bit ALU for fast Floating Point calculations, plus another adder used during decimal and character string operations. A dual-port register file receives the data from the control unit and stores the results.

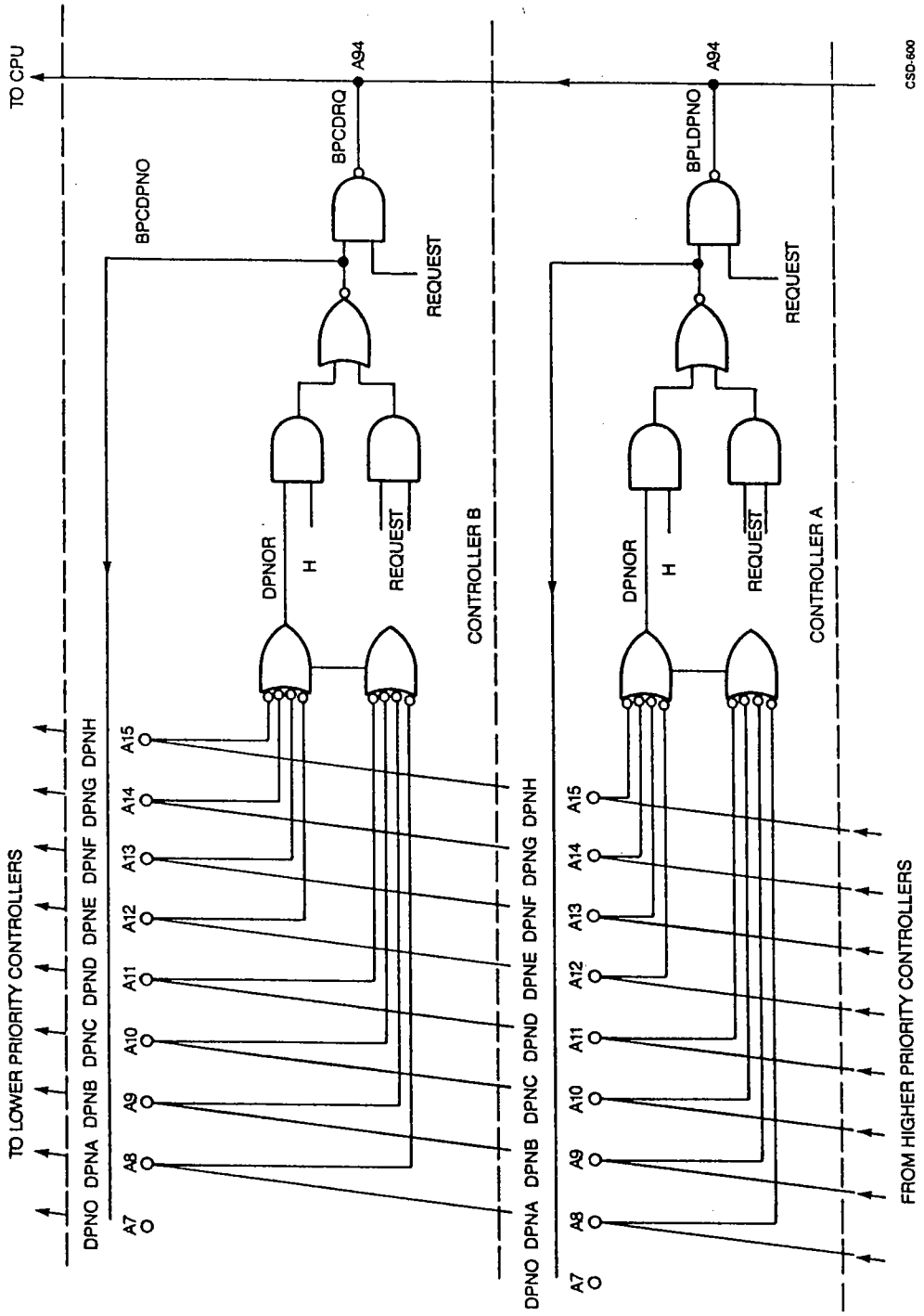


FIGURE 4-17: DMX PRIORITY NETWORK

4.2.12.2 Instruction Preprocessor Unit (P750)

The basic improvements in the Prime 750 over earlier models are: implementation of the diagnostic status word DSWPARITY, implementation of Burst mode DMA, and the Instruction Preprocessor Unit (IPU).

Burst mode I/O is implemented on the CS Board. Refer to the sections on burst mode DMA and wide-word memory for details.

The IPU, located on the J board, performs all the instruction fetch and decode functions of the 750/850 CPU. In addition, the IPU forms partial effective addresses of instructions to be executed by the CPU. The IPU's Instruction Phase (I phase) processing overlaps the A board's Execute Phase (E phase) processing. While the A board (or E unit) is executing one instruction, the IPU may be decoding, forming the effective address of the next instruction and fetching more instructions.

As stated previously, cache stores a program's series of instructions and most commonly referenced memory locations. During normal execution of a program, the CPU fetches a single instruction from cache, decodes the real address using the STLB, and executes the instruction. Then the process is repeated. The IPU speeds up processing time, since it fetches instructions from cache, then partially decodes them, before the CPU is ready to execute them.

The IPU takes up about half of the J board and can directly read 32 bits of data from the cache on the C board. In many cases, the cache performs a second read cycle on behalf of the IPU, during the execution of the last half of an E unit microinstruction.

The IPU can prefetch four instruction words ahead of the currently executing instruction. The IPU fetches 32 bits at a time from cache, then stores the bits in the Instruction Preprocessor Buffer (IPB). Each fetch from cache is normally overlapped with the last half of the current E unit microinstruction. Once the instructions are stored in the IPB, the IPU decodes and forms the partial effective address of the next instruction to be executed by the E unit.

The IPU continues to prefetch instructions from cache, until it encounters an obstacle that prevents fetching the next instruction word (e.g. IPU causes a STLB miss). A separate IPU register, RPI, contains the address of the next cache location to be fetched.

The IPU maintains copies of the base registers, but not of index registers. Therefore, the IPU can form the complete effective address of some instructions, but only the partial effective address if the instruction specifies indexing. In this case, the IPU gives the partial effective address to the E unit. The E unit must complete the effective address formation, using the appropriate index register.

The IPU is capable of resolving one level of indirectness as part of the effective address formation. Instead of fetching instructions from cache, the IPU can use one cycle to fetch an indirect word, which is needed for effective address formation. If the next instruction includes both an indirect word and indexing, the IPU cannot handle it. Both of these tasks must be done by the E unit. If post indexing is specified, then the IPU does the indirect fetch and gives the index

register addition to the E unit. If the IPU encounters an error (cache miss, pointer fault, etc.) during an indirect fetch, the E unit must fetch the indirect word and form the effective address.

In summary, the IPU does as much effective address formation as it can and gives the rest to the E unit. The IPU then begins working on the next instruction in the buffer.

4.2.12.3 Multi-Stream Processor (P850)

The 850 multi-stream processor is made up of two modified 750s (5-board processors), coordinated by the Stream Synchronization Unit (SSU Board). Multi-stream processing means that user requests are serviced by both CPUs simultaneously, instead of sequentially (see Figures 4-18 and 4-19).

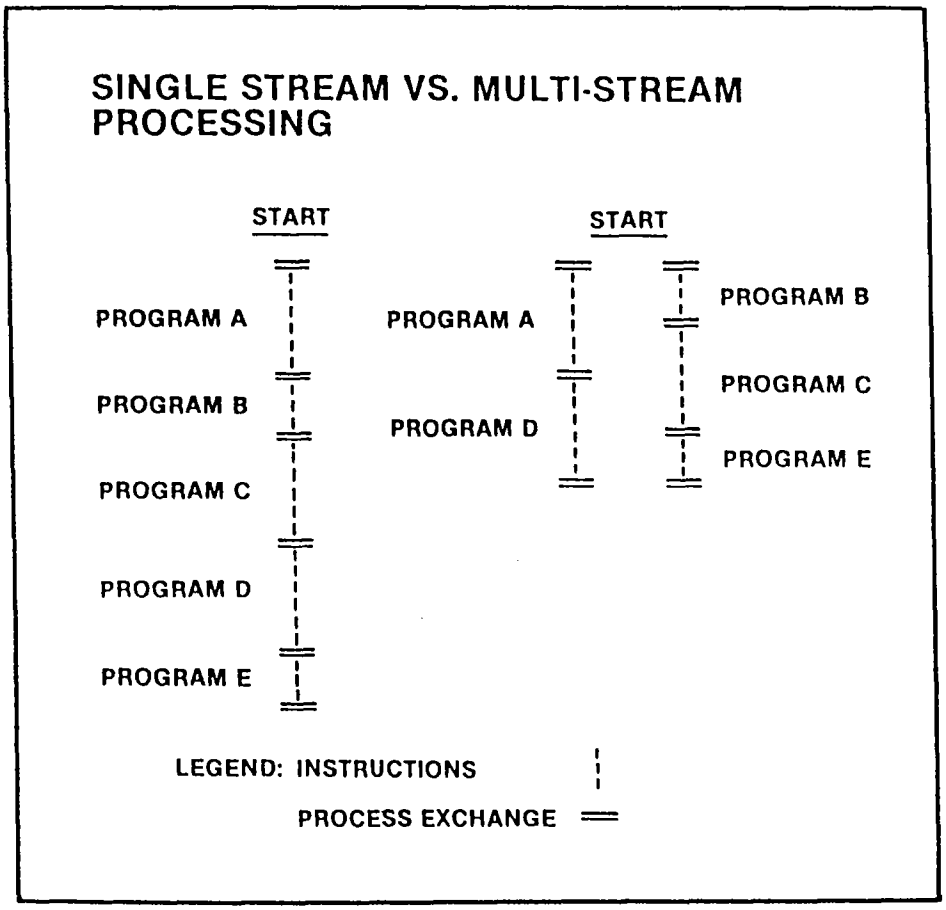


FIGURE 4-18: SINGLE STREAM VS. MULTI-STREAM PROCESSOR

The 850 uses standard power supplies, peripheral controllers and wide-word interleaved memory (E6, E7 E8 and E9 pairs); the E6 pairs are only used for test purposes. The 850 was the first processor to use 1Mb memory boards. These 1Mb boards allow maximum memory configuration to be housed in the main cabinet, thus obsoleting the memory extender. A new set of microcode, 96 pieces per CPU, and multilayer 16-slot and 19-slot backplanes are also used in the 850.

New artwork is incorporated in the C, J, and CS boards. The 850 CPU boards are not compatible with the 750 boards.

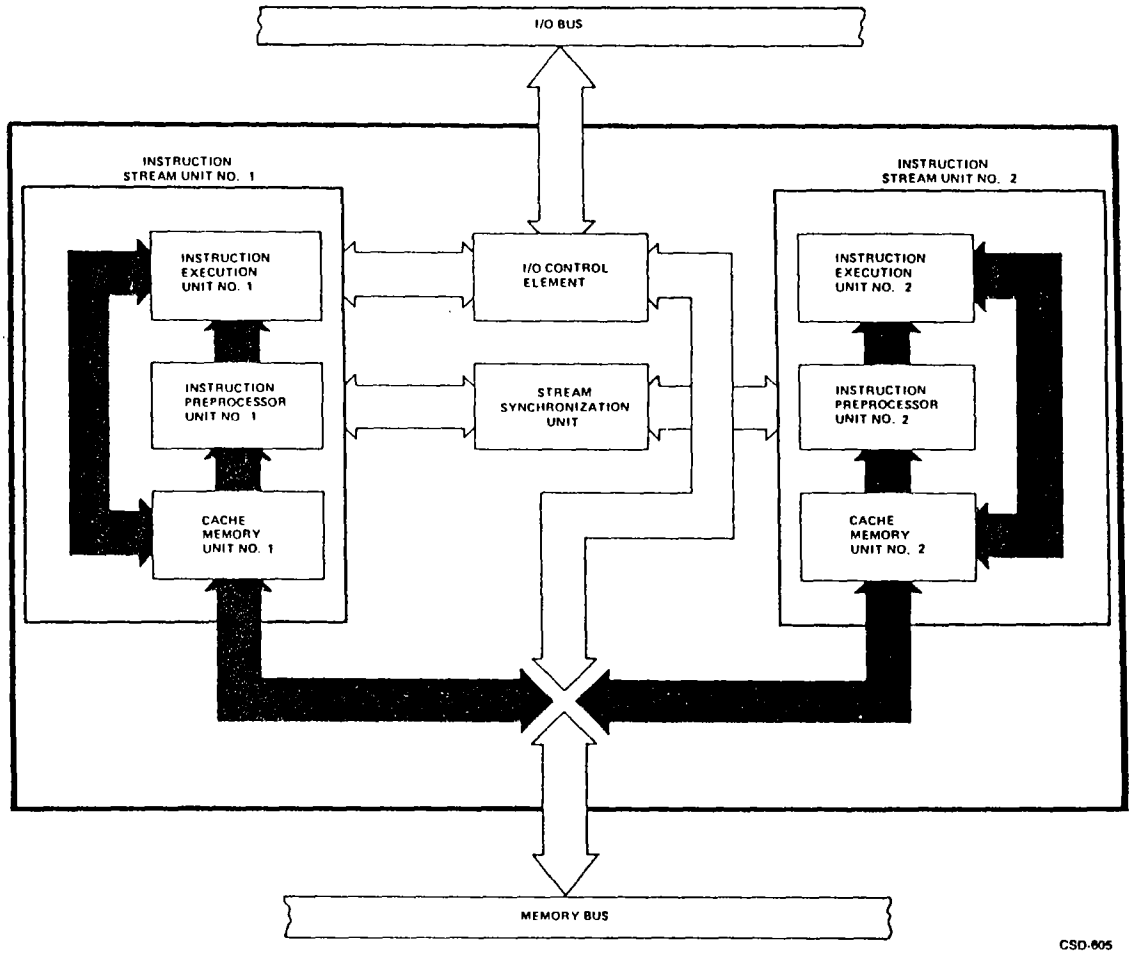


FIGURE 4-19: P850 FUNCTIONAL BLOCK DIAGRAM

To allow the processors to coordinate properly, process exchange (UPX), control panel (UCP), microcode traps (TRAPS), generics (GENA, GENB) and system clear (SYSCLR, APEIN) microcode have been modified. In addition, hardware and firmware for a microsecond process timer has been added.

4.2.12.4 Stream Synchronization Unit (SSU)

The SSU allows two processors to share memory and coordinate activities via the following mechanisms:

- Automatic Cache Invalidation
- Processor-to-Processor Communications
- Diagnostic Modes
- Switching of the I/O Bus

Each of these is discussed in the following paragraphs.

One problem with two processors sharing memory is to keep the cache current in both processors. This is solved by the SSU (Stream

Synchronization Unit), which plugs into the memory chassis and monitors all memory traffic. By keeping a copy of both cache indices, the SSU can detect a write by one processor into a memory location contained in the other processor's cache. microcode in the other processor, (notified via a FETCH CYCLE TRAP), can then perform the cache invalidation. The SSU provides a communications area for coordination between the two CPUs. (The SSU monitors all accesses to memory, and responds directly to addresses within the last page of segment 4.)

4.2.12.4.1 Automatic Cache Invalidation

There are two phases to a memory cycle. The first is an address. Address bits are sent on the BMA lines and latched on the memory boards and SSU. During the address phase, a line on the backplane is activated indicating which CPU is using the bus (BCPUNUM-). CPUNUM is used in addressing the cache indices, LIFOs, communication RAM and certain hardware registers. During the second phase of the memory cycle, data is transferred between the CPU and the SSU or memory boards. The SSU uses BMCINLV- to determine if one or two index cycles are required.

The SSU has a 4K cache index and a 4K LIFO buffer for each processor. A control latch written by BMCWDLL+ (Data Latch), holds data sent by the CPU C board on BMA.[95-00], during the data phase of the memory cycle. The information includes: 3 Virtual Address bits (VA.[04-06] to select the correct leaf in the cache), 1 bit to tell if this memory cycle is due to a cache miss, and 1 bit to indicate if this reference is to a shared page. In addition, a line on the backplane is sampled which indicates if the current memory cycle is a ring 0 access (BRING0+). An extra driver would have been needed on the C board to include BRING0+ with the virtual address, cache miss and shared page bits.

MEMORY WRITE OPERATION

During a write cycle that is not addressing the SSU:

1. Address bits BMA.[07-15] and the CPU number are combined with the VA.[04-06] bits to form an address to access the cache index of the other CPU.

2. BMA.[94-06] bits are compared with the data coming out of the addressed index cell.

NOTE

BMA.[94] has been defined but not implemented on the P850 to allow expansion of physical memory to 16Mb.

3. The counter which addresses the LIFO is incremented. The cache address bits (VA.[04-06] BMA.[07-15]) are written into the LIFO, if a hit is detected. (The LIFO count is initially set by microcode to zero.)

4. A nonmaskable interrupt is generated to the CPU whose index is being addressed. microcode in that machine will read the LIFO DATA register, load it into RMA and invalidate the cache cell. (Reading the LIFO DATA register also decrements the counter.)

5. The microcode continues reading the LIFO data until the LIFO is empty.

MEMORY READ OPERATION

During a read cycle, the cache index of the CPU doing the memory cycle is addressed similarily.

1. BMA.[94-06] is written into the index of the appropriate CPU, if the cycle is due to a cache miss. Also, the INDEX location is marked valid if the shared page bit is not set.

2. Master clear, via APEIN microcode, initializes all locations of both indices on the SSU to be invalid.

3. The SSU maintains a copy of the CPU's index, as the processor fills its cache.

For both reads and writes, interleaving turned on causes two index access cycles to be performed.

The SSU is implemented in such a way that the P850 may only be used with wide-word memories E8 and E9). The P850 microcode also makes this assumption. Because of burst mode, the memories must also be interleaved.

4.2.12.4.2 Processor-to-Processor Communications

Three hardware mechanisms are provided by the SSU to facilitate processor-to-processor communications:

1. The following function registers allow software and microcode to send messages between two processors:

   - HIGHPRI
   - SCAN
   - LOWPRI

   The registers are like two control buses between the processors. Each CPU has its own set of registers. By setting bits in its registers, one CPU sends instructions to the other CPU. The Most Significant Bit (MSB) is set by microcode or software to indicate that a function is pending in the Least Significant Bits (LSB). Just as the LIFO counter causes an interrupt when it isn't zero, the FUNCTION REGISTERS cause an interrupt to the other CPU when BIT.[01]=1. If, for example, one CPU loads a value of '100001 in the HIGHPRI register, the other CPU will be interrupted and will decode the least significant bit as a command to halt.

   To acknowlege a message, the receiving CPU clears the register. Since each CPU has its own registers, communication is

bidirectional at the same time. Each CPU can set the bits in its registers to cause an action by the other CPU.

The HIGHPRI register generates a nonmaskable interrupt, while the SCAN and LOWPRI registers create a maskable interrupt. The functions of the three registers are:

- HIGHPRI allows one processor to start or stop the other
- LOWPRI passes PTLB, ITLB and LIOT messages to keep both STLBs consistent and also holds a Process Exchange message, so one processor can request a register set held by the other processor
- SCAN is used by the Process Exchange microcode on one CPU to notify the other CPU of a change in the Ready List, which requires attention

2. A mapped (by CPU number) area of communication RAM acts as a data bus, so the CPUs can transfer data back and forth. This area is used in conjunction with the function registers. The unique feature of this area and the function registers is that address bit 11 holds the CPU number. This allows microcode in each CPU to use the same addresses to access physically different register and RAM locations.

3. The COMMON RAM area is shared memory. This RAM is addressed normally and contains the PX lock (SSU Address: 4/176101), the INH B lock (address 4/176102), the slave run cell (address 4/176100) slave state cell (address 4/176104) and other information common to both CPUs.

In summary, the CPUs communicate through two sets of SSU registers; exchange data through SSU communication RAM; and refer to common RAM for shared routines.

Each CPU can access these SSU registers and RAM locations because the SSU responds as an extended wide-word-type memory. The wide-word select codes (BMCSELB, BMCSELD) are the same as those used by the old 32K word modules (1232-D85). The old memories cannot be run on the P750/P850 because the CPU hardware interprets BMCSELB as wide-word capability. The old memories have been replaced by wide-word memories, which can be used for future types of wide word memories.

The CPU expects the SSU, as a wide word memory, to return 32 bits of data at a time, even though the SSU internal data paths are only 16 bits wide. To overcome this, the SSU drives two identical copies of the data back to the CPU (on BMD and BMA). For this reason, software and microcode must never attempt to perform long loads/stores from the SSU.

The SSU responds as page '477 in memory. So that the microcode can access it without concern for whether segmentation is enabled or not, the last page in Segment 4 (the 477th virtual page) must be mapped to the 477th physical page.

SSU MEMORY PROTOCOL

The SSU is addressed as the last page in segment 4 ('176000 - '177777). Address space definitions are listed in Table 4-2. All addresses are located in segment 4.

TABLE 4-2: SSU ADDRESS SPACE DEFINITION

ADDRESS SPACE	DEFINITION
'176000--'176007	Registers (this CPU)
'176010--'176037	Commun. RAM (this CPU)
'176040--'176047	Registers (other CPU)
'176050--'176077	Commun. RAM (other CPU)
'176100--'176177	Common RAM
'176400--'176417	Diagnostic

When the SSU detects that it is being addressed, it activates BMCDINH- (Data INHibit), to prevent a normal memory module at that address from responding. The SSU responds as an extended E6, but the memory timer PROM on the C board has been reprogramed to provide a short SSU memory cycle.

Then, the SSU latches the address from the BMA using BMCADL+. The CPU also uses the BMA during the data phase to transmit additional information to the SSU control latch (on BMA.[95-00]). The CPU sends the following information to the SSU control latch:

- VA.[04-06] - These are copies of RMA/RIA .[04-06], the cache leaf select bits are used to address the SSU's cache indices.
- Cache Miss - This bit is asserted by the CPU when the memory read in progress will update cache.
- Shared bit - This is asserted if the current cache miss cycle is to a shared page whose data can only be used once.

Two dedicated lines transfer the following information:

- BCPUNUM - CPUs are numbered 0 & 1. The CPU using the current memory cycle puts its number on this line. (SSU Address: 4/176106)
- BRING0+ - Ring 0 access asserts this bit.

Each CPU uses the same addresses to access the first 64 locations of the SSU page. The CPUNUM is used as an additional address bit, so the same address refers to two different register or RAM locations. The rest of the SSU page is addressed normally.

PARITY OPERATIONS

Seven bits of information are latched on the SSU whenever a parity error is detected. Six of these are parity error bits; the seventh indicates which processor was using the memory bus at the time of the error. These bits are located in the DIAGNOSTIC STATUS register at location '176401.

A parity error on the SSU will occur if:

1. A CPU reads a location on the SSU which has bad parity. In this case, the read data is returned to the CPU with bad parity.

2. An address on the memory bus has bad parity. In this case, the BMA parity error lines are asserted back to the CPU.

3. A parity error is detected during a write to a non-SSU location (which causes an index read on the SSU). In this case, the BMD parity error lines are asserted back to the CPU, immediately reporting an error.

4. A parity error is detected when closing the CONTROL latch, followed by bad parity returned on data read from the SSU. Again, the BMD parity error lines are continuously (until the error is cleared) driven back to the CPU, to immediately report the failure.

Anytime a parity error occurs while in Machine Check mode, the microcode will be trapped, the Check Lock will be obtained (to prevent the other CPU from interfering), the Diagnostic Status Register will be read and the parity bits checked for an SSU error. If an SSU error has occurred, DSWPARITYH.[16] will be set.

The Machine Check software then moves the parity information from the Diagnostic Status Register on the SSU to the logging area in PRIMOS.

The parity latch (the bits in the Diagnostic Status Register) may be cleared by writing to location '176406 on the SSU.

In Diagnostic Mode 00 or Mode 01, bad parity can be generated by setting the desired forced bad parity bit in the Control Register at location '176400. These three bits [10-12] can only be loaded by using the Memory Diagnostic instruction (MDWC op=1307).

SYSTEM CLOCK

The processors must use the same System Clock (TOSC+) to arbitrate the memory cycles quickly. To help synchronize the processors, the 25 MHz clock is located on the SSU. The clock skew between any two boards on different processors will have no more than double the maximum skew between boards within the processor. This results in a maximum skew of about 10 nanoseconds between processors.

4.2.12.4.3 Diagnostic Modes

Two SSU diagnostic modes allow all data paths, RAMs, registers and control paths to be tested. This means that except for the drivers for the special signals, the SSU may be tested on any CPU which supports E6 memory.

NOTE

The SSU uses two PRINET lines to drive signals to the CPU. When I/O controllers and the SSU reside in the same backplane

(P750 testbed), the nearest I/O controller must be at least 4 slots away.

Two bits control the diagnostic modes. When DIAG1-(See the Control register description in 850 NPB) is low, all diagnostic multiplexers are in the diagnostic state, except the Control Latch MUX. When DIAG2- is low, the Control Latch MUX is in the diagnostic state. These bits are defined in Table 4-3.

TABLE 4-3: 850 DIAGNOSTIC STATUS MODES

DIAG2-	DIAG1-	MODE
0	0	Diagnostic MODE 00
0	1	Diagnostic MODE 01
1	0	Not used
1	1	Normal mode

On power-up, both DIAG1- and DIAG2- are low. This is called Diagnostic Mode 00. In Mode 00, all the RAM and registers on the board may be written and read. Bad parity can be forced and a check made that the correct parity error bits are set. See the subsection on parity in this chapter.

The second mode (Mode 01) allows a simulated SSU cycle to determine if the cache invalidation detection and notification hardware is working properly. In Mode 01, DIAG1- is high and DIAG2- is low. In Mode 00 the indices are loaded with known data. Then in Mode 01, memory accesses are made and the LIFO data is checked, to see that the correct address is queued up and that a hit has occurred.

4.2.12.4.4 I/O and Refresh Master/Slave Logic

One CPU is the Refresh Master (BMSTCPU+=1) and provides refresh, fast and slow I/O Bus clocks.

The I/O Master is the CPU which is enabled to do I/O (DMX, Interrupts, PIO). The CPU number is also derived from I/O Master. The SWITIO+ bit in the Control Register changes I/O bus mastership and allows the VCP to talk with either CPU.

SSU switches, also duplicated on the status panel bezel, control the system configuration. In Multi mode, the top processor is both the Refresh and I/O Master; the bottom one does neither. In Uni mode, one or the other of the processors is enabled to operate; it is both Refresh and I/O Master.

NOTE

Switching between top processor Uni and bottom processor Uni modes while power is on, may cause a refresh cycle to be missed. The contents of main memory would then be invalid.

4.3 MAIN MEMORY

The E6, E7, E8 and E9 wide-word memory boards (2 x 16 bit words) are the standard memory boards for the 50 Series systems. The CPU generates all memory cycles, using its memory sequencer logic located on the B board (C on 750/850), to provide the proper timing for the type of memory selected by the address.

Discussed in the following subsections are:

- Noninterleaved Memory
- Interleaved Memory
- Noninterleaved Write Cycles on Interleaved Boards
- Wide-Word Memory
- Memory Error Checking and Correcting
- Memory Type Selection
- Memory Slot Selection

4.3.1 NONINTERLEAVED MEMORY CYCLE

A noninterleaved memory cycle is described as follows:

1. The CPU puts a memory address on the memory address bus (BMA).
2. The address is latched onto all memory boards using control signal BMCADL (address latch).
3. Each board compares the address with its slot address.
4. The slot address is determined by the slot selection lines (BMCEXS2, BMCEXS3, BMCSS01, BMCSS02, BMCSS03) configured on the board's slot in the backplane.
5. The board with the correct slot address sends a select valid signal (BMCSELV) to the CPU.

NOTE

If no memory board responds with select valid, the CPU causes a missing memory module check.

6. The CPU then triggers the selected memory using the precharge signal (BMCPRCH), followed by a write signal (BMCWRB). The absence of a write signal indicates a read memory cycle.
7. Next, the CPU transmits data to the memory on the memory data bus (BMD) and latches it onto the selected memory board using control signal BMCWDLL (write data latch). The memory then stores the latched data completing the write cycle.
8. On read cycles, the memory fetches the data from the addressed location and presents it to the memory data bus (BMD). The CPU,

at the proper time, receives the data, checks its parity, and ends the cycle.

Memory addressing is illustrated in Figures 4-20 and 4-21. For use in this illustration, memory boards containing only eight locations are shown. Therefore, only five address lines (BMA12-16) are required to access four boards. The first two boards (first pair) are shown in the illustration.

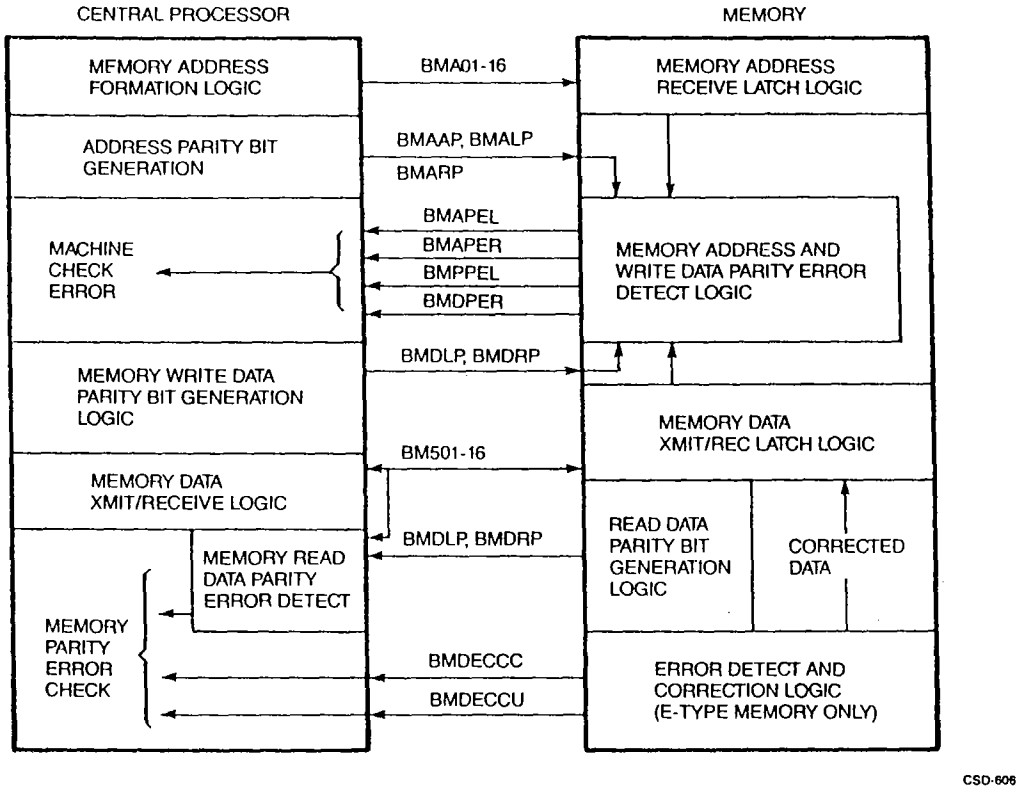


FIGURE 4-20: MEMORY INTERFACE ADDRESS AND DATA PATHS

4.3.2 INTERLEAVED MEMORY CYCLE

Interleaved main memory means that consecutive memory locations reside on separate memory boards. Interleaving speeds sequential memory accesses and maximizes the cache hit rate, since the CPU can read or write to two sequential locations during one memory cycle. The CPU accesses both boards of an interleaved pair during one cycle (see Figure 4-21).

All even memory addresses are located on the first board of an interleaved pair. All odd memory addresses for the pair are on the second memory board. The first board of the interleaved pair must be physically located in the slot directly above the second board in the pair. If the CPU accesses address 6, address 6 is selected from the first board, and address 5 is selected from the second board. If the CPU accesses address 5, address 5 is selected from the second board, and address 6 is selected from the first board.

The least significant address bit defines the first or second board of an interleaved pair. The most significant address bit selects the even or odd location on the memory boards. For example, if the

address requests location 5 on the first board, memory address 14 is accessed. If the address requests location 5 on the second board, memory address 15 is accessed.

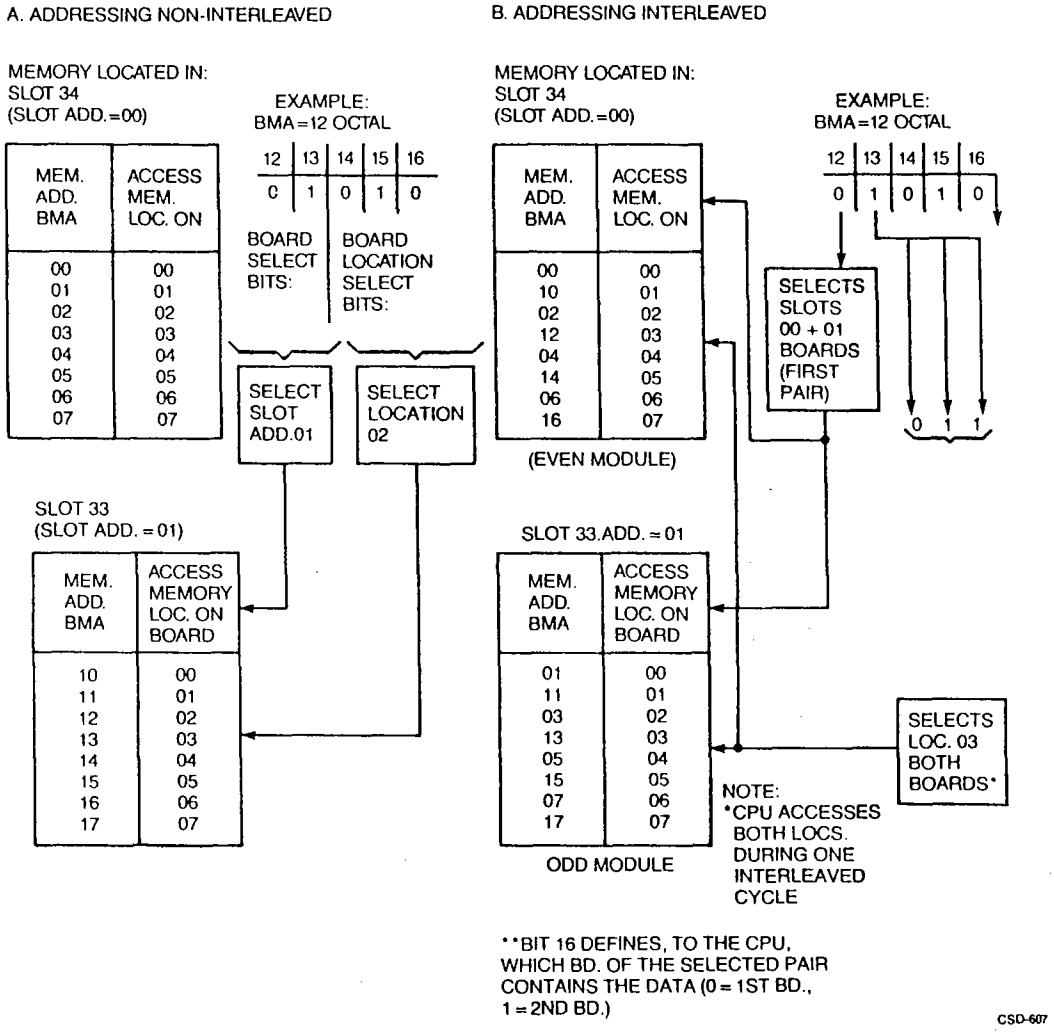


FIGURE 4-21: MEMORY ADDRESSING CONCEPTUAL ILLUSTRATIONS

NOTE

The CPU uses bit 16 to determine which board will send or receive data.

Interleaving memory cycles require two signals. Memory board control line BMCINLV indicates interleaving turned on for the memory boards. CPU control line BMCI orders an interleaving cycle to occur in the CPU and memory. BMCI cannot occur if BMCINLV is not sent from the memory.

Interleaved read cycles occur as follows:

1. The CPU sets up BMA with the desired address and latches it onto all memory boards. Two boards select returning BMCSELV and BMCINLV. The selected boards are considered an interleaved pair and always select together.

2. The CPU sends BMCI, which allows cycles to occur on both boards, and then sends BMPRCH, triggering the read cycles. The two boards are allowed time to complete their read cycles, at which time data is available from each board to the BMD. However, data from both addresses cannot be put onto the bus at the same time.

3. The low order slot select line (BMCSS03), which determines which board is even and which is odd, along with the absence of control signal BMCEBL (enable B latch), causes the even board (module 0) to enable its data to the data bus (BMD). The CPU takes the data word.

4. The CPU then enables signal BMCEBL, and along with BMCSS03 to point out the board, shuts off data from the even board and causes the odd board (module 1) to enable its data to BMD. The CPU takes this data word; two words have been transferred during the read cycle.

Interleaved write cycles occur as follows:

1. The CPU sends the address on BMA with BMCADL to latch it on to all boards. The selected pair of memories select and return BMCSELV and BMCINLV.

2. The CPU sends BMCI and write control signal BMCWRB. The write cycle is triggered on both boards when the CPU sends BMCPRCH.

3. The CPU sends the first data word on the BMD and write data latch control signal (BMCWDLL). Module 0 (even board) will receive this data, since BMCEBL is absent.

4. The CPU then enables BMCEBL and places the second data word on BMD. BMCWDLL then allows the odd board (Module 1) to latch the data. Both modules then complete the write cycle, storing their respective data words.

4.3.3 NONINTERLEAVED WRITE CYCLES ON INTERLEAVED BOARDS

Though interleaving is enabled, in most cases writes are noninterleaved (single-word). The CPU usually only knows the data to be stored in one location of the interleaved pair. Noninterleaved write cycles proceed as follows:

1. The CPU sends BMA and BMCADL. Both boards of the pair select returning BMCSELV and BMCINLV. Because the CPU does not desire an interleaved cycle, it does not send BMCI. The absence of BMCI forces the memory boards to look at BMCEBL to see which board will write and receive data.

2. The CPU sends control signal BMCEBL, setting the low order address bit (bit 16) for the correct board. If BMCEBL is not true (0), the first board receives the data and starts a write cycle when BMCPRCH is sent from the CPU. If BMCEBL is true (bit 16=1), then the odd board (module 1) is enabled to receive data and write.

3. The enabled module only stores the data word.

4.3.4 WIDE-WORD MEMORY

Wide-word memory is the standard for 50 Series processors. It operates the same as nonwide-word memory, when set to E4 mode and used with processors other than the 750/850. When the memory is set to E6 mode, it can be used in the 750/850 for wide-word transfers. During a wide-word transfer, data is sent on both the BMD and the BMA.

During normal cycles, 16 data bits are transferred from memory to the CPU. During interleaved cycles, 32 bits are transferred. If wide-word interleaved memory is used (750/850 only), 64 bits (four 16 bit wide words) are transferred in one cycle.

Interleaved memories operate on a 16-bit bus and transfer 16 bits at a time, first from one board and then from the other. Wide-word memory transfers 16 bits from one board on the BMD and an additional 16 bits on the BMA.

The wide-word memory can operate in either E4 or E6 mode, depending on the dip switch settings. In E4 mode, the board operates as a single nonwide-word memory, and is used in P400 based processors. Data is stored in contiguous locations, transfers are done via the BMD, and single access cycles are executed. In E4 interleaved mode, a single memory can be used to test interleaving capabilities. Again, data is stored in contiguous locations and transferred via the BMD. Interleaved read operation reads data to see if a normal interleaving cycle can be executed. Interleaved write operation is not allowed. A pair of wide-word boards configured for E4 interleaved mode, operate the same as a pair of interleaved nonwide-word boards.

In E6 (wide-word) mode, the memory must be used in pairs. The key to wide-word operation is the use of the BMA to transfer data, in addition to address information. Normally, address bits are sent on the BMA as negative true (1=0V). Data bits are sent on the BMD as positive true (1=+5V). A new signal, BMCDONA, disables the address drivers on the memory and enables data drivers, so data is sent as positive true over the BMA. Wide-word operation is not dependent on signal BMCEBL, the way the interleaved cycle is.

During wide-word interleaved accesses, 64 bits are transferred. An extra signal allows two accesses in one cycle. Wide-word interleaved writes are performed during burst mode DMX input. To operate in the 750/850, the-wide word boards must be configured in pairs, with interleaving turned on.

4.3.4.1 Wide-Word Interleaved Read

Wide-word interleaved read operation is described as follows:

1. The CPU sets up BMA with the desired address and latches it onto all memory boards (BMCADL). The address is sent negative true (1=0 Volt). Two boards select returning BMCSELV, BMCINLV and BMCSELB (wide-word). The selected boards are considered a pair and always select together.

2. The CPU requests a wide-word interleaved access by sending BMCWWM and BMCI. The CPU then sends BMPRCH, which triggers read cycles on both boards. The two boards are allowed time to complete their read cycles, at which time data is available from each board.

3. The low-order slot-select line (BMCSS03), which determines which board is even and which is odd, causes the even board (module 0) to enable its data onto the data bus (BMD). The CPU takes the data word.

4. The CPU sends signal BMCDONA which disables the address drivers on the odd memory board. The signal tells memory that the BMA will be used to transmit data (positive true, 1=+5V). The odd board puts its data on the address bus. The CPU takes the data word.

5. The CPU sends signal BMCEBL, which forces the latches open again. The boards then place the second data words on the BMD and the BMA.

4.3.4.2 Wide-Word Interleaved Write

Wide-word interleaved write operation is described as follows:

1. The CPU sets up BMA with the desired address and latches it onto all memory boards (BMCADL). Address is sent negative true (1=0 Volt). Two boards select returning BMCSELV, BMCINLV and BMCSELB (wide-word).

2. The CPU sends BMCWWM, BMCI and write control signal BMCWRB. This signal is high when the CPU sends BMCPRCH; it triggers write cycles on both boards.

3. The CPU sends BMCDONA to disable the address drivers on the odd memory board, so memory will recognize the bits as data (positive true).

4. The CPU sends the first data word on the data bus (BMD), plus the write data latch control signal (BMCWDLL). Module 0 (even board) receives this data. The CPU then puts the second word on the address bus. Both modules complete the first write cycle, storing their respective data words.

5. The memory timing then generates a signal which opens the latches again. The CPU sends the next set of data words on the BMD and the BMA. The boards write their respective words.

4.3.5 MEMORY ERROR CHECKING AND CORRECTING (ECCC)

All 50 Series systems have MOS error checking and correcting (ECCC) memory. MOS is a low power, high density chip. Ultra high density MOS chips store up to 64K bits per chip. The 256Kb memory uses 16Kb MOS chips. The 64Kb chips are used in 1/2 and 1Mb memory boards.

ECCC memory does not generate byte parity. Instead, it generates parity on the entire 16-bit data word. Parity is checked (and data is corrected if necessary) during memory reads. Byte parity errors on old style memories caused machine halts. ECCC memories correct one-bit errors, so the machine does not halt on that kind of error.

Wide-word ECCC memory boards are listed in Table 4-4.

TABLE 4-4: MEMORY BOARD CAPACITY

MEMORY BOARD	CAPACITY
12128-E6	.25 Mb
12256-E7	.50 Mb
12512-E8	1.00 Mb
7615-902 (E9)	1.00 Mb

Read and write operations are described in detail in the following subsections.

4.3.5.1 ECCC Memory Write Operation

Memory writes follow these steps:

1. The CPU sends 16 data bits and 2 parity bits to memory.
2. Memory generates 5 check bits and 1 overall parity bit from the data received.
3. Memory stores the 16 data bits and its 6 parity bits.

4.3.5.2 ECCC Memory Read Operation

Memory reads are performed as follows:

1. The CPU sends an address to memory.
2. Memory puts 16 data bits and 6 parity bits on the BMD.
3. Memory generates a syndrome pattern from the first 5 parity bits. Memory uses the syndrome pattern to detect one bit errors in the data.
4. Memory notifies the CPU on signal BMCECCC, if an error is detected.
5. Memory then sends the corrected data on the BMD.
6. Memory sends the syndrome pattern, plus a status bit for the overall parity bit, on BMD lines 01-06. The status bit is a check on the overall parity bit, whether it is good or bad. If the overall parity bit indicates an ECCC error, but the syndrome pattern does not, the overall parity bit may be bad. The status bit would indicate this.
7. The CPU stores the syndrome pattern and the overall parity bit in the Diagnostic Status Word Register File.

If memory detects multiple-bit errors:

1. It sends signal BMCECCU to the CPU.

2. The CPU's memory parity handling routine checks the Diagnostic Status Word Register File for the type of error (ECCU or ECCC).

   A) Determines what bit is in error, by checking the syndrome pattern.
   B) Prints an error at the system console.

The memory extender consists of several memory boards with a separate cabinet, chassis and power supply, cabled to a memory extender board in the mainframe cabinet. This product was necessary when a system needed more than eight memory boards. Since the 1Mb memories were developed, this product has become obsolete.

4.3.6 MEMORY TYPE SELECTION

The backplane can contain a mixture of wide-word or nonwide-word memories in different sizes, configured with interleaving on or off. Each time a memory board is selected on an access by the CPU, it identifies itself on control lines BMCSELB, BMCSELC, and BMCSELD. These control lines cause the CPU to initiate the proper memory timer sequence for that type of memory (see Table 4-5).

TABLE 4-5: MEMORY TYPE SELECTION TO CPU

SELECT LINE	E6,E7,E8,E9	MEMORY TYPE: E4	MEM. EXTENDER
BMCSELB	1	0	x
BMCSELC	x	x	1
BMCSELD	0	1	x

NOTE

The memory extender reports itself (BMCSELC) plus the memory type located in the extender chassis (BMCSELB or BMCSELD).

4.3.7 MEMORY SLOT SELECTION

Memory address is determined by slot location and slot selection signals. The memory address is not hardwire to the board.

The BMC slot selection signals on the backplane are actually a series of grounded and ungrounded pins in the backplane slots. Each slot has its own slot address (code) configured into these pins. During manufacture, these pins are either grounded or left ungrounded (open). Because a ground will override a high (+5VDC in Prime's case), the memory board attempts to pull up all slot selection lines to a +5V. Any of the pins left ungrounded in the backplane are pulled up. The top-most slot in a backplane has all slot-selection pins ungrounded, resulting in a code of 00 as a slot address. Any memory board plugged into this slot uses the slot address to identify itself. The memory board compares its slot address to the board select bits of the address on the address bus (BMA). If they match, it will return select valid (BMCSELV) to the CPU, thus allowing itself to be accessed

by the CPU. These slot-select signals are qualified true when detected at ground by the memory board logic (True=1).

NOTE

When interleaving is turned on, the compare of BMCSS03- and BMAXX (low order board select address bit) is disabled. Two boards of an even odd pair are selected.

4.4 CHASSIS AND BACKPLANE

Prime systems utilize a chassis and mother board backplane combination to hold the Prime printed circuit boards (PCB) and act as a source of dc power and common interface signals between the CPU, memories, and I/O controllers. A new backplane was introduced on the 850 system. The chassis and backplanes are discussed in detail in the following subsections.

4.4.1 CHASSIS

The chassis is mounted flush to the cabinet cooling plenum (see Figure 4-22). When plenum baffle plates are removed, cool air is forced into the chassis and across any installed boards.

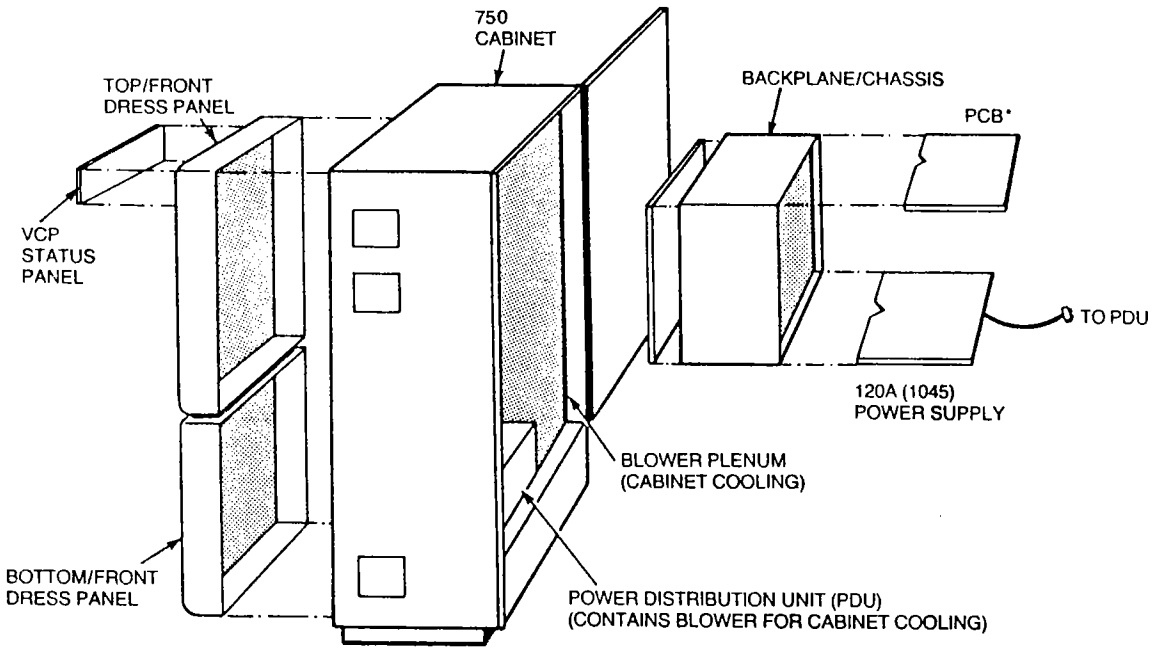


FIGURE 4-22: SYSTEM ILLUSTRATION (PART ONE)

There are two basic chassis configurations. The 37-slot chassis is designed for up to three power supplies. Older 750 systems use this type of chassis. The 38-slot chassis, designed for up to four power supplies, is used by newer 750s.

The 37-slot (26 board) chassis is made of two 10-slot chassis (top backplane) stacked on top of one 17-slot chassis (lower backplane). Because of power and bus loading specifications, a maximum of 26 boards can be housed in the 37-slot chassis. In single-cabinet systems, the CPU and memory are limited to the slots in the upper backplane. (Refer to Figure 4-23.)

The 38-slot chassis is also made up of two backplanes. One backplane is 19-slots, the other is 16-slots.

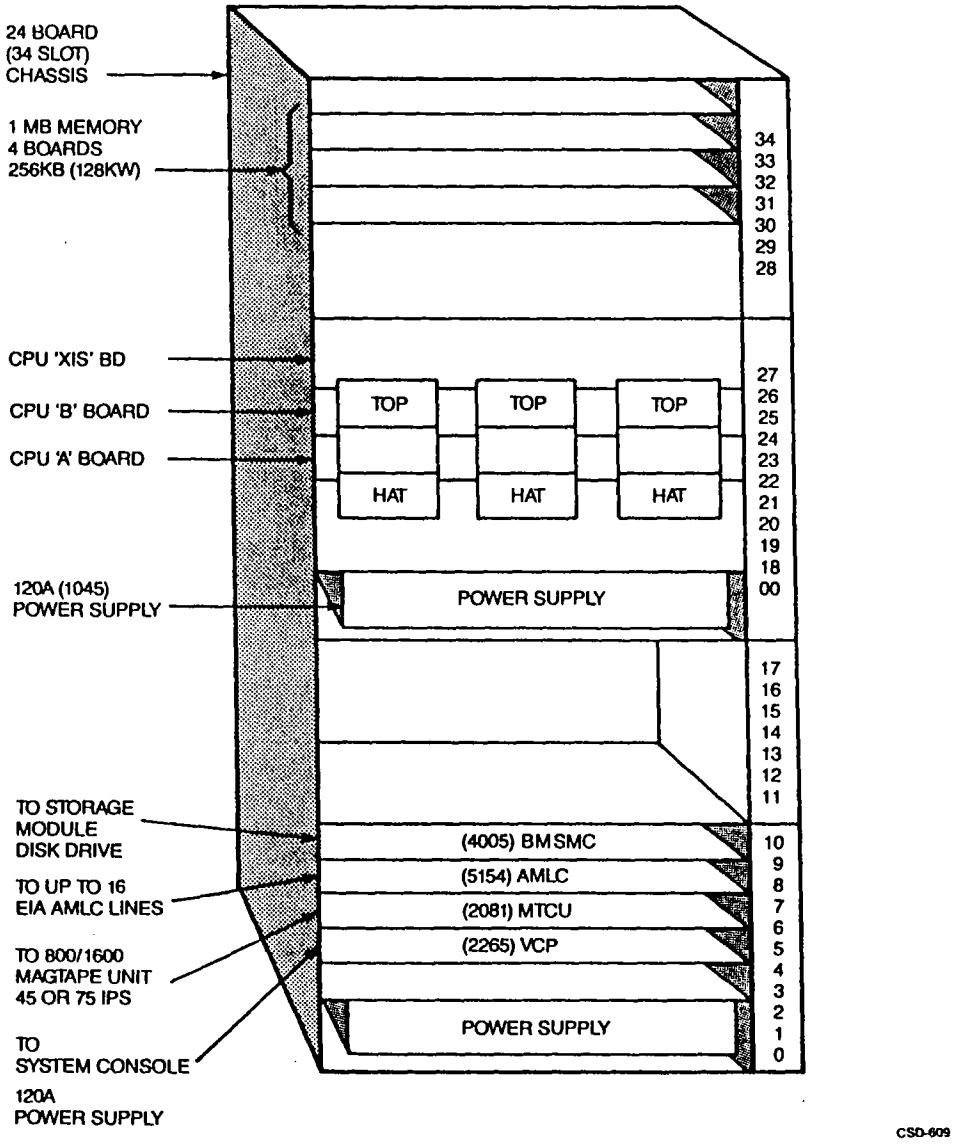


FIGURE 4-23: SYSTEM ILLUSTRATION (PART TWO, REAR VIEW)

The 150-II and 250-II are housed in the 17-slot chassis. The 450-II and 550-II are housed in 34-slot (24 board) chassis, made up of two 17-slot chassis stacked together. The 850 CPU is housed in a 35-slot chassis, made up of one 19-slot backplane and one 16-slot backplane, mounted on one 17-slot chassis and two ten-slot chassis. Table 4-6 lists the number of slots and the number of chassis for each system.

TABLE 4-6: SYSTEM SLOTS AND CHASSIS

SYSTEM	NO. SLOTS	NO. CHASSIS
150/250II	10	1
550-II	34	2 (17,17)
Old 750	37	3 (10,10,17)
New 750	38	4 (10,10,10,10)*
850 CPU	35	3 (10,10,17)*
850 I/O	19	2 (10,10)**

* Two slots not used
** One slot not used

The total number of boards plugged into each section of the backplane cannot exceed the power specifications for that section's power supply. The +5 Vdc and ±12 Vdc voltages must not be overloaded.

4.4.2 BACKPLANE

The backplane connects all the boards in the system (see Figures 4-24 and 4-25). Voltage from the power supplies, plus control and data signals from the various boards, pass along the backplane buses to other parts of the system. In dual-backplane systems, backplane I/O bus lines and memory slot select lines are wired from the top backplane to the lower one.

The 750 and 850 use a multilayered backplane, two outer layers contain buses and two inner layers supply voltages. In multilayered backplanes, four mass-terminated shielded cables carry I/O signals and two carry memory bus signals.

The backplane is an etched printed circuit board (PCB), containing two 100-pin connectors for each PCB and power supply slot. In the 850, the top slot is used for the mass-terminator pins, which are on a .100 center. This results in a 19-slot backplane across two 10-slot chassis; and a 16-slot backplane on a 17-slot chassis. The 19-slot backplane provides special stitch connections (jumper plug) between its upper and lower chassis. These stitches allow the I/O bus to be connected or not connected between the two chassis.

Logic signals are wired in parallel, except memory slot selection and DMX interrupt priority network lines. This means that PCBs are not restricted to specific slots in the backplane. The slot selection logic and DMX priority give PCBs in lower backplane slots higher priority in using system resources. In Figure 4-24 for example, the tape controller has higher priority than the disk controller, if both are trying to pass data to memory simultaneously.

4.4.2.1 Major Backplane Buses

The backplane has six major buses:

- Three are for communications between the CPU and the I/O controllers.
- Three are for communications between the CPU and memory.

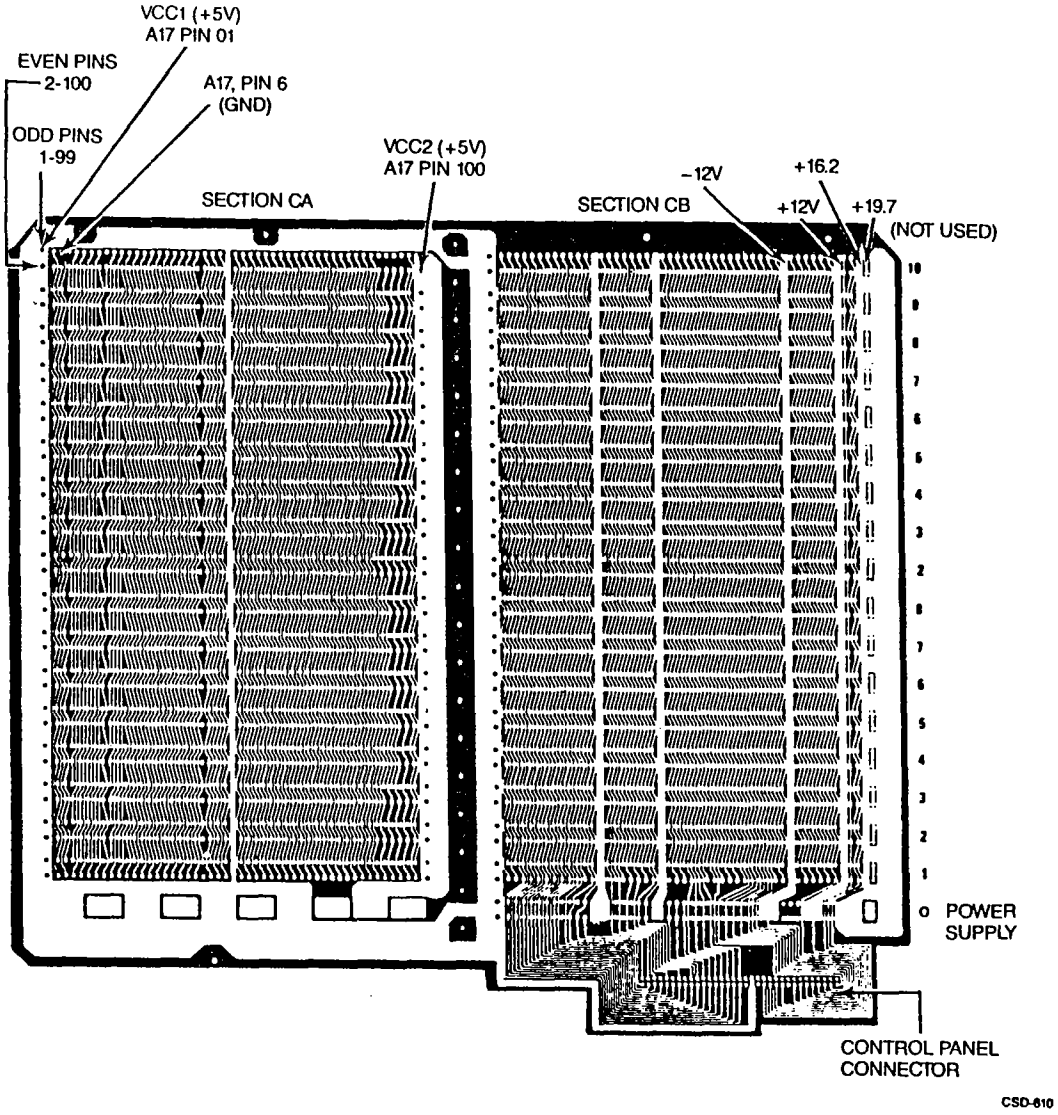


FIGURE 4-24: 17-SLOT BACKPLANE

These buses are illustrated in Figure 4-26.

Controllers cannot communicate directly with memory. To transfer data from a peripheral device to memory, the controller passes the data to the CPU on an I/O bus. The CPU in turn, passes the data to a specific storage location using a memory bus. The I/O buses, all bidirectional, are the:

- Data Bus (BPD) - which passes data bits between the CPU and I/O controllers. The BPD (Bus Peripheral Data) has 16 data bits, 2 parity bits, and 2 parity error signals (BPDPEL and BPDPER).

- Address Bus (BPA) - which passes address information between the CPU and I/O controllers. The BPA (Bus Peripheral Address) consists of 16 address bits, 2 parity bits, and 2 parity error signals (BPAPER, and BPAPEL). Address information is either:

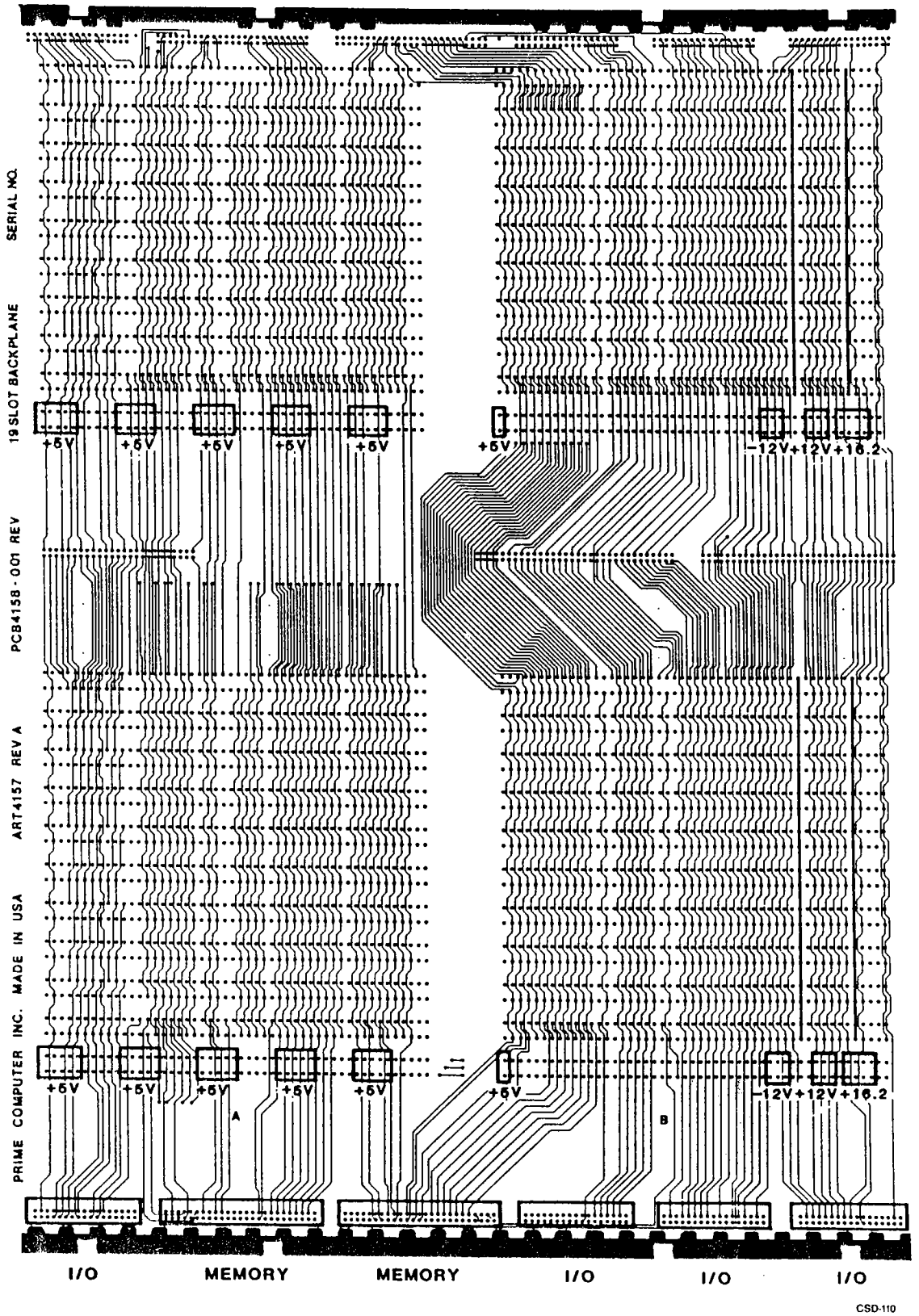


FIGURE 4-25: 19-SLOT BACKPLANE

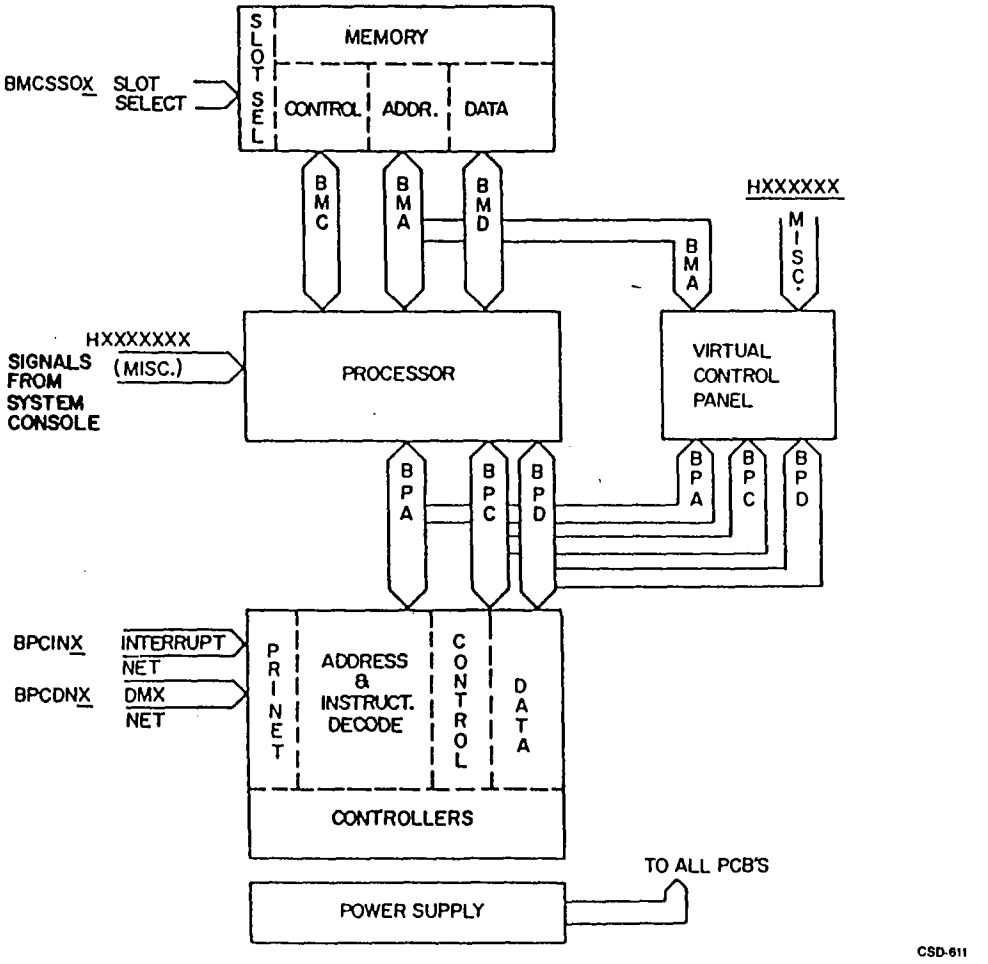


FIGURE 4-26: BASIC SYSTEM BLOCK

A) Programmed I/O (PIO) instructions from the CPU to the controller.
B) DMX and interrupt channel addresses from the controller to the CPU.

- Control Bus (BPC) - which passes control signals that determine how the BPD and BPA will be used. The BPC (Bus Peripheral Control) signals are used for timing and control, DMX and interrupt priority network commands, and operational mode lines from the controller to the CPU. Operational mode lines tell the CPU what kind of data transfer (DMA, DMQ, DMT, DMC, or BDMA) is needed; and whether the transfer will be to memory from the controller, or from memory to the controller.

The memory buses are:

- Data Bus (BMD) - which passes data bits between the CPU and memory. The bidirectional BMD (Bus Memory Data) has 16 data bits, 2 parity bits, and 4 error signals (BMDPER, BMDPEL BMDECCC and BMDECCU).

- Address Bus (BMA) - which passes memory addresses from the CPU to memory. The uni directional BMA (Bus Memory Address) has 22

address bits, 2 parity bits and 2 parity error signals (BMAPER, and BMAPEL).

NOTE

The BMA is bidirectional during wide-word memory transfers.

- Control Bus (BMC) - which passes control signals between the CPU and memory. The bidirectional BMC (Bus Memory Control) is used for memory timing and control and slot selection logic. Signals from the CPU indicate whether the transfer will be a memory read or write. Slot-selection signals from memory are used by the CPU to determine a controller's slot address and interrupt priority.

4.4.2.2 Backplane Bus Signals

Table 4-7 lists the backplane bus signals. Refer to Figure 4-27 for backplane pin number identification.

TABLE 4-7: BACKPLANE SIGNAL LIST

BACKPLANE PIN NO.	SIGNAL NAME	DESCRIPTION
A1,2,49 50, B1,2	VCC1	+5 VOLTS (not battery)
A99,100	VCC2	+5 VOLTS (battery)
B91,92	V12+	+12 VOLTS DC
B77,78	V12-	-12 VOLTS DC
B97,98	VSS	+16 VOLTS DC
B99,100	VBB	+19.2 VOLTS DC
A3,22, A26,48	SHIELD	CHASSIS GROUND
A6,24,42 A60,80,98 B3,26,30 B42,46,57 B80,96	GND	LOGIC GROUND
B59	BPCPIO+	PERIPHERAL CONTROL PROGRAMMED I/O - required by control unit to determine usage of (DMX, PIO or INTERRUPT) the address (BPA) lines
B62	BPCREDY+	PERIPHERAL CONTROL READY - notifies CPU of control unit's ability to accept or send data, or senses a condition is true in the control unit
B95	BPCSTRB+	PERIPHERAL CONTROL STROBE - signals the control unit data has been taken/sent to/from CPU

Left Right
A ⟷ B
From Front
ODD Pins on TOP.

TABLE 4-7: BACKPLANE SIGNAL LIST (Cont.)

BACKPLANE PIN NO.	SIGNAL NAME	DESCRIPTION
B61	BPC60CY+	PERIPHERAL CONTROL 60 CYCLE
A54	PS60CY+	POWER SUPPLY 60 CYCLE
A90	BPCFCLK+	SYSTEM FAST CLOCK- 5MHZ signal derived from the CPU Master Clock
B90	BPCSCLK+	SYSTEM SLOW CLOCK- Derived from CPU Master Clock
B41	HSYSCLR-	SYSTEM CLEAR- Developed from Power On or Master Clear
B27,28	HPFRLY+	POWER FAIL RELAY
B43,44	PSRLY+	POWER SUPPLY SYSTEM CLEAR RELAY
B25 (should be High at all times.)	HPWRFL-	SYSTEM POWER FAIL - developed on the control panel from the power supply (PFL)
B85	BPCMOD0+	MODE LINES- CPU determines, via code on lines MOD0-MOD3 what mode CPU is to work in (i.e. DMC,DMT,DMQ,DMA,PIO, OR INTERRUPT)
B86	BPCMOD1+	
B87	BPCMOD2+	
B88	BPCMOD3+	
B89	BPCINMD+	Determines input or output mode
A94	BPCDRQ-	DMX cycle request from control unit to CPU
A5	BPCDEN+	DMX cycle enabled from CPU
A4	BPCDCPN+	CLEAR DMX PRIORITY NET from CPU
A30	BPCEOR+	CPU DETECTED (DMX) END OF RANGE
A7	BPCDPNO-	DMX PRIORITY NET OUT
A8	BPCDPNA-	DMX PRIORITY NET IN A to H - Determines which controller of those requesting a DMX cycle has the highest priority, and holds off lower priority requests
A9	BPCDPNB-	
A10	BPCDPNC-	
A11	BPCDPND-	
A12	BPCDPNE-	
A13	BPCDPNF-	
A14	BPCDPNG-	
A15	BPCDPNH-	
A92	BPCIRQ-	PERIPHERAL INTERRUPT CYCLE REQUEST
A16	BPCIEN+	INTERRUPT CYCLE ENABLED FROM CPU
A23	BPCICPN+	CLEAR INTERRUPT PRIORITY NETWORK
A25	BPCCHI+	CLEAR HIGHEST ACTIVE INTERRUPT
A38	BPCIOVI+	INTERRUPT OVERRIDE INHIBIT

TABLE 4-7: BACKPLANE SIGNAL LIST (Cont.)

BACKPLANE PIN NO.	SIGNAL NAME	DESCRIPTION
A17 A18 A19 A20 A21	BPCIPNO- BPCIPNA- BPCIPNB- BPCIPNC- BPCIPND-	INTERRUPT PRIORITY NET OUT INTERRUPT PRIORITY NET IN A thru D - Determines which control unit has highest interrupt priority of those requesting an interrupt cycle and holds off lower priority requests
A32	BMCSELD-	MEMORY SELECT D - Selects timing for E type memory boards
A79	BMCSELC-	MEMORY SELECT C - Selects timing for memory extender operation
A81	BMCSELB-	MEMORY SELECT B - Selects timing for D85 type memory boards
A82	BMCSELV-	MEMORY SELECT VALID - causes Missing Module Trap if not present
A87	BMCEXS1-	MEMORY SLOT SELECT EXTENSION 1 - slot select signals are used to indicate the slot address of the backplane slot
A89	BMCEXS2-	MEMORY SLOT SELECT EXTENSION 2
A91	BMCSSO1-	MEMORY SLOT SELECT 1
A93	BMCSS02-	MEMORY SLOT SELECT 2
A95	BMCSS03-	MEMORY SLOT SELECT 3
A33	BMCINLV-	MEMORY INTERLEAVED FROM SELECTED MEMORY
A51	BMCADL+	MEMORY ADDRESS DATA LATCH
A34	BMCEBL-	MEMORY ENABLE INTERLEAVE (from CPU)
A35	BMCI+	MEMORY INTERLEAVE (to memory)
A86	BMCRFSH-	ENABLE MEMORY CONTROL REFRESH CYCLE
A96	BMCPRCH-	MEMORY PRECHARGE - Initiate memory cycle on memory board.
A97	BMCMML-	MEMORY MODE LINE for E-type memory use only (to memory)
A83	BMCDINH-	MEMORY DATA INHIBIT
A88	BMCWSTRB-	MEMORY WRITE STROBE
A84	BMCWRB-	MEMORY WRITE, RIGHT BYTE
A85	BMCWLB-	MEMORY WRITE, LEFT BYTE
A43	BMCWDLR+	MEMORY WRITE DATA LATCH, RIGHT BYTE
A47	BMCWDLL+	MEMORY WRITE DATA LATCH, LEFT BYTE

TABLE 4-7: BACKPLANE SIGNAL LIST (Cont.)

BACKPLANE PIN NO.	SIGNAL NAME	DESCRIPTION
A61	BMD01+	MEMORY DATA BUS: (BMD01 THRU BMD16)
A62	BMD02+	
A63	BMD03+	MEMORY DATA BIT PATTERN:
A64	BMD04+	
A65	BMD05+	MSB LSB
A66	BMD06+	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
A67	BMD07+	LEFT BYTE RIGHT BYTE
A68	BMD08+	
A69	BMD09+	
A70	BMD10+	
A71	BMD11+	
A72	BMD12+	
A73	BMD13+	
A74	BMD14+	
A75	BMD15+	
A76	BMD16+	
A77	BMDLP+	MEMORY DATA, LEFT BYTE PARITY BIT
A78	BMDRP+	MEMORY DATA, RIGHT BYTE PARITY BIT
A44	BMDECCC-	MEMORY DATA ERROR-CORRECTION-CODE- -CORRECTABLE: (from E type memories only)
A55	BMDECCU-	MEMORY DATA ERROR-CORRECTION-CODE- -UNCORRECTABLE: (from E type memories only)
A58	BMDPEL-	MEMORY DATA PARITY ERROR, LEFT BYTE
A59	BMDPER-	MEMORY DATA PARITY ERROR, RIGHT BYTE
A27	BMA95-	MEMORY ADDRESS BUS: (BMA95 thru BMA16)
A28	BMA96-	
A29	BMA97-	
A31	BMA98-	
B5	BMA99-	
B6	BMA00-	
B7	BMA01-	
B8	BMA02-	
B9	BMA03-	
B10	BMA04-	
B11	BMA05-	
B12	BMA06-	MEMORY ADDRESS BIT PATTERN:
B13	BMA07-	
B14	BMA08-	MSB LSB
B15	BMA09-	9 9 9 9 9 0 1 1 1 1 1 1 1
B16	BMA10-	5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6
B17	BMA11-	
B18	BMA12-	
B19	BMA13-	
B20	BMA14-	
B21	BMA15-	
B22	BMA16-	

TABLE 4-7: BACKPLANE SIGNAL LIST (Cont.)

BACKPLANE PIN NO.	SIGNAL NAME	DESCRIPTION
A46	BMAAP-	MEMORY ADDRESS PARITY BIT for BMA-BITS 95 to 00
B23	BMALP-	MEMORY ADDRESS LEFT PARITY BIT for BMA-BITS 1 to 8
B24	BMARP-	MEMORY ADDRESS RIGHT PARITY BIT for BMA-BITS 9 to 16
A56	BMAPEL+	MEMORY ADDRESS PARITY ERROR LEFT on BMA95 to 08, BMAAP and BMALP.
A57	BMAPER+	MEMORY ADDRESS PARITY ERROR RIGHT on BMA09 TO 16 and BMARP.
A36	BMCXDV-	MEMORY EXTERNAL DATA VALID
B04	BMCWWM-	MEMORY CONTROL WIDE WORD
A40	BMCXPER-	EXTERNAL MEMORY PARITY ERROR
B64	BMCDonA-	MEMORY CONTROL DATA ON ADDRESS LINES
B65	BPD01+	PERIPHERAL DATA BUS: (BPD01 thru BPD16)
B67	BPD02+	
B68	BPD03+	
B69	BPD04+	PERIPHERAL DATA-BIT PATTERN:
B70	BPD05+	
B71	BPD06+	MSB LSB
B72	BPD07+	1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
B73	BPD08+	LEFT BYTE RIGHT BYTE
B74	BPD09+	
B75	BPD10+	
B76	BPD11+	
B79	BPD12+	
B81	BPD13+	
B82	BPD14+	
B83	BPD15+	
B84	BPD16+	
B63	BPDLP+	PERIPHERAL DATA LEFT BYTE PARITY BIT
B66	BPDRP+	PERIPHERAL DATA RIGHT BYTE PARITY BIT
B45	BPDPEL-	PERIPHERAL DATA PARITY ERROR, LEFT BYTE
B47	BPDPER-	PERIPHERAL DATA PARITY ERROR, RIGHT BYTE
B29	BPA01+	PERIPHERAL ADDRESS BUS* (BPA99 thru BPA16)
B31	BPA02+	
B32	BPA03+	
B33	BPA04+	PERIPHERAL ADDRESS BIT PATTERN:
B34	BPA05+	
B35	BPA06+	MSB LSB
B36	BPA07+	99 00 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
B37	BPA08+	LEFT BYTE RIGHT BYTE
B38	BPA09+	

TABLE 4-7: BACKPLANE SIGNAL LIST (Cont.)

BACKPLANE PIN NO.	SIGNAL NAME	DESCRIPTION
B39	BPA10+	NOTE: FOR PARITY CHECKING AND GENERATION
B40	BPA11+	PURPOSES, BITS 99 AND 00 ARE NOT
B51	BPA12+	INCLUDED DURING GENERATION OR CHECKING
B52	BPA13+	BY THE CPU.
B53	BPA14+	
B54	BPA15+	
B55	BPA16+	
B49	BPA99+	
B50	BPA00+	
B56	BPALP+	PERIPHERAL ADDRESS PARITY BIT for BPA01 to 08
B58	BPARP+	PERIPHERAL ADDRESS PARITY BIT for BPA09 to 16
B48	BPAPEL-	PERIPHERAL ADDRESS PARITY ERROR on BPA01 - 08, and BPALP (LEFT BYTE)
B60	BPAPER-	PERIPHERAL ADDRESS PARITY ERROR on BPA09 - 16, and BPARP (RIGHT BYTE)
A52	BPCXB-	PERIPHERAL EXTENDER CONTROL B
A53	BPCXA-	PERIPHERAL EXTENDER CONTROL A
A55	BPCAD-	PERIPHERAL EXTENDER ADJUST
A36	BMCXDV-	MEMORY EXTERNAL DATA VALID
A37	BMCEPCS+	EXTENDED PERIPHERAL CONTROL SELECT
B04	BMCWWM-	MEMORY CONTROL WIDE WORD
B93,94	HRUN-	SYSTEM RUN
A41	BPCBSTRB+	DMX BURST MODE STROBE
A40	BMCXPER-	EXTERNAL MEMORY PARITY ERROR
B64	BMCDONA-	MEMORY CONTROL DATA on ADDRESS LINES
A39	SPARE	

4.4.2.3 P850 Multilayer Backplanes

Two new multilayer backplanes are used on the P850 system. The two outer layers are used for signals, while the two inner layers are used for VCC and Ground.

Six mass-terminated, shielded cables are used to interconnect backplanes. Four of these carry I/O signals, while the other two carry Memory Bus signals.

Each of the new backplanes uses the top slot for the mass-terminator pins which are on .100 centers. This results in a 19-slot backplane that fits across two 10-slot chassis and a 16-slot backplane that mounts on a 17-slot chassis.

The 19-slot backplane provides special stitch connections (jumper plug) between its upper and lower chassis. These stitches allow the I/O bus to be connected or not connected between the two chassis.

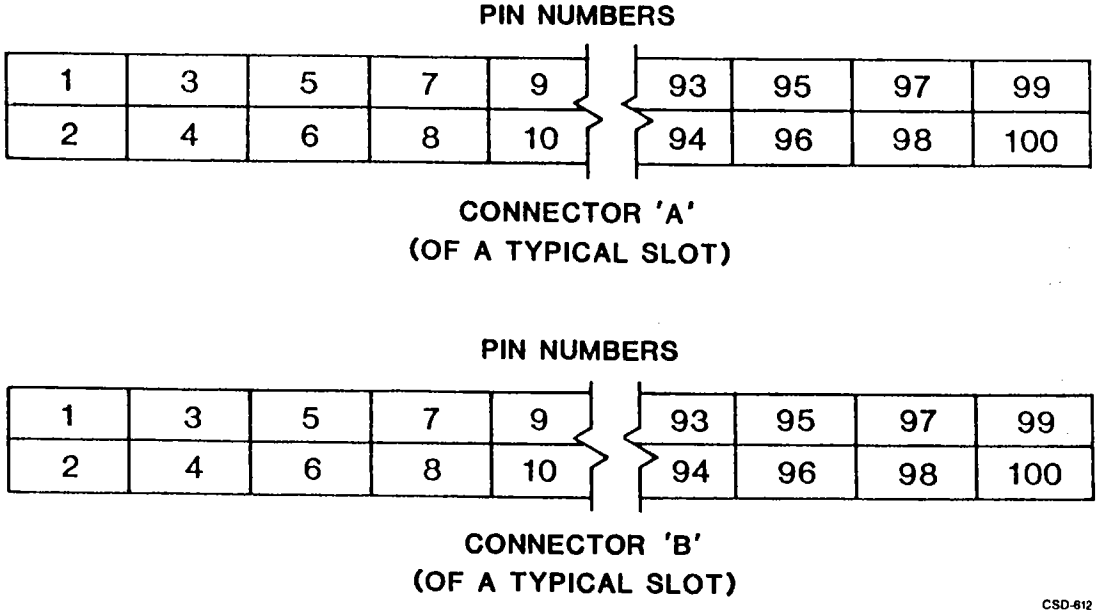


FIGURE 4-27: BACKPLANE (SLOT) PIN NUMBER IDENTIFICATION

A ground strap between the CPU and I/O backplanes is provided.

On the P850, 12 hand wired backplane signals are required. In addition, three pins (OSCOUT+) must be isolated from the rest of the backplane. Modifications to the backplanes for P850 operations may be found on the 35-slot assembly for the P850.

Although the connector pins for the old control panel have been eliminated, a cable has been designed to interface the control panel to the new backplanes.

P850 backplane signals are listed in Table 4-8. These backplanes can be used for P750s as well.

TABLE 4-8: 850 BACKPLANE SIGNAL LIST

PIN	TOP	BOTTOM	19-SLOT INTER CONNECT	I/O	CPU #0	CPU #1	MEMORY
CAx-01			NONE	VCC	VCC	VCC	VCC
CAx-02			NONE	VCC	VCC	VCC	VCC
CAx-03			ETCH	GND	GND	GND	GND
CAx-04	CHT-03	CHB-03	JUMP	BPCDCPN+	BPCDCPN+	BPCDCPN+	
CAx-05	CHT-04	CHB-04	JUMP	BPCDEN+	BPCDEN+	BPCDEN+	
CAx-06			ETCH	GND	GND	GND	GND
CAx-07	CHT-08		JUMP	BPCDPN0-			
CAx-08	CHT-06	CHB-08	JUMP	BPCDPNA-			
CAx-09	CHT-10	CHB-06	JUMP	BPCDPNB-			
CAx-10	CHT-07	CHB-10	JUMP	BPCDPNC-	GND	GND	GND
CAx-11	CHT-12	CHB-07	JUMP	BPCDPND-			

TABLE 4-8: 850 BACKPLANE SIGNAL LIST (Cont.)

PIN	TOP	BOTTOM	19-SLOT INTER CONNECT	I/O	CPU #0	CPU #1	MEMORY
CAx-12	CHT-09	CHB-12	JUMP	BPCDPNE-	OSCOUT+	OSCOUT+	OSCOUT+
CAx-13	CHT-16	CHB-09	JUMP	BPCDPNF-			
CAx-14	CHT-11	CHB-16	JUMP	BPCDPNG-			
CAx-15		CHB-11	JUMP	BPCDPNH-			
CAx-16	CHT-15	CHB-15	JUMP	BPC1EN+	BPC1EN+	BPC1EN+	
CAx-17	CHT-20		NONE	BPC1PN0-			
CAx-18	CHT-17	CHB-20	JUMP	BPC1PNA-			
CAx-19	CHT-22	CHB-17	JUMP	BPC1PNB-			
CAx-20	CHT-19	CHB-22	JUMP	BPC1PNC-			
CAx-21		CHB-17	JUMP	BPC1PND-			
CAx-22			ETCH	GND	GND	GND	GND
CAx-23	CHT-24	CHB-24	JUMP	BPC1CPN+	BPC1CPN+	BPC1CPN+	
CAx-24			ETCH	GND	GND	GND	GND
CAx-25	CHT-23	CHB-23	JUMP	BPCCH1+	BPCCH1+	BPCCH1+	
CAx-26			ETCH	GND	GND	GND	GND
CAx-27	CJT-11	CJB-11	ETCH		BMA95-	BMA95-	BMA95-
CAx-28	CJT-07	CJB-07	ETCH		BMA96-	BMA96-	BMA96-
CAx-29	CJT-09	CJB-09	ETCH		BMA97-	BMA97-	BMA97-
CAx-30	CHT-26	CHB-26	JUMP	BPCE0R+	BPCE0R+	BPCE0R+	IOMST0+
CAx-31	CJT-05	CJB-05	ETCH		BMA98-	BMA98-	BMA98-
CAx-32	CJT-03	CJB-03	ETCH		BMCSELD-	BMCSELD-	BMCSELD-
CAx-33	CJT-04	CJB-04	ETCH		BMC1NLV-	BMC1NLV-	BMC1NLV-
CAx-34	CJT-08	CJB-08	ETCH		BMCEBL-	BMCEBL-	BMCEBL-
CAx-35	CJT-10	CJB-10	ETCH		BMC1+	BMC1+	BMC1+
CAx-36			NONE		OTHERBOWN-	OTHERBOWN-	
CAx-37			NONE	BPCEPCS+	IOMST0+	IOMST1+	IOMST1+
CAx-38	CHT-28	CHB-28	JUMP	BPC1OV1-	BPC1OV1-	BPC1OV1-	
CAx-39			NONE		APINTOP-	APINBOT-	
CAx-40	CJT-16	CJB-16	ETCH		BMCXPER-	BMCXPER-	BMCXPER-
CAx-41	CHT-30	CHB-30	JUMP	BPCBSTRB+	BPCBSTRB+	BPCBSTRB+	
CAx-42			ETCH	GND	GND	GND	GND
CAx-43	CJT-17	CJB-17	ETCH		BMA94-	BMA94-	BMA94-
CAx-44	CJT-13	CJB-13	ETCH		BMDECCC-	BMDECCC-	BMDECCC-
CAx-45	CJT-18	CJB-18	ETCH		BMDECCU-	BMDECCU-	BMDECCU-
CAx-46	CJT-15	CJB-15	ETCH		BMAAP-	BMAAP-	BMAAP-
CAx-47	CJT-19	CJB-19	ETCH		BMCWDLL+	BMCWDLL+	BMCWDLL+
CAx-48			ETCH	GND	GND	GND	GND
CAx-49			NONE	VCC	VCC	VCC	VCC
CAx-50			NONE	VCC	VCC	VCC	VCC
CAx-51	CJT-22	CJB-22	ETCH		BMCADL+	BMCADL+	BMCADL+
CAx-52			NONE		MYBREQ-	MYBREQ-	
CAx-53			NONE		OTHERBREQ-	OTHERBREQ-	
CAx-54			NONE	PS60CY+	PS60CY+	PS60CY+	PS60CY+
CAx-55			NONE		MYBOWN-	MYBOWN-	
CAx-56	CJT-26	CJB-26	ETCH		BMAPEL+	BMAPEL+	BMAPEL+
CAx-57	CJT-30	CJB-30	ETCH		BMAPER+	BMAPER+	BMAPER+
CAx-58	CJT-28	CJB-28	ETCH		BMDPEL-	BMDPEL-	BMDPEL-
CAx-59	CJT-31	CJB-31	ETCH		BMDPER-	BMDPER-	BMDPER-
CAx-60			ETCH	GND	GND	GND	GND
CAx-61	CJT-34	CJB-34	ETCH		BMD01+	BMD01+	BMD01+
CAx-62	CJT-32	CJB-32	ETCH		BMD02+	BMD02+	BMD02+

TABLE 4-8: 850 BACKPLANE SIGNAL LIST (Cont.)

PIN	TOP	BOTTOM	19-SLOT INTER CONNECT	I/O	CPU #0	CPU #1	MEMORY
CAx-63	CJT-36	CJB-36	ETCH		BMD03+	BMD03+	BMD03+
CAx-64	CJT-35	CJB-35	ETCH		BMD04+	BMD04+	BMD04+
CAx-65	CJT-38	CJB-38	ETCH		BMD05+	BMD05+	BMD05+
CAx-66	CJT-37	CJB-37	ETCH		BMD06+	BMD06+	BMD06+
CAx-67	CJT-40	CJB-40	ETCH		BMD07+	BMD07+	BMD07+
CAx-68	CJT-39	CJB-39	ETCH		BMD08+	BMD08+	BMD08+
CAx-69	CJT-42	CJB-42	ETCH		BMD09+	BMD09+	BMD09+
CAx-70	CJT-41	CJB-41	ETCH		BMD10+	BMD10+	BMD10+
CAx-71	CJT-44	CJB-44	ETCH		BMD11+	BMD11+	BMD11+
CAx-72	CJT-43	CJB-43	ETCH		BMD12+	BMD12+	BMD12+
CAx-73	CJT-46	CJB-46	ETCH		BMD13+	BMD13+	BMD13+
CAx-74	CJT-45	CJB-45	ETCH		BMD14+	BMD14+	BMD14+
CAx-75	CJT-48	CJB-48	ETCH		BMD15+	BMD15+	BMD15+
CAx-76	CJT-47	CJB-47	ETCH		BMD16+	BMD16+	BMD16+
CAx-77	CKT-11	CKB-11	ETCH		BMDLP+	BMDLP+	BMDLP+
CAx-78	CKT-13	CKB-13	ETCH		BMDRP+	BMDRP+	BMDRP+
CAx-79	CKT-04	CKB-04	ETCH		BMCSELC-	BMCSELC-	BMCSELC-
CAx-80			ETCH	GND	GND	GND	GND
CAx-81	CKT-03	CKB-03	ETCH		BMCSELB-	BMCSELB-	BMCSELB-
CAx-82	CKT-12	CKB-12	ETCH		BMCSELV-	BMCSELV-	BMCSELV-
CAx-83	CKT-14	CKB-14	ETCH		BMCD1NH-	BMCD1NH-	BMCD1NH-
CAx-84	CKT-08	CKB-08	ETCH		BMCWRB-	BMCWRB-	BMCWRB-
CAx-85			NONE		APNMINTOP-	APNMINBOT-	Spare
CAx-86	CKT-07	CKB-07	ETCH		BMCRFSH-	BMCRFSH-	BMCRFSH-
CAx-87	CKT-17	CKB-17	ETCH		APEMODE-	APEMODE-	APEMODE-
CAx-88	CKT-15	CKB-15	ETCH		BCPUNUM-	BCPUNUM-	BCPUNUM-
CAx-89			NONE		BMCEXS2-	BMCEXS2-	BMCEXS2-
CAx-90	CLT-07	CLB-07	ETCH	BPCFCLK+	BPCFCLK+	BPCFCLK+	
CAx-91			NONE		BMCSS01-	BMCSS01-	BMCSS01-
CAx-92	CLT-05	CLB-05	ETCH	BPC1RQ-	BPC1RQ-	BPC1RQ-	BMSTCPU1+
CAx-93			NONE		BMCSS02-	BMCSS02-	BMCSS02-
CAx-94	CLT-03	CLB-03	ETCH	BPCDRQ-	BPCDRQ-	BPCDRQ-	BMSTCPU0+
CAx-95			NONE		BMCSS03-	BMCSS03-	BMCSS03-
CAx-96	CKT-18	CKB-18	ETCH		BMCPRCH-	BMCPRCH-	BMCPRCH-
CAx-97	CKT-20	CKB-20	ETCH		BMCMML-	BMCMML-	BMCMML-
CAx-98			ETCH	GND	GND	GND	GND
CAx-99			NONE	VCC2	VCC2	VCC2	VCC2
CAx-00			NONE	VCC2	VCC2	VCC2	VCC2
CBx-01			NONE	VCC	VCC	VCC	VCC
CBx-02			NONE	VCC	VCC	VCC	VCC
CBx-03			ETCH	GND	GND	GND	GND
CBx-04	CKT-21	CKB-21	ETCH		BMCWWM-	BMCWWM-	BMCWWM-
CBx-05	CKT-26	CKB-26	ETCH		BMA99-	BMA99-	BMA99-
CBx-06	CKT-22	CKB-22	ETCH		BMA00-	BMA00-	BMA00-
CBx-07	CKT-30	CKB-30	ETCH		BMA01-	BMA01-	BMA01-
CBx-08	CKT-24	CKB-24	ETCH		BMA02-	BMA02-	BMA02-
CBx-09	CKT-27	CKB-27	ETCH		BMA03-	BMA03-	BMA03-
CBx-10	CKT-25	CKB-25	ETCH		BMA04-	BMA04-	BMA04-
CBx-11	CKT-29	CKB-29	ETCH		BMA05-	BMA05-	BMA05-
CBx-12	CKT-28	CKB-28	ETCH		BMA06-	BMA06-	BMA06-

TABLE 4-8: 850 BACKPLANE SIGNAL LIST (Cont.)

PIN	TOP	BOTTOM	19-SLOT INTER CONNECT	I/O	CPU #0	CPU #1	MEMORY
CBx-13	CKT-31	CKB-31	ETCH		BMA07-	BMA07-	BMA07-
CBx-14	CKT-32	CKB-32	ETCH		BMA08-	BMA08-	BMA08-
CBx-15	CKT-33	CKB-33	ETCH		BMA09-	BMA09-	BMA09-
CBx-16	CKT-34	CKB-34	ETCH		BMA10-	BMA10-	BMA10-
CBx-17	CKT-35	CKB-35	ETCH		BMA11-	BMA11-	BMA11-
CBx-18	CKT-36	CKB-36	ETCH		BMA12-	BMA12-	BMA12-
CBx-19	CKT-37	CKB-37	ETCH		BMA13-	BMA13-	BMA13-
CBx-20	CKT-38	CKB-38	ETCH		BMA14-	BMA14-	BMA14-
CBx-21	CKT-39	CKB-39	ETCH		BMA15-	BMA15-	BMA15-
CBx-22	CKT-40	CKB-40	ETCH		BMA16-	BMA16-	BMA16-
CBx-23	CKT-41	CKB-41	ETCH		BMALP-	BMALP-	BMALP-
CBx-24	CKT-42	CKB-42	ETCH		BMARP-	BMARP-	BMARP-
CBx-25	CKx-48	=CLx-20	JUMP	HPWRFL-	HPWRFL-	HPWRFL-	HPWRFL-
CBx-26			ETCH	GND	GND	GND	GND
CBx-27			NONE	HPFRLY+	HPFRLY+	HPFRLY+	HPFRLY+
CBx-28			NONE		BMSTCPU0+	BMSTCPU1+	SPARE
CBx-29	CLT-22	CLB-22	JUMP	BPA01+	BPA01+	BPA01+	
CBx-30			ETCH	GND	GND	GND	GND
CBx-31	CLT-24	CLB-24	JUMP	BPA02+	BPA02+	BPA02+	
CBx-32	CLT-23	CLB-23	JUMP	BPA03+	BPA03+	BPA03+	
CBx-33	CLT-26	CLB-26	JUMP	BPA04+	BPA04+	BPA04+	
CBx-34	CLT-25	CLB-25	JUMP	BPA05+	BPA05+	BPA05+	
CBx-35	CLT-28	CLB-28	JUMP	BPA06+	BPA06+	BPA06+	
CBx-36	CLT-27	CLB-27	JUMP	BPA07+	BPA07+	BPA07+	
CBx-37	CLT-30	CLB-30	JUMP	BPA08+	BPA08+	BPA08+	
CBx-38	CLT-29	CLB-29	JUMP	BPA09+	BPA09+	BPA09+	
CBx-39	CLT-32	CLB-32	JUMP	BPA10+	BPA10+	BPA10+	
CBx-40	CLT-31	CLB-31	JUMP	BPA11+	BPA11+	BPA11+	
CBx-41	CKx-47	=CMx-04	JUMP	HSYSCLR-	HSYSCLR-	HSYSCLR-	HSYSCLR-
CBx-42			ETCH	GND	GND	GND	GND
CBx-43	CKT-45	CKB-45	ETCH		BRING0+	BRING0+	BRING0+
CBx-44			NONE	PSRLY+	PSRLY+	PSRLY+	PSRLY+
CBx-45	CMT-06	CMB-06	JUMP	BPDPEL-	BPDPEL-	BPDPEL-	
CBx-46			ETCH	GND	GND	GND	GND
CBx-47	CMT-08	CMB-08	JUMP	BPDPER-	BPDPER-	BPDPER-	
CBx-48	CMT-03	CMB-03	JUMP	BPAPEL-	BPAPEL-	BPAPEL-	
CBx-49	CMT-10	CMB-10	JUMP	BPA99+	BPA99+	BPA99+	
CBx-50	CMT-07	CMB-07	JUMP	BPA00+	BPA00+	BPA00+	
CBx-51	CMT-12	CMB-12	JUMP	BPA12+	BPA12+	BPA12+	
CBx-52	CMT-09	CMB-09	JUMP	BPA13+	BPA13+	BPA13+	
CBx-53	CMT-14	CMB-14	JUMP	BPA14+	BPA14+	BPA14+	
CBx-54	CMT-11	CMB-11	JUMP	BPA15+	BPA15+	BPA15+	
CBx-55	CMT-16	CMB-16	JUMP	BPA16+	BPA16+	BPA16+	
CBx-56	CMT-13	CMB-13	JUMP	BPALP+	BPALP+	BPALP+	
CBx-57			ETCH	GND	GND	GND	GND
CBx-58	CMT-15	CMB-15	JUMP	BPARP+	BPARP+	BPARP+	
CBx-59	CMT-20	CMB-20	JUMP	BPCP10+	BPCP10+	BPCP10+	
CBx-60	CMT-19	CMB-19	JUMP	BPAPER-	BPAPER-	BPAPER-	
CBx-61	CMT-22	CMB-22	JUMP	BPC60CY+	BPC60CY+	BPC60CY+	
CBx-62	CMT-23	CMB-23	JUMP	BPCREDY-	BPCREDY-	BPCREDY-	
CBx-63	CMT-24	CMB-24	JUMP	BPDLP+	BPDLP+	BPDLP+	

TABLE 4-8: 850 BACKPLANE SIGNAL LIST (Cont.)

PIN	TOP	BOTTOM	19-SLOT INTER CONNECT	I/O	CPU #0	CPU #1	MEMORY
CBx-64	CKT-43	CKB-43	ETCH		BMCDONA-	BMCDONA-	BMCDONA-
CBx-65	CMT-28	CMB-28	JUMP	BPD01+	BPD01+	BPD01+	APINTOP-
CBx-66	CMT-25	CMB-25	JUMP	BPDRP+	BPDRP+	BPDRP+	APINBOT-
CBx-67	CMT-30	CMB-30	JUMP	BPD02+	BPD02+	BPD02+	APNMINTOP-
CBx-68	CMT-27	CMB-27	JUMP	BPD03+	BPD03+	BPD03+	APNMINBOT-
CBx-69	CMT-32	CMB-32	JUMP	BPD04+	BPD04+	BPD04+	
CBx-70	CMT-31	CMB-31	JUMP	BPD05+	BPD05+	BPD05+	
CBx-71	CNT-04	CNB-04	JUMP	BPD06+	BPD06+	BPD06+	
CBx-72	CNT-03	CNB-03	JUMP	BPD07+	BPD07+	BPD07+	
CBx-73	CNT-06	CNB-06	JUMP	BPD08+	BPD08+	BPD08+	
CBx-74	CNT-05	CNB-05	JUMP	BPD09+	BPD09+	BPD09+	
CBx-75	CNT-08	CNB-08	JUMP	BPD10+	BPD10+	BPD10+	
CBx-76	CNT-07	CNB-07	JUMP	BPD11+	BPD11+	BPD11+	
CBx-77			NONE	V12-	V12-	V12-	V12-
CBx-78			NONE	V12-	V12-	V12-	V12-
CBx-79	CNT-10	CNB-10	JUMP	BPD12+	BPD12+	BPD12+	
CBx-80			ETCH	GND	GND	GND	GND
CBx-81	CNT-12	CNB-12	JUMP	BPD13+	BPD13+	BPD13+	
CBx-82	CNT-09	CNB-09	JUMP	BPD14+	BPD14+	BPD14+	
CBx-83	CNT-14	CNB-14	JUMP	BPD15+	BPD15+	BPD15+	
CBx-84	CNT-11	CNB-11	JUMP	BPD16+	BPD16+	BPD16+	
CBx-85	CNT-16	CNB-16	JUMP	BPCM0D0+	BPCM0D0+	BPCM0D0+	
CBx-86	CNT-13	CNB-13	JUMP	BPCM0D1+	BPCM0D1+	BPCM0D1+	
CBx-87	CNT-18	CNB-18	JUMP	BPCM0D2+	BPCM0D2+	BPCM0D2+	
CBx-88	CNT-15	CNB-15	JUMP	BPCM0D3+	BPCM0D3+	BPCM0D3+	
CBx-89	CNT-20	CNB-20	JUMP	BPC1NMD+	BPC1NMD+	BPC1NMD+	
CBx-90	CNT-17	CNB-17	JUMP	BPCSCLK+	BPCSCLK+	BPCSCLK+	
CBx-91			NONE	V12+	V12+	V12+	V12+
CBx-92			NONE	V12+	V12+	V12+	V12+
CBx-93	CNT-24	CNB-24	JUMP	HRUN-	HRUN-	HRUN-	HRUN-
CBx-94	CNT-22	CNB-22	JUMP	HRUN-	HRUN-	HRUN-	HRUN-
CBx-95	CNT-28	CNB-28	JUMP	BPCSTRB+	BPCSTRB+	BPCSTRB+	
CBx-96			ETCH	GND	GND	GND	GND
CBx-97			NONE	VSS	VSS	VSS	VSS
CBx-98			NONE	VSS	VSS	VSS	VSS
CBx-9	CNT-31	CNB-31	JUMP	SPARE	SPARE	SPARE	SPARE
CBx-00			ETCH	SPARE	SPARE	SPARE	SPARE

4.5 PERIPHERAL I/O CONTROLLERS

This section presents the basic functions, as well as logical descriptions of Prime peripheral controllers. The following controllers are discussed in this section:

- Disk Controllers
- Magnetic Tape Controllers (MTC)
- Unit Record Controller (URC)

- System Option Controller (SOC)

For any additional information on these or other Prime controllers, refer to the service manual for the particular device.

4.5.1 CONTROLLER FUNCTION

Peripheral I/O controllers provide a means of communicating data between external devices and the CPU. As illustrated in Figure 4-28, an I/O bus common to all controllers and the CPU, makes communications possible. The I/O Bus consists of the BPA (Peripheral Address Bus), the BPD (Peripheral Data Bus) and the Peripheral Command Bus (BPC). The CPU places a PIO command on the BPC. The controller with the correct device address responds to the instruction.

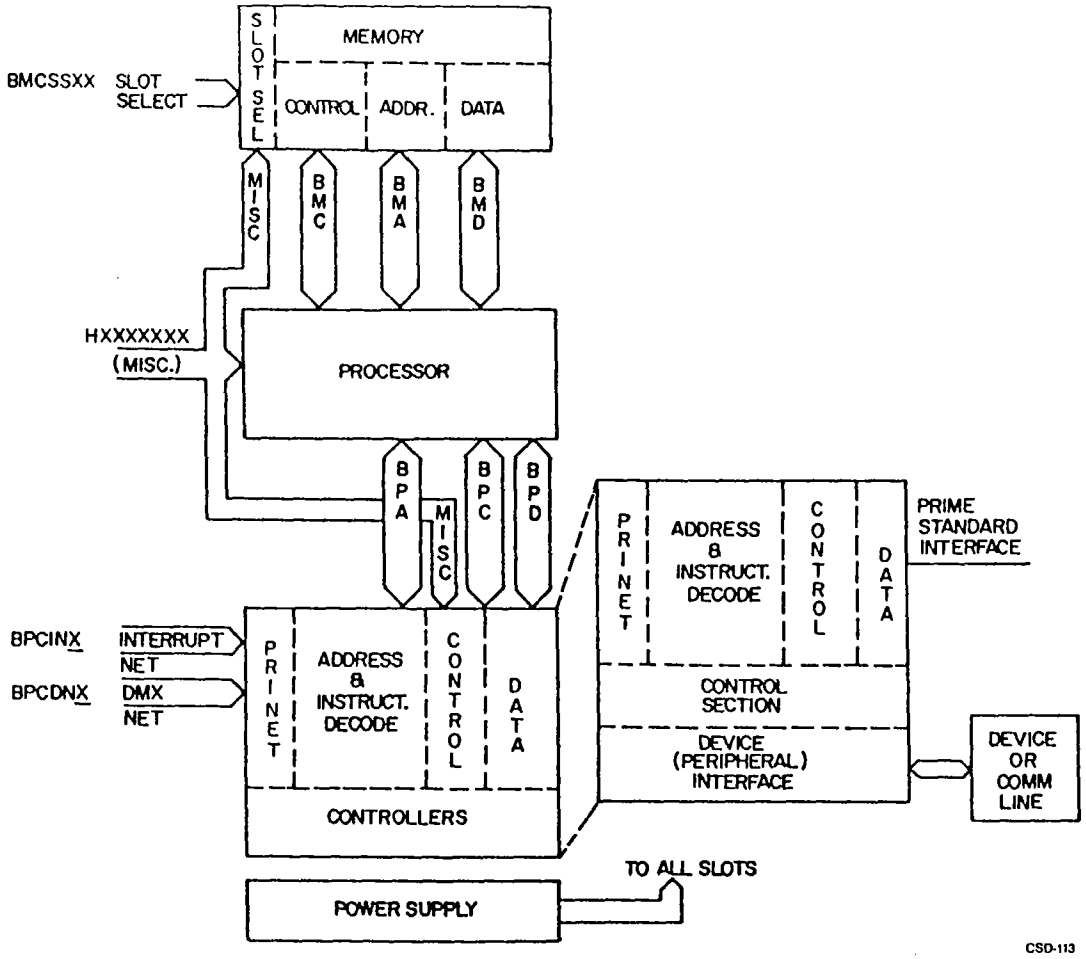


FIGURE 4-28: I/O AND MEMORY BUSES

Controller device addresses are not determined by slot selection, the way memory boards are. Each controller in the system has a unique device address hardwired on the board. In systems with identical model controllers, the device addresses must be different, so the CPU can send instructions to the correct device. The device address on all identical controllers, except the first, must be changed. This is described in Chapter 2 of this manual as well as in the Service Manual for the device.

4.5.2 CONTROLLER LOGIC BLOCKS

A controller consists of three major logic blocks:

- I/O Bus Interface Logic - interfaces the controller with the CPU. Since this logic is standard, it is nearly identical, both physically and logically, on all controllers.

- Peripheral Device Interface - interfaces the control section logic to the peripheral device or communications link. For example, the EIA or 20mA drivers and Universal Asychronous Receiver/Transmitters (UARTs), that actually drive the communication lines on an AMLC, are part of the peripheral device interface for the AMLC controller.

- Control Section Logic - provides control over the conversion of data and commands from the CPU, to a format compatible with the output device. This logic interfaces the other two logic blocks and is the heart of the controller.

4.5.3 DISK CONTROLLER (SMC)

The disk controllers, model 4005 (burst mode), interface the SMDs, CMDs, and FMDs to the CPU. Disk controller operation is detailed in the Service Manual for the disk device.

4.5.4 MAGNETIC TAPE CONTROLLER (MTC)

The magnetic tape controller, with a remote or integrated formatter, interfaces the tape drive to the CPU. Each model of the tape controller is slightly modified to accomodate the variety of tape drives, from 556 bpi 7-track 45 ips models to the Telex 6250 bpi 9-track 125 ips model.

Magnetic tape devices transfer data via DMA and burst mode. The controller uses PIO commands (not DMA channels) to initialize itself. Magnetic tape controller operation is detailed in the service manual for the tape device.

4.5.5 UNIT RECORD CONTROLLER (URC)

The URC, or MPC board, interfaces record oriented devices, such as line printers and cardreaders.

4.5.6 SYSTEM OPTION CONTROLLER (SOC)

Originally the SOC board provided the serial interface for the system console and the serial printer. Since the development of the VCP, the SOC is used to interface the printer/plotters and papertape devices.

4.6 COMMUNICATIONS I/O CONTROLLERS

Communications controllers operate synchronously and asynchronous, transferring variable size blocks of data at speeds of 2 to 56 Kbyte baud.

Prime offers several products designed for synchronous and asynchronous communication, among them:

- PRIMENET Node Controller (PNC) - along with PRIMENET software is used to connect several Prime machines (hosts or nodes) into a local ring network.

- Asynchronous Multi-Line Controller - allows interfacing between user terminals and the host system.

- Multi-Data Link Controller (MDLC) - provides interface between a Prime host and a packet-switching network or another type of host; such as IBM, CDC, UNIVAC, and Honeywell.

- Intelligent Communications Subsystem (ICS1 & ICS2) - provides interaction with a Prime host to provide increased flexibility and control in data communications networking.

It is possible to configure a very large network over hundreds of miles, using a combination of Prime systems with PNCs and MDLCs, and packet switching networks.

Prime communications hardware is supported by software products other than PRIMENET. Remote Job Entry (RJE) allows an interactive Prime host to network with, and simulate, the batch operation of large mainframes, such as IBM and UNIVAC. Distributed Processing (DPTX) networks a Prime host to an IBM 3270. Transparent to the users, all terminals can communicate directly with either host. All resources of both systems are shared.

4.6.1 PRIMENET NODE CONTROLLER

Prime systems can be networked together using the PRIMENET Node Controller (PNC). Each node in the network is equipped with a PNC. Each system also has a junction box connection to the ring. In that way, one node can be disconnected from the network without effecting the rest of the ring. The systems are cabled together so the transmit side of one junction box feeds into the receive side of the next junction box, all the way around the ring. All systems in the ring must be no more than 750 feet apart. A basic PNC network is shown in Figure 4-29.

4.6.1.1 PRIMENET Network Information

Information transmitted or received on a PRIMENET network is in a token or a packet.

The token is a unique 12-bit pattern which is either on the network alone, or following the trailer portion of the last packet on the network. When a PNC wants to transmit, it first must detect a token. If the receive side of the PNC receives another token, while the transmit side is transmitting, it sets the Multiple Token Status Bit, then removes and buffers the received token and packet. Once the transmit side has finished sending the packet, the PNC goes from Transmit to Transceive mode. That is, it examines the packets (and tokens) received, passing them around the ring if the receive address is not its own.

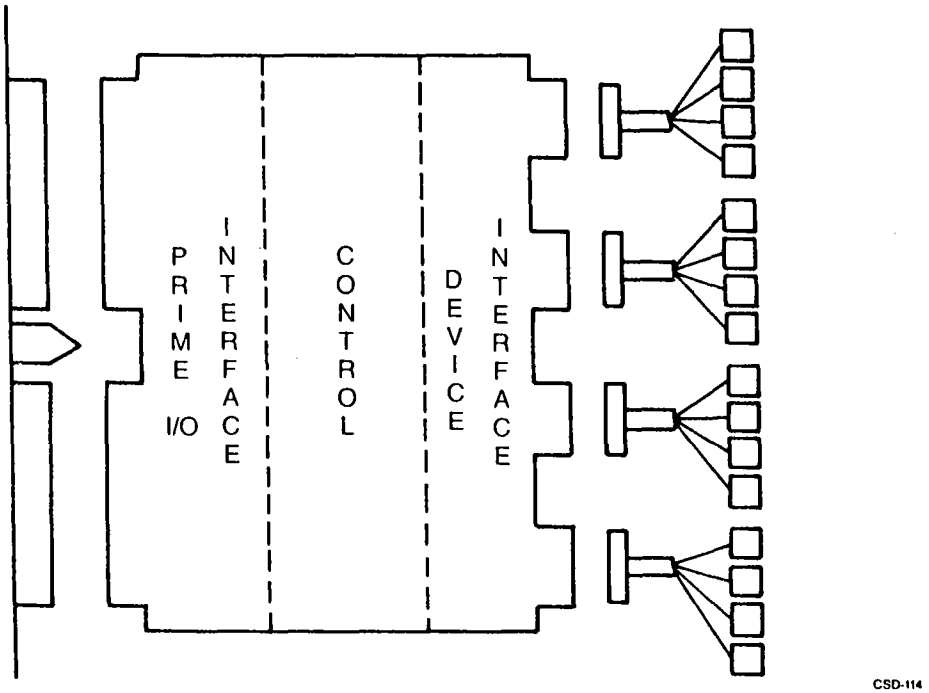


FIGURE 4-29: PNC NETWORK

The packet is made up of three parts: header, data and trailer. The packet size ranges from two to 1022 words. The 12-bit leading frame, which identifies the beginning of the packet, is the first part of the header. The rest of the header is supplied by PRIMENET software: the receive node address, the transmit node address, the packet type (not currently used), and the retry count (0 for transmitted messages). The data portion of the packet contains the protocol and the message being sent. This too, is supplied by the software.

The trailer has several parts. The Cyclical Redundancy Check (CRC) is the parity checking mechanism. This is followed by the 12 bit Acknowledgement Frame, which signals the end of the CRC and the beginning of the AC and the Acknowledgement Byte. The information in these two locations is used by the PNC to indicate that the message was transmitted successfully. The PRIMENET software also uses the information to report status to the CPU. The last part of the trailer is a 12-bit trailing frame, which signals the end of the packet.

4.6.1.2 PRIMENET Network Operation

During PNC operation (see Figure 4-30), a token constantly goes around the ring. When Host A wants to send data to Host E, Host A takes the token off the ring and stores it in a buffer. Through the PRIMENET software, it writes its own address and the receiving node's 8 bit address in the header portion of a packet on the PNC transmit side. It writes the message in the data portion of the packet, then puts the packet and token back on the ring.

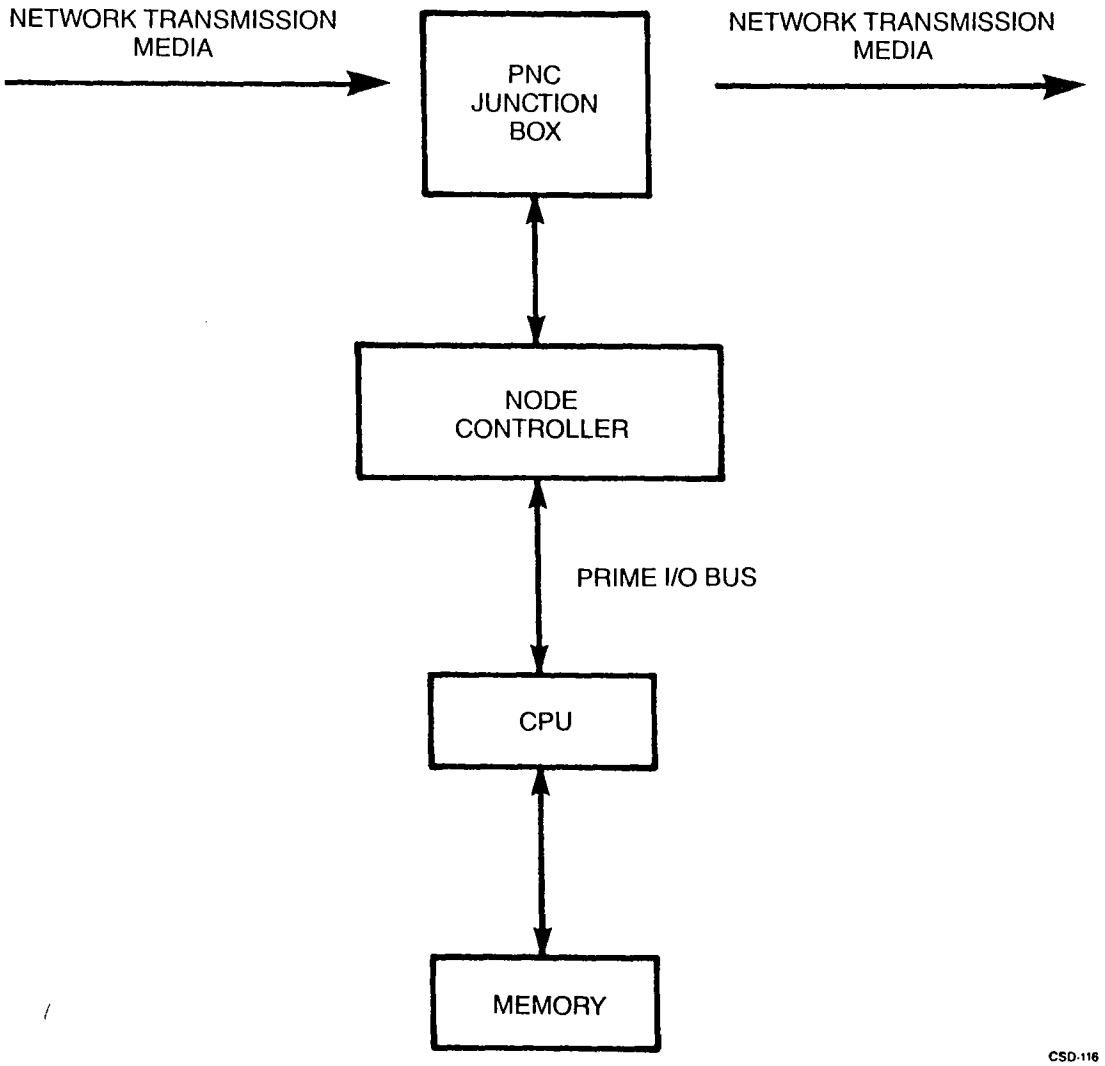


FIGURE 4-30: PRIMENET NODE DATA FLOW

Each system receives the token on its receive side, reads the node address, and retransmits the packet and token to the next node on the ring. When Host E receives the packet, it recognizes the node address as its own, and retransmits the packet around the ring. Host E also buffers the packet, checks the CRC and Acknowledgement Check (AC) and writes to the AC. If the CRC and AC check, the PNC interrupts the CPU and passes the data via DMA or DMC.

The PRIMENET software notifies the PNC that the data was successfully transferred to user space. The PNC then modifies the Acknowledgement Byte and AC to reflect the action taken, then puts the packet back on the ring. The token and packet pass on around the ring, read by each node, until they arrive back at Host A. Host A buffers and removes the packet. It will interrupt the CPU, which will, in turn, report the status of the transmission. The CPU acknowledges the interrupt. Then Host A puts the token back on the ring. The token continually passes around the ring until another node wants to send a message.

If the receiving node detected a CRC error, it does not modify the AC or Acknowledgement Byte. The transmitting node reports this as an error to its CPU; PRIMENET software will retransmit the message.

4.6.2 ASYNCHRONOUS MULTI-LINE CONTROLLER (AMLC)

The Asynchronous Multi-Line Controller (AMLC) is a communications controller that allows interfacing between user terminals (and some serial devices), and the Prime computer. An AMLC consists of eight or sixteen individual channels, depending on the model number. A basic diagram of an AMLC is shown in Figure 4-31.

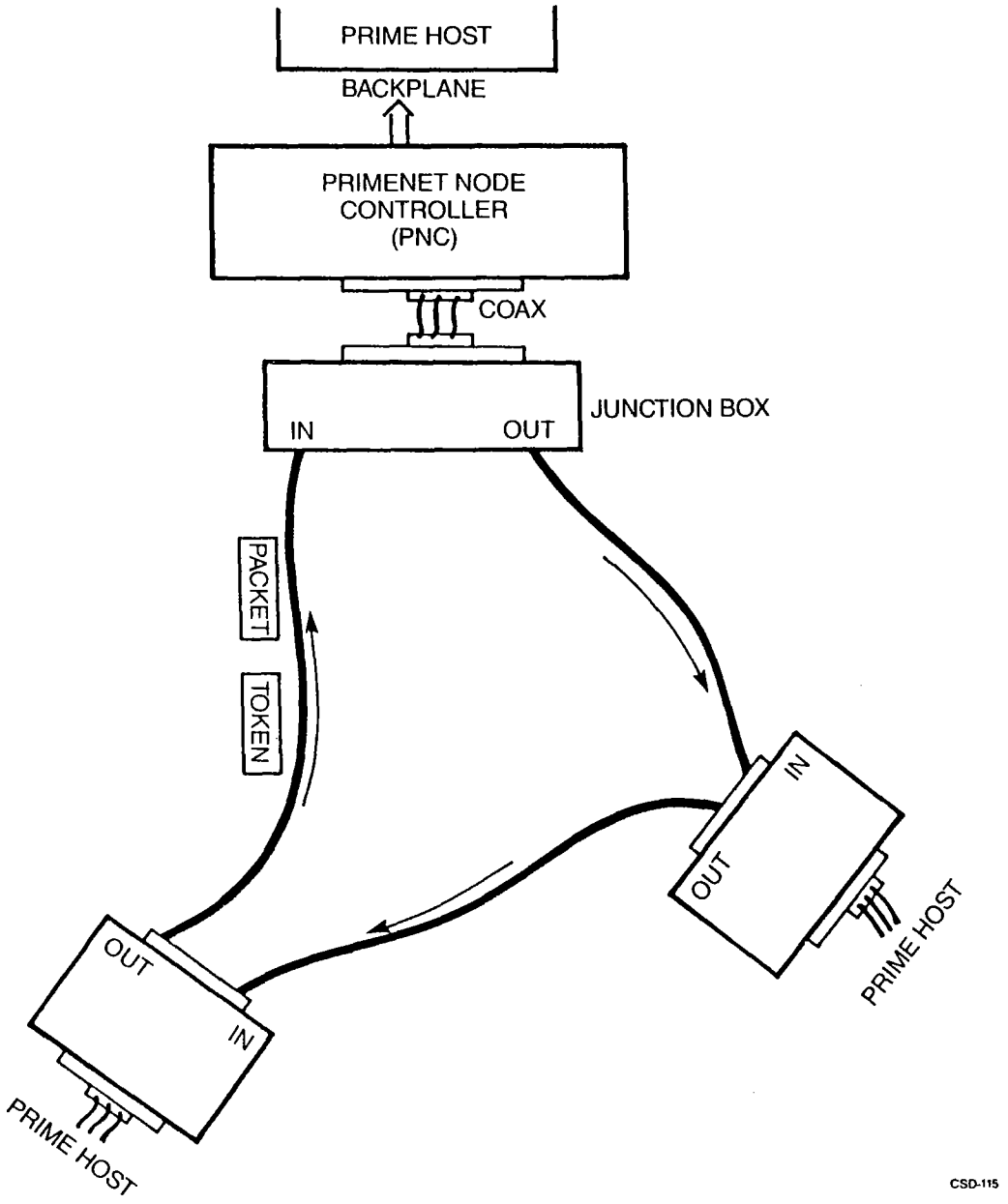


FIGURE 4-31: AMLC: BASIC DIAGRAM

Each channel connects directly to a user terminal, or connects a user terminal via industry type 103/113/202 data sets. Also, each channel operates independently of the others. A channel may be set to operate in full or half-duplex mode, and at any selectable baud rate, without affecting the operation of the other channels. Line types (channels) may be RS232-C/CCITT, V24, or 20mA compatible terminals.

PRIMOS supports up to eight AMLCs. The maximum number of terminals is one less than the number of lines. PRIMOS uses the last line of the last AMLC for interrupt timing.

The AMLC comes in two versions:

- QAMLC (High Performance AMLC)
- AMLC (Standard Performance)

These versions are described in the following subsections.

4.6.2.1 AMLC & QAMLC Functional Operation

The QAMLC, or High Performance AMLC, is an AMLC with additional functions. The QAMLC can use Direct Memory Queue (DMQ) to output data from the CPU whereas the AMLC can only use Direct Memory Transfer (DMT).

During DMQ, output data is stored in blocks or queues, rather than in dedicated locations. Queueing (DMQ) is a performance feature that reduces the amount of software overhead and enables faster transfer of data.

A QAMLC can operate in standard mode like the AMLC, or it can operate in the high performance (DMQ) mode. The AMLC is able to use DMQ mode via a single OCP instruction (OCP '1354).

NOTE

Because nearly all new systems are shipped with QAMLCs, the term AMLC often refers to both the AMLC and the QAMLC.

For each of the possible data lines, four basic operations are performed within the AMLC:

- Transmit (output) - There are two output signals per AMLC output line. This includes a control signal to the device indicating that the AMLC is ready (or not ready), plus a serial data line.
- Receive (input) - There are two input signals per AMLC input line. The AMLC receives a control signal from the device, indicating that the device is ready (or not ready), plus a serial data line.
- Report Status - On command from the CPU software, the AMLC reports any of its various status and control registers. Included in these registers is the state of the status signal from the device.

- Interrupt the CPU - The AMLC generates several interrupts to the CPU to facilitate programming and notify the CPU of changes in status.

4.6.2.2 AMLC Initialization

Before performing I/O to any user terminal, the AMLC must be initialized, so that the operation of each line is compatible with the attached user terminal. The PRIMOS AMLC command passes configuration parameters to the AMLC controller. There is one command and corresponding control word for each AMLC line. Configuration control bits are provided to select character length, type of parity, and number of stop bits. Both receiver and transmitter have double character buffering. Once configured and initialized, the AMLC operates autonomously to process character traffic.

4.6.2.3 AMLC Transmit Operation

There are two modes of transmission:

- Standard (DMT)
- High performance (DMQ).

In the standard mode of operation, the CPU program places a single character to be transmitted in the dedicated cell, a specific memory location. When the AMLC transmits the character, it uses one DMT cycle to read the cell and a second to zero out the dedicated cell. The AMLC also generates an interrupt to the CPU to indicate that a character has been taken.

In order to transmit a second character the CPU must first test the dedicated cell to ensure that it has been zeroed out (character transmitted). The CPU then stores the next character to be transmitted. This process requires CPU intervention on every character.

The DMQ mode of operation was implemented to reduce the amount of software overhead involved with transmitting data. DMQ eliminates the need for software intervention at each character. The DMQ uses a buffer in the CPU memory to contain the characters to be transmitted. The Queue Control Block is a special group of locations which tells the size and location of the buffer.

Since the CPU's DMQ logic (the microcode) examines and updates the data in the Queue Control Block as data is being transmitted by the AMLC, the entire output buffer can be transmitted without intervention from the CPU.

Once data is taken from the CPU's memory and transferred to the AMLC the operation is identical to the DMT mode of operation, except that the AMLC does not have to zero out the location from which the data character was taken.

4.6.2.4 AMLC Receive Operation

In Direct Memory Access (DMA) and Direct Memory Channel (DMC) modes of operation, the data input to the CPU memory is input to a common buffer area that is shared by all input lines. The operation software examines the line number portion of each data word to determine which AMLC line sent the character.

In preparation to receive data, the software outputs a control word to the AMLC to identify what DMA/DMC channel is to be used for input transfers. Then, the software sets up the transfer's starting address and range. The AMLC uses two consecutive channel pairs, automatically switching from one to the next, each time a buffer is filled (end-of-range). Once the DMA/DMC channel is set up, it remains set up until the AMLC is reinitialized. To input data, DMA/DMC dedicated pair locations must be reintialized each time the end of range is reached.

The sequence of events and data flow for receiving data on an AMLC line is:

1. The AMLC detects the start character (Mark to space transition) and begins inputting the serial character.

2. As the character is entered completely, it is converted from serial to parallel. The parity bit is checked and the start and stop bits are removed.

3. The AMLC forms a 16 bit data word. The data word contains either the AMLC line number and the data character just input, or the line status information.

4. Using the DMA/DMC channel, the AMLC transfers the 16 bit word to the CPU main memory.

4.6.2.5 AMLC Status Reporting

The AMLC uses status words to tell the CPU about AMLC operations. Some of the status words and the uses are as follows:

- AMLC Status Word - When an AMLC interrupt occurs, this status word may be input to determine what type of interrupt happened, the line number associated with the interrupt, and if the AMLC is operating in DMT or DMQ mode.

- Data Set Status Word - Each line of the AMLC has an input status line associated with it. This line may be called by any number of names and tied to any number of points on a modem or terminal. It is the only line the AMLC has to sense whether the device connected to it is ready or not.

- AMLC Identification - This status word identifies the type of AMLC, if it is configured to support DMQ, if it is EIA or Current Loop, and in which slot the board is.

- DMA/DMC (Input) Channel Number - This status word indicates the DMA/DMC channel number for the input data.

- DMT/DMQ (Output) Channel Number - This status word indicates the DMT/DMQ channel number for the output data.

- Interrupt Vector Address - This status word indicates the selected interrupt vector address to be used.

4.6.2.6 AMLC Interrupts

The AMLC can cause external hardware interrupts under the following conditions:

- End-Of-Range - This interrupt is sent from the AMLC to the CPU. It indicates that the buffer the AMLC was filling with data has become full. That is, a complete block of data has been transferred to the CPU. The end of range interrupt is a result of the end of range signal from DMX transfer.

- First-Character-Time Interrupt - This is an interrupt from the AMLC to the CPU. It indicates that the character has been successfully output and the AMLC is ready to transmit another character. It can be enabled or disabled on a line-by-line basis, by a bit in the line configuration control word.

- Second-Character-Time Interrupt - If another character time interrupt occurs while one of the above is pending, a second character time interrupt bit is set in the AMLC status word.

4.6.2.7 UART Functional Operation

The Universal Asynchronous Receiver/Transmitter (UART) is the key Large Scale Integration (LSI) device used on the AMLC. It is a complete subsystem for one AMLC line.

The transmitter portion accepts parallel binary characters from the CPU and converts them to serial characters to send to the device. The receiver portion does the reverse; it converts serial characters from the terminal to parallel binary characters to send to the CPU. Although it is implemented on a single 40 pin IC, this device contains a control register for controlling the number of data bits, stop bits and parity.

Each time the UART needs servicing, it activates one or more of its five status lines. These status lines tell the AMLC's control logic section that data is ready to be transferred to the CPU, data has been transferred successfully to the device, or an error has been detected.

The UART transmitter accepts parallel binary data and places it in a transmitter holding register. Under control of the transmit register clock, it appends the start bit and shifts the character out serially to the end of the character, the transmitter adds the parity bit (if configured for parity), then appends the stop bit. This leaves the line in a Spacing condition.

The receiver's operation is just the reverse. The Word Length Gating logic searches for a MARK to SPACE transition on the serial input line. If this transition is detected, the receiver samples the serial input data at specific timing intervals, based on the baud rate, to detect the data content. Then, the serial character is moved to the

receive register. Next, the character is formed into a parallel character of the proper character length, and all error checks are made. The receiver stores the converted character in the Receiver Holding Register until the AMLC takes it for transfer.

Control lines to the UART load the Transmit Buffer, Inhibit Parity, Master Clear the device, Reset the Receive Data Register, set the character length and control the baud rates.

4.6.3 MULTI-DATA LINK CONTROLLER (MDLC)

The MDLC is a microprogrammed controller designed for synchronous communications. The MDLC provides interface between a Prime host and a packet switching network or another type of host; such as IBM, CDC, UNIVAC, and Honeywell. It replaces the High Speed Synchronous Multi-Line Controller (HSSMLC) and the original product, the Synchronous Multi-Line Controller (SMLC). The terms MDLC and SMLC are often used interchangeably.

Each system can support up to two MDLCs. Each MDLC has two cables; each cable has two full-duplex lines which are usually connected to modems. Each cable can support one protocol, so there is a maximum of two protocols per MDLC.

A protocol is a series of instructions which allows two different machines to communicate. The protocol converts the data word format of one machine into that of another machine. Some of the protocols available on the MDLC are: Bisync, SDLC, HDLC, ICL7020 (U.K.), UT200 (CDC), GRTS (Honeywell), and UNIVAC1004. Bisync is IBM's version of synchronous communication, based on the EPSDIC character set. SDLC is the protocol used specifically by the IBM8100 and 3790 series. HDLC is the X.25 protocol with no specific character set, used by packet switching networks, such as Tymnet.

The basic MDLC microcode is 512 X 48 bit PROM. Two additional PROM are also provided. One provides a one microstep decode of the line status (data mode, buffer full, etc.), to determine the jump address. The other does the same thing for the protocol, decoding special characters and some mode bits.

MDLC operation is similar to the AMLC. Each MDLC line has a Large Scale Integration (LSI) device called the USNRT. The USNRT transmitter converts data from parallel to serial. The USNRT receiver converts data from serial to parallel. Each MDLC has four USNRTs.

Parity checking (CRC) is done with hardware rather than microcode. Eight 24 bit registers in RAM hold the current CRC accumulation for the eight data lines (4 transmit, 4 receive). An additional 8 bit register is used for shifting a character for inclusion in the CRC accumulation. A bank of 16 Exclusive OR nodes is also used to calculate the CRC.

The I/O data register holds the data being transferred. The address register holds the DMA/DMC address of the data being transferred from/to the CPU.

The MDLC uses a sequence of PIO instructions to transfer data. During MDLC initialization, each line's parity, character length, and any

special characters used by the protocol for transmit formatting, are sent with a series of OTA commands. Another OTA command specifies the DMA/DMC address where the data is to be transmitted from/to. On receives, two DMA/DMC addresses are specified. Then, an additional OTA command enables the transmitter/receiver.

During transmits, the MDLC fetches data from memory and stores it in a register location. The data is reformatted according to parity, character, and protocol information; then transmitted down the line. During receives, the MDLC stores data in two buffers, decodes the data, and then transmits it to the CPU on the BPD.

4.6.4 INTELLIGENT COMMUNICATIONS SUBSYSTEM (ICS1 &ICS2)

The ICS1 & ICS2 interface asynchronous serial devices to a Prime central processor and enables protocol and electrical interface configuration to be specified on a per-device basis.

4.7 VIRTUAL CONTROL PANEL (VCP)

The VCP (Figure 4-32) is a microprocessor based controller and provides interface between the CPU, a directly connected and remote system console, plus a serial printer.

NOTE

Although the VCP is capable of supporting a serial printer, it is not recommended. Connecting a serial printer via the VCP significantly degrades system performance. If at all possible, the serial printer should be connected through an AMLC line.

The VCP emulates the SOC board functions of I/O Bus parity checking and interface with the system console and the serial printer. In addition, the VCP provides interface so the system can be accessed remotely via modem. The VCP also provides Control Panel functions:

- Power failure sequencing
- Automatic BOOT timing
- Auto Program Load (BOOT)

The VCP is a PCB like any other controller and plugs into the backplane just above the power supply (usually slot 2). If at all possible, there should be one empty slot between the power supply and the VCP, to allow for the heat dissipation from the power supply. Connector F on the back of the VCP board connects the VCP to the status panel. A molex connector connects the VCP to the PDU.

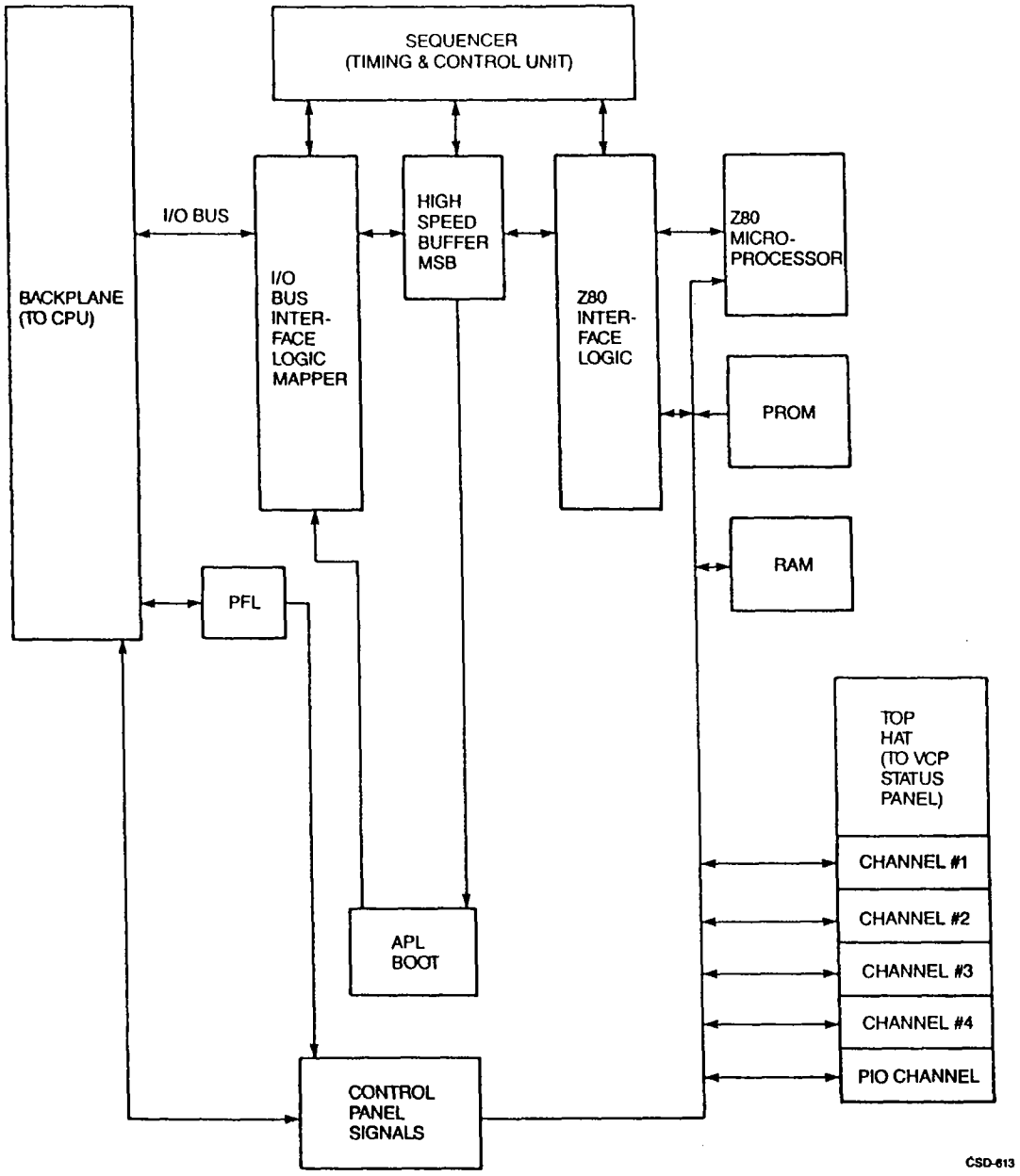


FIGURE 4-32: VCP BLOCK DIAGRAM

The following VCP functions are discussed in the next subsections:

- VCP Interface
- VCP Implementation of PIO Commands
- Z80 Code Debugger Functions
- VCP Connector Signals

4.7.1 VCP INTERFACE

Communication between the VCP and the CPU occurs via the I/O Bus and PIO instructions. The VCP also has four communications channels located on Connector E. Lines two, three, and four provide asynchronous communication between the VCP and the system console and the serial printer(s). Line one has additional logic to interface with a modem.

One parallel I/O channel is located on Connector C. It may be programmed to access four Z80 memory locations, and to troubleshoot the Z80 microprocessor.

All signals on the VCP are controlled by the Z80 system. The Z80 system is made up of a Z80 microprocessor, memory, and interface with the I/O Bus. The VCP has 10K static memory (PROM) and 32K dynamic memory (RAM).

Interface with the I/O bus is necessary because the VCP's Z80 microprocessor operates much slower than the Prime CPU. There are four basic elements of the I/O interface.

1. The I/O Bus Interface Logic and I/O Device Mapper: take the signal from the I/O Bus. The logic consists of bus transceivers, parity check logic, parity generation logic, DMX controller, and interrupt request and reset logic.

   The Mapper is a 64 word by 10 bit lookup table that matches the Prime CPU BPA command to the HSB storage location for the device address (for PIO) or the interrupt. Mapper output is read to the HSB Address MUX, then the Sequencer determines which address source to use.

2. The High Speed Buffer (HSB): compensates for the speed difference between the Prime CPU and the Z80. The HSB is a 1K by 22 bit high speed register file with 16 device tables, which stores all data necessary for performing PIO and interrupts.

3. The Z80 Interface Logic: passes the data from the HSB to the Z80. The logic includes bus receivers, bus drivers, and interrupt request logic.

4. The Microprogrammed Sequencer: provides timing and control. The Sequencer arbitrates the CPU and Z80 accesses to the HSB. The CPU requests have priority over Z80, since the CPU requests are faster. A Z80 request is interrupted, its address is stored in a stack, the CPU request is completed during the next microstep, then the Z80 request is resumed. The Sequencer has a 80 nanosecond cycle, which may be lengthened by conditions set in the WAIT field of the Sequencer's microcode word. Each of the 11 fields in the 20 bit microcode word controls a portion of the HSB access process.

All I/O signals (except Clock Timer) between the Z80 microprocessor and other devices are handled through mapping. Sixteen High Speed Buffer (HSB) locations are reserved for communication between the I/O Bus and the Z80. These locations provide access to:

- HSB address and data buses
- DMX Pointer
- LPCC Register (program counter)
- The Clock Control register

The Z80 and the Interface Logic access these HSB locations. Reading or writing these registers, sets and clears interrupt requests.

It is important to realize that the HSB can be addressed four ways:

- The Z80 can access the HSB directly, by providing the HSB location to be read or written.
- During DMX transfers, the HSB is accessed by a counter which keeps track of the address/data word pairs.
- The Mapper accesses the HSB via the device address that matches the BPA received on the I/O Bus.
- The Interrupt Mapper addresses the HSB through the HSB location for the type of interrupt being processed.

4.7.2 VCP IMPLEMENTATION OF PIO COMMANDS

The process the VCP uses to implement PIO commands is as follows:

1. During an INA instruction, the Mapper receives the signal from the I/O bus, decodes it to determine the addressed device, then maps it to the appropriate HSB location. If the device is ready (HSB ready bit set), the data in HSB is passed to the Prime CPU on the BPD. The Sequencer then clears the HSB ready bit.

2. During an OTA instruction, the Mapper again decodes the BPA. This time a Z80 interrupt occurs. No further transactions are processed (except for device '20 Control Panel) until the Z80 services the OTA request.

3. During an SKS instruction, the function code feeds the bit test logic which selects the appropriate bit. The bit is then fed to the ready logic. All skip conditions are stored in one HSB location. Some skips are handled in hardware (random logic).

4. OTA conditions are stored in one bit of a HSB location, just like SKS. Since OCPs always consider the device ready, special logic is used. Each time an OCP is pending service, a counter is incremented. Each time the counter is incremented from 0 to 1, a Z80 interrupt is generated. Each time an OCP is serviced by the Z80, the counter is decremented.

4.7.3 Z80 CODE DEBUGGER

The VCP is controlled by the Z80 microprocessor. The Z80 has its own registers, ALU, control unit and buses and its own assembly language, Z80 Code Debugger.

4.7.4 VCP CONNECTOR SIGNALS

The VCP PCB has two backpanel connectors CA and CB. It also has four interface connectors (CC, CD, CE, CF) located on the front of the PCB. Tables 4-9 through 4-12 list the connector pins and signal names. Figure 4-33 illustrates the connector locations.

TABLE 4-9: CONNECTOR CA SIGNAL LIST

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
VCC1	CA-1		CA-51
VCC1	CA-2		CA-52
SHIELD (GND)	CA-3		CA-53
BPCDCPN+	CA-4	PS60CY+	CA-54
BPCDEN+	CA-5		CA-55
GND	CA-6		CA-56
BPCDPNO-	CA-7		CA-57
BPCDPNA-	CA-8		CA-58
BPCDPNB-	CA-9		CA-59
BPCDPNC-	CA-10	GND	CA-60
BPCDND-	CA-11		CA-61
BPCDNE-	CA-12		CA-62
BPCDNF-	CA-13		CA-63
BPCDNG-	CA-14		CA-64
BPCDNH-	CA-15		CA-65
BPCIEN+	CA-16		CA-66
BPCIPNO-	CA-17		CA-67
BPCIPNA-	CA-18		CA-68
BPCIPNB-	CA-19		CA-69
BPCIPNC-	CA-20		CA-70
BPCIPND-	CA-21		CA-71
SHIELD (GND)	CA-22		CA-72
BPCIPN+	CA-23		CA-73
GND	CA-24		CA-74
BPCCH1+	CA-25		CA-75
SHIELD (GND)	CA-26		CA-76
	CA-27		CA-77
	CA-28		CA-78
	CA-29		CA-79
BPCEOR+	CA-30		CA-80
	CA-31		CA-81
	CA-32		CA-82
	CA-33		CA-83
	CA-34		CA-84
	CA-35		CA-85
	CA-36		CA-86
	CA-37		CA-87
BPCIOVI-	CA-38		CA-88
	CA-39		CA-89
	CA-40	BPCFCLK+	CA-90
BPCBSTRB+	CA-41		CA-91
GND	CA-42	BPCIRO-	CA-92
	CA-43	BPCDRO-	CA-93
	CA-44		CA-94
	CA-45		CA-95

TABLE 4-9: CONNECTOR CA SIGNAL LIST (Cont.)

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
	CA-46		CA-96
	CA-47		CA-97
SHIELD (GND)	CA-48	GND	CA-98
VCC1	CA-49	VCC2	CA-99
VCC1	CA-50	VCC2	CA-100

TABLE 4-10: CONNECTOR CB SIGNAL LIST

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
VCC1	CB-1	BPA12+	CB-51
VCC1	CB-2	BPA13+	CB-52
GND	CB-3	BPA14+	CB-53
ISO (SPARE)	CB-4	BPA15+	CB-54
VSS	CB-5	BPA16+	CB-55
	CB-6	BPALP+	CB-56
	CB-7	GND	CB-57
	CB-8	BPARP+	CB-58
	CB-9	BPCPIO+	CB-59
	CB-10	BPAPER-	CB-60
	CB-11	BPC60CY+	CB-61
	CB-12	BPCREDY-	CB-62
	CB-13	BPDLP+	CB-63
	CB-14		CB-64
	CB-15	BPD01+	CB-65
	CB-16	BPDRP+	CB-66
	CB-17	BPD02+	CB-67
	CB-18	BPD03+	CB-68
	CB-19	BPD04+	CB-69
	CB-20	BPD05+	CB-70
	CB-21	BPD06+	CB-71
	CB-22	BPD07+	CB-72
	CB-23	BPD08+	CB-73
	CB-24	BPD09+	CB-74
HPWRFL-	CB-25	BPD10+	CB-75
GND	CB-26	BPD11+	CB-76
HPFRLY+	CB-27	V12-	CB-77
	CB-28	V12-	CB-78
BPA01+	CB-29	BPD12+	CB-79
GND	CB-30	GND	CB-80
BPA02+	CB-31	BPD13+	CB-81
BPA03+	CB-32	BPD14+	CB-82
BPA04+	CB-33	BPD15+	CB-83
BPA05+	CB-34	BPD16+	CB-84
BPA06+	CB-35	BPCMOD0+	CB-85
BPA07+	CB-36	BPCMOD1+	CB-86
BPA08+	CB-37	BPCMOD2+	CB-87
BPA09+	CB-38	BPCMOD3+	CB-88
BPA010+	CB-39	BPCINMD+	CB-89
BPA011+	CB-40	BPCSCLK+	CB-90
HSYSCLR-	CB-41	V12+	CB-91

TABLE 4-10: CONNECTOR CB SIGNAL LIST (Cont.)

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
GND	CB-42	V12+	CB-92
PSRLY+	CB-43	HRUN-	CB-93
	CB-44	HRUN-	CB-94
BPDPEL-	CB-45	BPCSTRB+	CB-95
GND	CB-46	GND	CB-96
BPDPER-	CB-47	VSS	CB-97
BPAPEL-	CB-48	VSS	CB-98
BPA99+	CB-49	VBB	CB-99
BPA00+	CB-50	VBB	CB-100

TABLE 4-11: CONNECTORS CC & CD SIGNAL LISTS

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
WDTEXS-	CC-1	D01+	CD-1
RETOUT-	CC-2	D02+	CD-2
EXPF-	CC-3	D03+	CD-3
RETIN-	CC-4	D04+	CD-4
	CC-5	D05+	CD-5
	CC-6	D06+	CD-6
DZ01+	CC-7	D07+	CD-7
DZ02+	CC-8	D08+	CD-8
DZ03+	CC-9		CD-9
DZ04+	CC-10	A01+	CD-10
DZ05+	CC-11	A02+	CD-11
DZ06+	CC-12	A03+	CD-12
ZP1001+	CC-13	A04+	CD-13
	CC-14	A05+	CD-14
ZP1002+	CC-15	A06+	CD-15
DZ08+	CC-16	A07+	CD-16
ZP1003+	CC-17	A08+	CD-17
ARDY+	CC-18	A09+	CD-18
ZP1004+	CC-19	A10+	CD-19
BRDY+	CC-20	A11+	CD-20
ZP1005+	CC-21	A12+	CD-21
ASTB-	CC-22	A13+	CD-22
ZP1006+	CC-23	A14+	CD-23
BSTB-	CC-24	A15+	CD-24
ZP1007+	CC-25	A16+	CD-25
VCC	CC-26		CD-26
ZP1008+	CC-27	MI-	CD-27
VCC	CC-28	MREQ-	CD-28
ZP1009+	CC-29	IORQ-	CD-29
DZ09+	CC-30	RD-	CD-30
ZP1010+	CC-31	WR-	CD-31
DZ10+	CC-32	RFSH-	CD-32
ZP1011+	CC-33	WAIT-	CD-33
DZ11+	CC-34	INT-	CD-34
ZP1012+	CC-35	NHI-	CD-35
DZ12+	CC-36	RSET-	CD-36
ZP1013+	CC-37	BSRQ-	CD-37

TABLE 4-11: CONNECTORS CC & CD SIGNAL LISTS (Cont.)

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
DZ13+	CC-38	BUSAK-	CD-38
ZP1014+	CC-39	HALT-	CD-39
DZ14+	CC-40		CD-40
ZP1015+	CC-41		CD-41
DZ15+	CC-42		CD-42
ZP1016+	CC-43		CD-43
DZ16+	CC-44	CLK+	CD-44

TABLE 4-12: CONNECTORS CE & CF SIGNAL LISTS

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
CTXC1-	CE-1		CF-1
GND23R-	CE-2		CF-2
CTXDL1-	CE-3		CF-3
GND23R-	CE-4		CF-4
CRXC1-	CE-5		CF-5
GND23R-	CE-6		CF-6
CRXDL1-	CE-7		CF-7
GND23R-	CE-8		CF-8
CRTSL1-	CE-9		CF-9
GND	CE-10		CF-10
CDTRL1+	CE-11		CF-11
GND	CE-12		CF-12
CDSCL1+	CE-13		CF-13
GND	CE-14		CF-14
CDCDL1+	CE-15		CF-15
GND	CE-16		CF-16
CCTSL1+	CE-17		CF-17
GND	CE-18		CF-18
CDSRL1+	CE-19		CF-19
GND	CE-20		CF-20
CTXC2-	CE-21		CF-21
GND	CE-22		CF-22
CTXDL2-	CE-23		CF-23
GND	CE-24		CF-24
CRXC2-	CE-25		CF-25
GND	CE-26		CF-26
CRXDL2-	CE-27		CF-27
GND	CE-28		CF-28
CTXC3-	CE-29		CF-29
GND	CE-30		CF-30
CTXDL3-	CE-31		CF-31
GND	CE-32		CF-32
CRXC3-	CE-33	BSPMC-	CF-33
GND	CE-34	BSPRE-	CF-34
CRXDL3-	CE-35	BSPGND2-	CF-35
GND	CE-36	BSPRP-	CF-36
CTXC4-	CE-37	BSPGND-	CF-37
GND	CE-38	BSPKL+	CF-38
CTXDL4-	CE-39	BSPGND1-	CF-39

TABLE 4-12: CONNECTORS CE & CF SIGNAL LISTS (Cont.)

NAME	CONNECTOR PIN	NAME	CONNECTOR PIN
GND	CE-40	BSPRNL-	CF-40
CRXC4-	CE-41	BSPVCC1+	CF-41
GND	CE-42	BSPRL-	CF-42
CRXDL4-	CE-43	BSPVCC2+	CF-43
GND	CE-44	BSPRAL-	CF-44

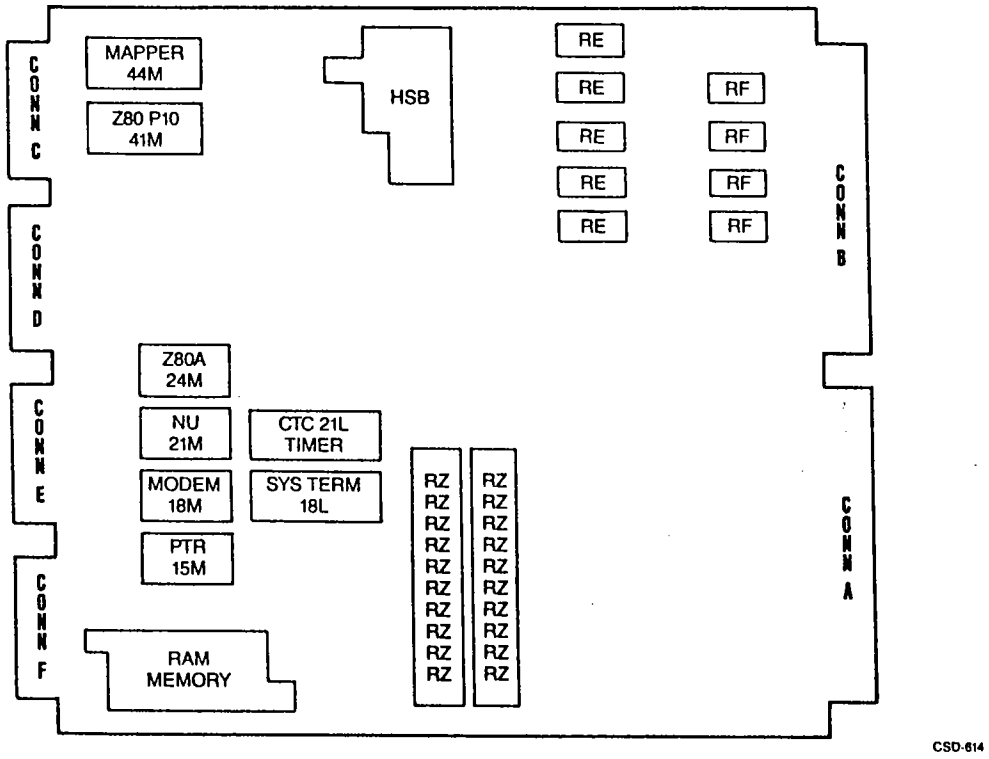


FIGURE 4-33: VCP PCB CONNECTORS

4.8 POWER SUPPLIES

Discussed in the following subsections are:

- 1045 and 1051 Power Supplies
- DC Voltage Buses
- Power Supply Protection
- AC/DC Power Failure Sequence and Controls

- Uninterruptable Power Supply (UPS)

4.8.1 1045 AND 1051 POWER SUPPLIES

The 50 Series processors use models 1045 and 1051 power supplies. Block diagrams of the supplies appear in Figures 4-34 and 4-35. These supplies, in slots 0, 00, 000, and 0000 of the backplane, provide dc voltages through the backplane PCB connectors to the logic boards. The voltage buses of each backplane are isolated from each other, so that each supply provides voltage to only one section of the chassis. The power failure detection signal (HPWRFL) is wired from the bottom backplane up to the top backplane. The system senses power failure from the bottom power supply.

CAUTION

Insert the power supply into slots 0, 00, 000, or 0000 ONLY. Otherwise, PCBs plugged into the backplane will be severely damaged. Keep supplies isolated from each other to avoid system damage.

4.8.2 DC VOLTAGE BUSES

DC voltage serves three main purposes:

- PCB General Logic
- PCB RS232-C Communications Interface
- Memory

VCC1 and VCC2 (+5 Vdc) - supply general logic voltage to all PCBs, including the VCP. These buses are tied together in the power supply. The +5 Vdc is produced by a 20KC off-line switcher circuit. A minimum load of 12 amps is required to maintain the +5 Vdc.

V12- and V12+ (+/-12 Vdc) - supply voltage primarily to the EIA drivers on communications controllers and any other PCB with communications interfaces (VCP, for example). Storage module controllers (4004,5) use -12 Vdc to supply the special device interface $\pm$5 Vdc requirements.

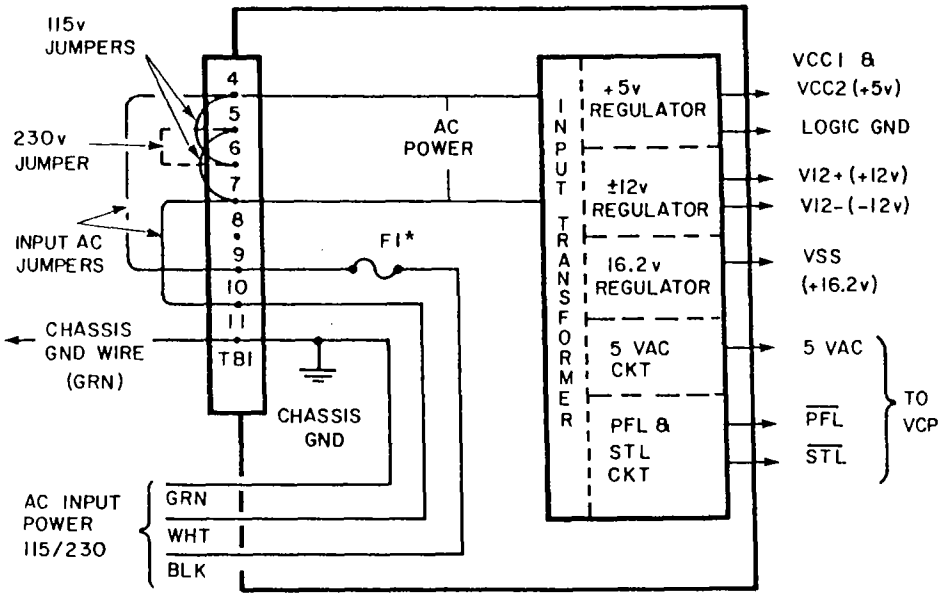
VSS (+16.2 Vdc) - supply voltage primarily to the MOS memory RAM chips and chip drivers.

The +16.2 Vdc, +12 Vdc, and -12 Vdc supplies are all linear series pass type circuits, and will maintain regulation with little or no load.

4.8.3 POWER SUPPLY PROTECTION

The power supply is protected against the following conditions:

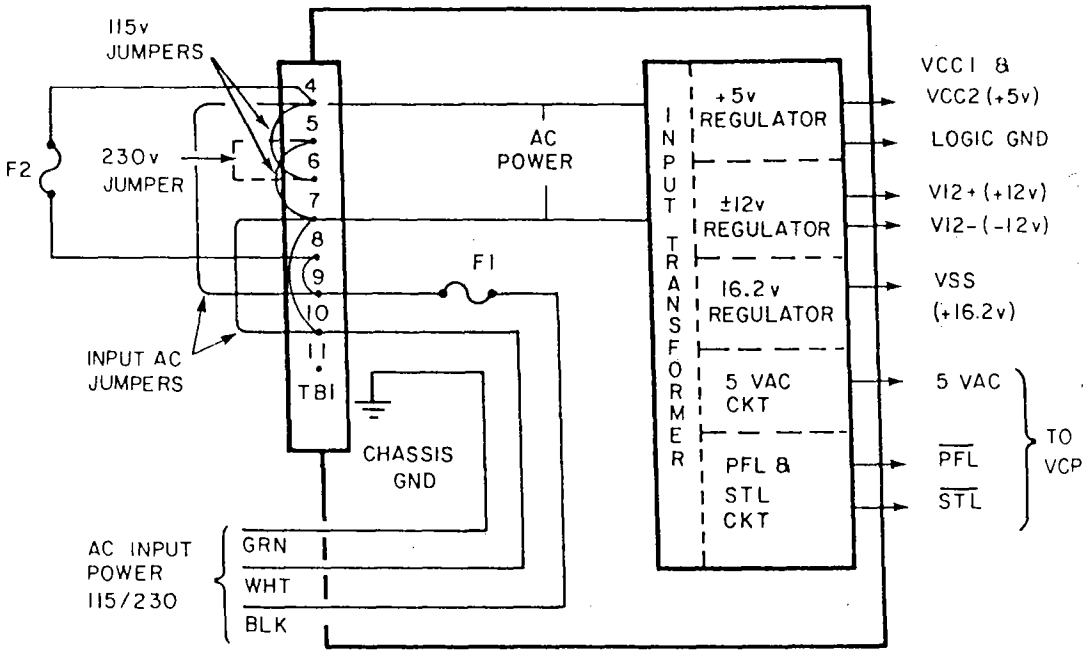
- Current overload - If the maximum current load is exceeded on any of the dc voltages (crowbars), the voltage cuts off, triggering a power failure condition.



*F1 = 15ASB - FOR 115 VAC, 60 HZ INPUT (DOMESTIC)
= 10ASB - FOR 230 VAC, 50 HZ INPUT (INTERNATIONAL)

CSD-615

FIGURE 4-34: 1045 POWER SUPPLY BLOCK DIAGRAM



FOR 115 VAC, 60 HZ INPUT (DOMESTIC): F1= 15A SB
F2= 3A SB

FOR 230 VAC, 50 HZ INPUT (INTERNATIONAL): F1= 10A SB
F2= 1.6A SB

CSD-120

FIGURE 4-35: 1051 POWER SUPPLY BLOCK DIAGRAM

- Overvoltage - If the maximum dc voltage is exceeded on any of the dc voltages, both voltage and the entire supply shut off (crowbar).

Refer to Chapter 6 for power supply overload and overvoltage specifications.

4.8.4 AC/DC POWER FAILURE SEQUENCE AND CONTROLS

The power supply generates PFL and STL signals (PSRLY), which are developed on the VCP as HSYSCLR (power on/system clear) and HPWRFL (power fail). These signals pass to the rest of the system via the backplane.

1. PFL is generated when a loss of ac power is detected by the power supply (prior to the actual loss of dc power). This gives the system 1m-sec to generate HPWRFL and perform all software power fail routines (close files, stop I/O transfers, etc.).

2. STL is generated when a loss of dc power is detected by the power supply. The STL signal halts the CPU.

3. PS60CY, a 30 mA, truncated 5 Vac signal, is generated by the power supply to the VCP as soon as input power is detected. The VCP in turn, develops signal BPC60CY+ and HSYSCLR, which are used by the real time clock.

4.8.5 UNINTERRUPTIBLE POWER SUPPLY (UPS)

Prime does not presently install or support the UPS. However, Prime recommends the UPS as an alternative to poor electrical conditions. The customer must arrange for purchase, installation and maintenance support of a UPS.

The uninterruptible power supply (UPS) maintains ac power if a system's main power source is shut off. The power supply is normally used when the customer's power source is subject to blackouts, brownouts or power fluctuations. The UPS transforms a relatively unstable power source into a well regulated and uninterrupted source, capable of supplying a computer with the high quality power it requires. Essentially, the UPS takes ac power from the power line, converts it to dc and then reconverts it back to ac.

The UPS consists of three major components:

- Rectifier
- Batteries
- Inverter

The rectifier converts the power line voltage to dc voltage so that the batteries can be charged continually. The inverter converts the dc voltage back into the proper ac line voltage for the computer system. In general, the rectifier regulates all power to the system and isolates it from power fluctuation. A UPS supplies uninterrupted regulated ac power, based on battery reservoir energy, to an entire system or parts of a system.

UPS operation has been integrated into Prime hardware and software. For example, consider a UPS which supports the central processor and memories. When the ac power goes down, the UPS switches to its batteries to maintain power to the system. During this transition, CPU and memory operation is not disturbed. The UPS then notifies PRIMOS that power has been lost. PRIMOS shuts down the system in the normal manner (as if HPWRFL was detected) and waits for power to return. The CPU and memories remain powered up during the outage.

When ac power returns, the UPS notifies PRIMOS that ac power has been restored. PRIMOS generates a master clear, to initialize the CPU and controllers. A warm start is performed and normal processing continues. Some processes which were using peripherals will receive errors. If the outage lasts so long that the UPS batteries are exhausted, the operator must cold start the system when power is restored.

The support capability of a single UPS is dependent on the size of the power supply and ranges from a minimum of one CPU with memory to a complete system with associated peripherals. Depending on the number and capacities of the batteries purchased, ac power backup can last from as little as twenty minutes to as long as several hours.

4.9 POWER DISTRIBUTION UNIT (PDU) NON-FCC CABINET

The PDU is a central control for all power supplies within the peripheral or mainframe cabinet. All power supplies in the cabinet plug into either the PDU's switched or unswitched receptacles. Once the PDU circuit breaker is set, all power supplies connected to the PDU's switched receptacles can be turned on by the VCP Status Panel power button. Any power supply connected to the PDU's unswitched receptacle can be turned on from the PDU circuit breaker.

There are three types of PDUs. Each one uses the same mounting plate and is mounted in the bottom rear of the cabinet on the base assembly.

- Domestic Mainframe Cabinet PDU: The Domestic mainframe cabinet PDU (Figure 4-36) has a 4-wire ac inlet for 30 amp, 120/208 volt service (see NOTE). The 60 amp capability at 120 volts allows up to 48 amps of input power when derated by a 20% derating factor. Three 120 amp, +5V power supplies and the cabinet blower would use approximately 35 amps of this input power.

  NOTE

  The 208V service consists of two 120V single phase lines with a common return and a safety ground.

- International Mainframe Cabinet PDU: The International mainframe cabinet PDU (Figure 4-37) uses a 3-wire inlet at 30 amps, 240 VAC. The cabinet includes a 240 to 115 step-down transformer for use by the blower.

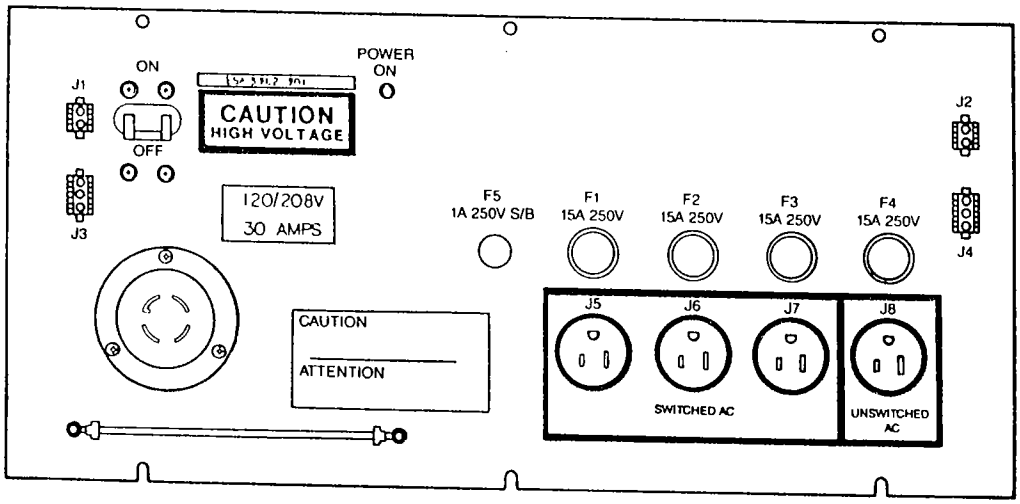


FIGURE 4-36: DOMESTIC MAINFRAME CABINET PDU

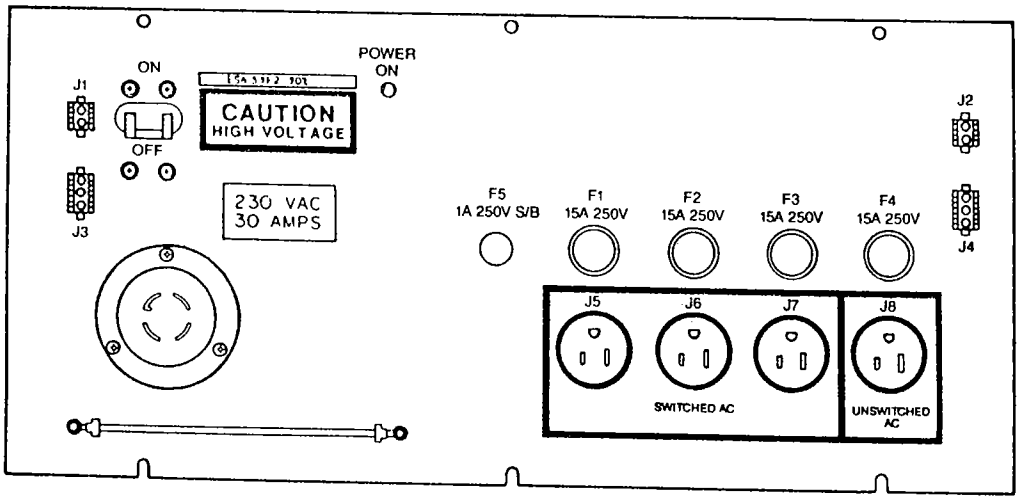


FIGURE 4-37: INTERNATIONAL MAINFRAME CABINET PDU

- Domestic and International Peripheral Cabinet PDU: The Domestic and International peripheral cabinet PDUs (Figures 4-38 and 4-39) use a 3-wire service at 30 amps, 120 or 240 VAC. The 240/115 VAC step-down transformer is included in the International peripheral cabinet.

NOTE

The Domestic peripheral cabinet must be operated on 120 Vac, since it does not contain the step-down transformer.

Each PDU has its own ac circuit breaker, which is used by the blower. Therefore, when system power is turned off at the mainframe's Status Panel, the blowers continue to operate until the main ac circuit breaker is turned off.

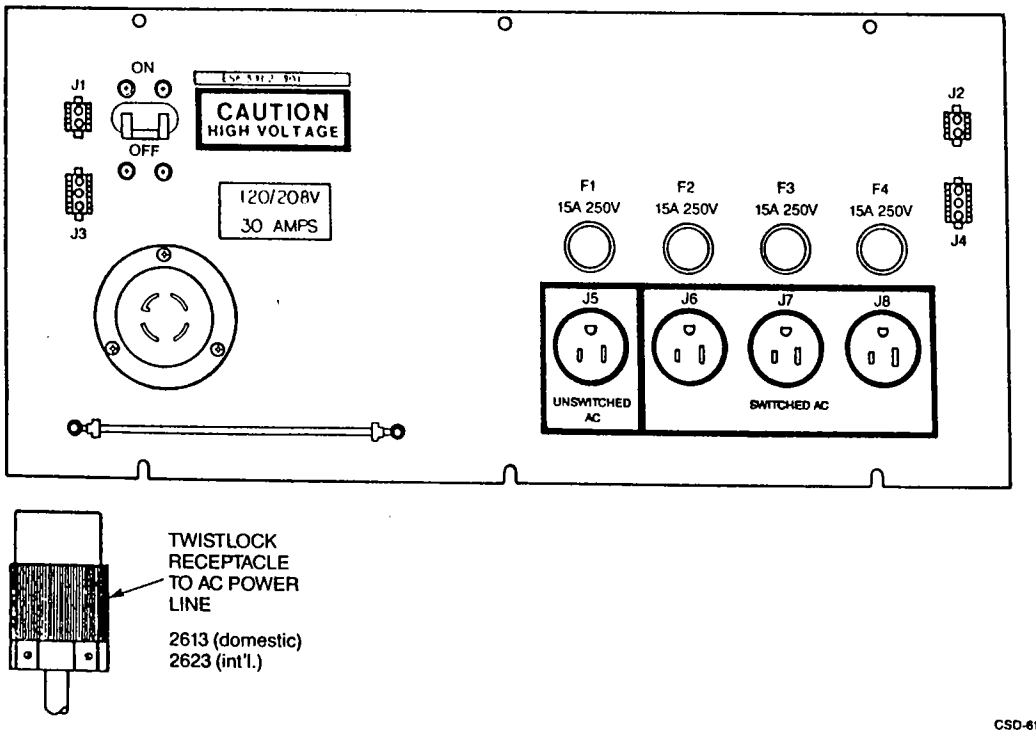


FIGURE 4-38: DOMESTIC PERIPHERAL CABINET PDU

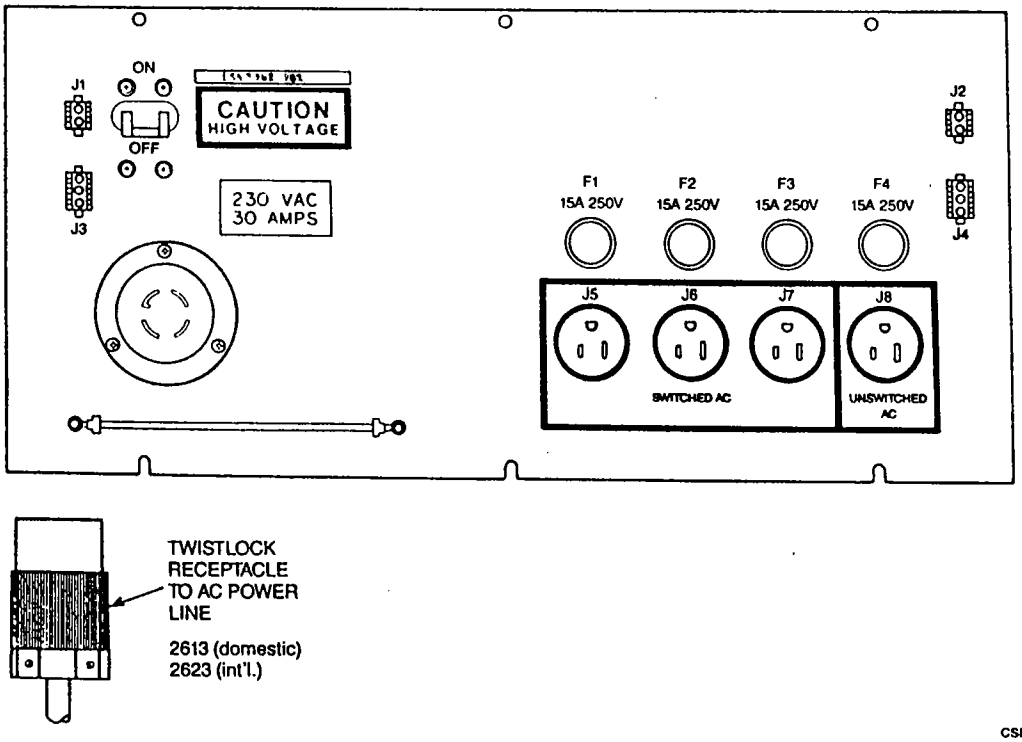


FIGURE 4-39: INTERNATIONAL PERIPHERAL CABINET PDU

The mainframe PDU has a +12 Vdc power supply which is switched through the VCP Status Panel power button. Depressing the power button activates the +12 Vdc to relays, which supply ac to the switched ac duplexes. Mate-n-lock connectors J3 and J4 connect this +12 Vdc to other (peripheral) cabinets in the system, so that all switched ac outlets can be enabled from the Status Panel power switch.

All PDUs have five duplex outlets. The mainframe has three switched (four on the 750) duplexes, each powered from a separate solid state relay, which supply 15 amp +5V of power for one 120 amp power supply. The two unswitched ac (none on the 750) duplexes are powered directly from the main ac circuit breaker. The peripheral cabinets also have five duplexes, however, only one solid state relay powers the three switched ac outlets. The two unswitched outlets may be connected to other peripheral devices.

4.10 POWER DISTRIBUTION UNIT (PDU) FCC

On a 50 Series system mounted in a FCC cabinet the four-channel PDU performs the following functions:

- Sequentially distributes ac power to the CPU, memory and I/O devices
- Shuts down ac power in the event of overtemperature, air flow interrupt, or loss of a phase of ac power
- Provides remote turn on or off of the ac power from or to another PDU

Figure 4-40 is a logic schematic of the PDU.

The purpose of the PDU is to distribute two phases (one International) of ac power in a prescribed sequence to the various units within the cabinet. The PDU contains a control/distribution panel, line filter, circuit breakers, power relays and a board containing the control/sequence circuitry.

The PDU interfaces to the Power On switch on the front panel and the temperature sensors via the VCP. A fault indicator shows loss of a phase within the PDU or an error signal from the previous or main cabinet. A remote/local switch is provided to control the PDU without using the front panel (remote= front panel active).

When the main circuit breakers are switched on, the control board/sequencer is provided with power. The Power On switch enables the control board to power on the various outlets in sequence in order to balance the load. When taking measurements always have in mind the high voltage of a two phase system. Always take measurements in reference to the neutral line. Note that no three phase device is present in the system. The phases are split up to balance the load.

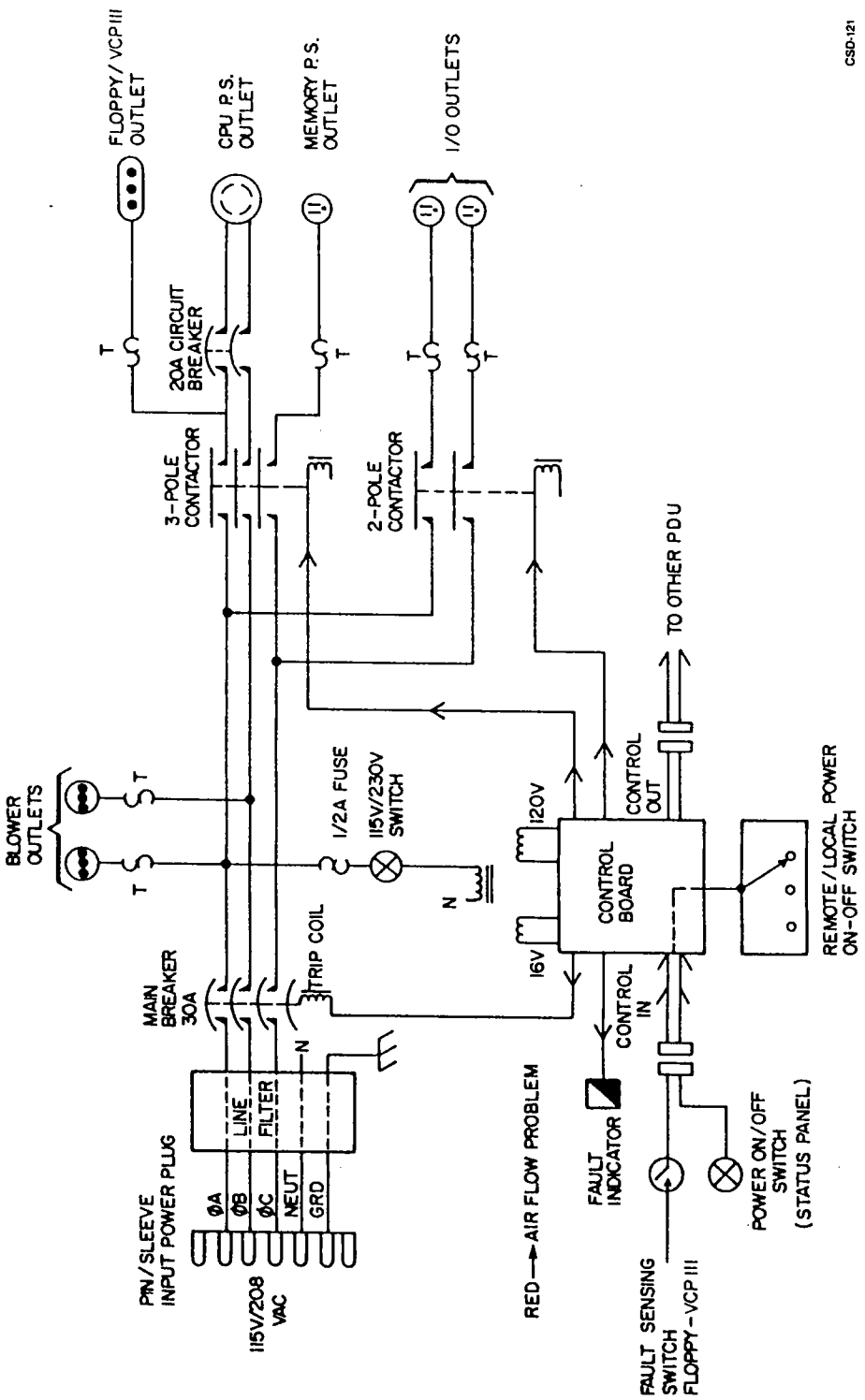


FIGURE 4-40: PDU SCHEMATIC

CHAPTER 5
PREVENTIVE MAINTENANCE

5.1 INTRODUCTION

This chapter contains Preventive Maintenance instructions and procedures. Preventive Maintenance consists of reviewing the product's history and performing the appropriate maintenance. The product maintenance philosophy and product history are presented below.

5.2 MAINTENANCE PHILOSOPHY

The CSR is responsible for performing the 50 Series system Preventive Maintenance procedures outlined in this chapter.

5.3 PRODUCT HISTORY

A product's history refers to information concerning system configuration and events as well as trends in system performance. This information is available via the system logbook and the event logger buffer. These two sources are discussed in the following subsections.

5.3.1 SYSTEM LOGBOOK

The system logbook is used to report information on the system status and operation. The logbook should contain the following information:

- Hardware
  - System configuration, including model and serial numbers
  - Changes to the original configuration (additions, deletions, alterations, or substitutions)
  - Changes to the operating status (failures)
- Environmental
  - Abnormal temperatures
  - Unusual conditions (smoke, dust, or chemical spillage)
  - Unauthorized access to the computer room or to the system by remote login
  - Loss or damage to the equipment
  - Any actions and duration to correct the above problems
- Software
  - PRIMOS.COMI (C_PRMO) system startup file
  - CONFIG data file
  - CMNDC0 command directory contents and LIB library directory contents
  - RING0.MAP and RING3.MAP memory loadmaps
  - All shared memory segment numbers
  - Any addition, replacement, or alteration of the above

- Operations
  - System startups and shutdowns
  - Use of the FIX_DISK utility with the name of the physical device number, partition,and the results of the operation
  - Any disk formatting
  - Backups, including partion name, copy date, type of copy, and media type
  - Restoration of files or directories of the system
  - Archiving of directories
- Halts
  - System status messages
  - Startup procedure after halt
  - Functioning of system after restart

The system administrator decides what information is contained in the logbook. The system operators are responsible for entering the information. The entered information should be numbered, dated, and signed by the operator making the entry.

5.3.2 EVENT LOGGERS

Event loggers record information about significant system or network events in an internal buffer. PRIMOS has two event loggers:

- System
- Network

These loggers are detailed in the following sections.

5.3.2.1 System Event Logger

The system event logger records system events, such as cold and warm starts, machine checks, and disk Read/Write errors. Two methods enable/disables the logger:

- The CONFIG file directive, LOGREC (at system startup)
- The command, EVENT_LOG -[OFF] (when the system is running)
  -[ON]

When event logging is enabled, a file is opened in the UFD LOGREC*. The file name is LOG.mm/dd/yy. The mm/dd/yy represents the month, day, and year when the logging was enabled. The file contains a binary-encoded log of system events. The SET_QUOTA command allocates the logging file's maximum disk space.

Each time a PM is performed, the system log file is examined. The PRINT_SYSLOG utility analyzes the system log file and produces a formatted output file that chronicles the system events represented in the file. Invoke the PRINT_SYSLOG utility by the command line:

```
PRINT_SYSLOG [output-filename] [options]
             [     TTY       ]
```

The output-filename names the system log output file. TTY displays the output file to the user's terminal. If either output-filename or TTY is not specified, the system output file is placed into the filename, LOGLST. A sample output file is illustrated in Figure 5-1.

```
***** <0>LOGREC*>LOG.09/08/84, 11:55:52 MON 10 SEP 1984 *****

08:36:00 MON 10 SEP 1984

PRIORITY ACL SET ON DISK MASTER BY USER SYSTEM (#1 )

08:37:00 MON 10 SEP 1984

PRIORITY ACL SET ON DISK INSTRT BY USER SYSTEM (#1 )

08:38:00 MON 10 SEP 1984

PRIORITY ACL SET ON DISK DATA BY USER SYSTEM (#1 )

08:39:00 MON 10 SEP 1984

PRIORITY ACL SET ON DISK PUPILS BY USER SYSTEM (#1 )

PRIORITY ACL SET ON DISK SFTWRE BY USER SYSTEM (#1 )

PRIORITY ACL SET ON DISK SFT-II BY USER SYSTEM (#1 )


TYPE    NUMBER
TIMDAT  4
PACL    6

***** END OF FILE -- 6 ENTRIES, 6 PROCESSED *****
```

FIGURE 5-1: PRINT_SYSLOG SAMPLE FILE

In the UFD LOGREC*, multiple system log input files may exist. The option, [-INPUT treename], is used with the PRINT_SYSLOG utility to select a specific system log input file. If [-INPUT treename] is not defined, the most recent log file is selected as an output file. If no system log input files exist, the PRINT_SYSLOG utility prompts for an input filename. Table 5-1 lists and defines all options available for PRINT_SYSLOG.

TABLE 5-1: PRINT_SYSLOG AND PRINT_NETLOG OPTIONS

OPTION	DESCRIPTION*
-HELP	Prints a list of PRINT_SYSLOG options. PRINT_SYSLOG must be retyped after the options are printed.
-INPUT treename	Specifies the input log file's treename to be processed. If this option is not presented on the command line, the most

TABLE 5-1: PRINT_SYSLOG AND PRINT_NETLOG OPTIONS (Cont.)

OPTION	DESCRIPTION
	recent input log file is processed.
-FROM [mmddyy] [hhmm] [TODAY]	Input files from the specified date to the most recent date are processed. TODAY processes the input log file with today's date. [hhmm] specifies the time of the date to be processed.
-TYPE type type...	Processes entries of the indicated types. System Event types are listed in Table 5-2. Network events are listed in Table 5-3.
-SPOOL	Spools the output file after processing is complete.
-DELETE	Deletes the output file after processing is finished. This option is used only with the -SPOOL option.
-PURGE	Empties the specified event log input file when processing is complete. If the event file is the most recent input file and it is not disabled, the empty file continues to record system or network events.
-CENSUS	Totals the event types in the input file and writes the totals to an output file or user's terminal. Zero totals are not displayed.
-CONTINUE	Allows processing to continue after an illegal entry has halted PRINT_SYSLOG. The next valid entry is located to continue the process.
-DEBUG	Causes PRINT_SYSLOG to read entries from the terminal and test formatting of entry types. Each entry is entered as a series of tokens. Octal tokens are converted to binary while all others are read as ASCII strings. This mode is exited when a Q, q, or null line is entered.
-REMARK text	Enters the text directly into the input file. The text can be 80 characters maximum and cannot be surrounded by apostrophes.
-DUMP	Processes the input file and dumps each processed entry in octal.

* For PRINT_NETLOG options, replace all PRINT_SYSLOG references with PRINT_NETLOG.

TABLE 5-2: SYSTEM EVENT TYPES

TYPE	DESCRIPTION
COLD	Cold start
WARM	Warm start
TIMDAT	Time/data entry*
Checks	Machine checks (including memory parity)
POWERF	Power fail checks
DISK	Disk errors
DISKNAM	ADDISK entry
OVERFL	LOGBUF overflow entry
SHUTDN	Operator shutdown
CHK300	P300 machine check
PAR300	P300 memory parity checks
MOD300	P300 missing memory module checks
TYPE10	Entry for type 10
TYPE11	Entry for type 11
TYPE12	Entry for type 12
TYPE13	Entry for type 13
TYPE14	Entry for type 14
TYPE15	Entry for type 15
QUIET	Machine check mode now quiet
SETIME	Operator issued a SETIME command
REMARK	Operator remark
PACL	Priority ACL set
SENSOR	Sensor check

*The time/date stamps associated with selected entries are not processed unless TIMDAT is explicitly selected. If TIMDAT is specified in conjunction with one or more types, only the specified types' time/date is processed. If TIMDAT is specified alone, all time/date stamps are processed. If -TYPE option is not specified, all entries are processed.

5.3.2.2 Network Event Logger

The network event logger records major network events, such as operator shutdowns, event buffer overflow, and out-of-sequence packets. Two methods enable/disable the logger:

- The CONFIG file directive, NETREC (at system startup)
- The command, EVENT_LOG -NET -[OFF] (when the system is [ON] running)

When network logging is enabled, a file is opened in the UFD PRIMENET*. The filename is NET_LOG.mm/dd/yy. The mm/dd/yy represents

the month, day, and year that the logger was enabled. The SET_QUOTA command allocates the logging file's maximum disk space.

Each time a PM is performed, the network log file is examined. The PRINT_NETLOG utility analyzes the network input log file and produces a formatted output file that chronicles the network events. PRINT_NETLOG is invoked by the command line:

```
PRINT_NETLOG [output-filename] [options]
             [     TTY       ]
```

The output-filename names the output file. If TTY is specified, the output file is displayed on the user's terminal. If the output-filename or TTY is not specified, the output is written to the file, NETLST. An output file sample is illustrated in Figure 5-2

```
** <0>PRIMENET*>NET_LOG.09/08/84, 11:56:20 MON 10 SEP 1984 **

14:42:00 SAT 08 SEP 1984

COLD START

TOKEN INSERTED INTO THE RING NETWORK

TOKEN INSERTED INTO THE RING NETWORK

15:31:12 SAT 08 SEP 1984

NPX>R$CALL>R$CONN UNKNOWN CIRCUIT STATUS - NODE: 001005

      VC STATE(1): 000004
      VC STATE(2): 000372

17:30:44 SAT 08 SEP 1984

CIRCUIT RESET - LOCALLY ORIGINATED - RING NODE: 1

      CIRCUIT STATE: 5

RING NODE: 1 NOT ACCEPTED XMITS. XMIT STAT IS: 020300

RING NODE: 1 NOT ACCEPTING XMITS. XMIT STAT IS: 100300

                TYPE        NUMBER

                COLD        1
                TIMDAT      2
                RESET       1
                RING1       2
                RING2       1
                RING3       2
                NPXCON      2
```

FIGURE 5-2: PRINT_NETLOG SAMPLE FILE

In the UFD PRIMENET*, multiple network log output files may exist. The option [-INPUT treename] is used with the PRINT_NETLOG utility to select a specific network log input file. If this option is not defined, the most recent log file is selected as the output file. If no network log input files exist, the PRINT_NETLOG utility prompts for an input filename. Table 5-1 defines and lists all options available for PRINT_NETLOG.

TABLE 5-3: NETWORK EVENT TYPES

TYPE	DESCRIPTION
COLD	Cold Starts
WARM	Warm Starts
TIMDAT	Time/Date Entries (see Table 5-2)
RESET	Circuit Resets
BADSEQ	Packets out of sequence
OVERFL	NETBUF overflow entries
SHUTDN	Operator Shutdowns
LPE	Local procedure errors
RING1	Tokens inserted into the ring
RING2	Ring dims out of receive blocks
RING3	Ring nodes not accepting transmits
NETDMP	NETDMP calls
SMLC1	SMLC status errors
SMLC2	SMLC--no STX preceding ETX
SMLC3	No system blocks for SMLC protocol message
SMLC4	SMLC resets
HOSTDN	Level III protocol down
PWFAIL	Power fail checks
INCREQ	Incoming call request
OUCREQ	Outgoing call request
REMARK	Operator message
NPXTHR	NPX throttled on transmit/receive
NPXRCV	NPX unexpected receiver status
NPXCLR	NPX master circuit was cleared
NPXSEQ	NPX message out of sequence
NPXCON	NPX unknown circuit status
NPXRLS	NPX bad virtual circuit clearing
RNGRCV	PNC spurious receive interrupt
RNGHRD	PNC hardware failure
RNGRES	Resource failure

5.4 PM SCHEDULE

Figure 5-3 is a sample PM schedule for a system. When used in conjunction with a similar schedule for each device, the Branch Manager can tailor and maintain the PM schedule for each system according to configuration usage and environment. The schedule is based on monthly PMs and average usage of less than 60 hours a week power-on time. The schedule can be used to record PMs for one year; each column indicates one month.

Address 123 Main Street MA # 0678

Downtown, USA

PM TASKS		CIRCLE AVG. OR HIGH[1] USAGE		MONTHLY RECORD - ENTER DATE AND CHECK[2] TASKS PERFORMED												
	Ref[3]	Avg.	High	Date	Date	Date	Date	Date	Date	Date	Date	Date	Date	Date	Date	Est. Time
INSPECTION																
Check Blower Operation	5-1	1	1	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	.1 hrs
Check for System Malfunctions	5-1	1	1	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	.1 hrs
CLEANING																
Vacuum Cabinets	5-2	1	1	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	.2 hrs
Clean/Replace Filters[4]	5-2	1	1	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	.2 hrs
ADJUSTMENTS																
Check Pwr Sup Voltages	6-	6	3	OK			OK			OK			OK			.2 hrs
PERIPHERAL PM SCHEDULE[5]																
MHD Unit 0 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM						Due			Due			Due			Due	
MHD Unit 1 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM					Due			Due				Due			Due	
MAG TAPE Unit 0 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM				Due		Due		Due		Due		Due			Due	
MAG TAPE Unit 1 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM					Due		Due		Due			Due			Due	
LINE PRINTER STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM				Due						Due						
Customer Service Rep. Initials																

[1] Based on usage of device, Branch Manager establishes number of months between PM TASKS (Avg. usage is 60 hrs/wk or less; high usage is more than 60 hrs/wk) by circling appropriate usage number.

[2] Circle TASKS status if problem encountered. Record data and action taken on back.

[3] References are to pages in this manual.

[4] Circle Ⓒ for clean, Ⓡ for replace.

[5] Branch Manager fills in this part of schedule (peripherals shown are only for example).

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FIGURE 5-3: SAMPLE PM SCHEDULE

PMs should be performed on the 50 Series system once a month. Some peripherals require some PM each month, if only cleaning and inspection. The peripheral PM schedule has space for the Branch Manager to list the peripherals on a system. Peripheral PMs should be scheduled to coincide with the main frame PM. Doing peripheral and main frame PMs together aids in staggering the extended (extra time needed for PM) PMs that are periodically required on each peripheral (example: head alignment checks on disks). Note the use of STD (standard) and EXT (extended) PM for this purpose on example schedule Figure 5-3.

The schedule is quick and easy to complete. Take the schedule to the site. Enter the date in the appropriate column, check off the task status for those tasks performed and initial the bottom box. If a problem is discovered, circle the task status instead of the check. Enter the date and a brief (one line) explanation of action taken on the back of the schedule.

The Branch Manager should refer to individual service manuals to aid in scheduling peripheral PMs.

5.5 MAINTENANCE TOOLS

The following materials and equipment are required to service the main cabinet and I/O cabinet.

- Portable Vacuum Cleaner
- Kim-Wipes (large size)
- Household Cleaner
- Digital Voltmeter
- Front Air Filters (MEC2684-004)
- Bottom Air Filters (MEC5579-002)

5.6 PM PROCEDURE

The 50 Series system PM procedure is provided in the next subsections.

5.6.1 SYSTEM SHUTDOWN

The system shutdown procedure is outlined in the following steps.

1. Discuss system operation with the customer/operator. Take note of any complaints.
2. Inspect the system for obvious malfunctions.
3. Spool and review the system and network event logs.
4. If the system is up, have the operator bring it down.
5. Check for proper blower motor operation and airflow in the cabinet.

6. Cycle down the peripherals, then shut off ac power.

7. Shut off the main power switch on the status panel and turn the keylock

8. Turn the main PDU circuit breaker off.

5.6.2 CLEANING AND INSPECTION

To properly service and maintain the 50 Series system in a FCC cabinet:

1. Vacuum or replace the cabinet air filter and check the blower belt.

   A) Open the front door.
   B) Vacuum or replace the front air filter (MEC2684-004).
   C) Check the blower belt (MEC6529-001) for wear and replace as needed.
   D) Close the front door and open the rear door.
   E) Vacuum or replace the bottom filter (MEC5579-002).

2. Vacuum loose dust and dirt from the insides of the cabinet.

CAUTION

Do NOT attempt to service the inside filter with ac power applied to the cabinet.

3. Remove any visible dirt from the outside of the cabinet using a Kim-wipe dampened with household cleaner.

4. Check for loose power and cable connections.

To properly service the and maintain the 50 Series system in a non-FCC cabinet:

1. Vacuum loose dust and dirt from the insides of cabinets.

2. Clean or replace cabinet filters.

   A) Remove front-bottom dress panel of each cabinet.
   B) Remove the filter grill.
   C) Clean or replace the 6.50 x 21.75 front filter (MEC2684-002).
   D) Remove the inside filter bracket.
   E) Clean or replace the 6.50 x 16.75 inside filter (MEC2684-001).
   F) Reassemble filter in cabinet and replace dress panels.

CAUTION

Do NOT attempt to service the inside filter with AC power applied to the cabinet.

3. Remove any visible dirt from the outside of the cabinets, using a Kim-wipe dampened with household cleaner.

4. Check for loose power and cable connections.

5.6.3 PERIPHERALS

Clean the peripheral cabinets in the same manner as the mainframe. Additional PM guidelines are listed for each type of device. Refer to the appropriate Service Manual for more specific PM and adjustment procedures.

5.6.3.1 Disk Drives (Removable)

To check the disk drives:

1. Check any disk errors reported in the event log.
2. Inspect the pre-filters which should be changed monthly.
3. Inspect the absolute filters which should be changed every six months.
4. Inspect the shroud, spindle and lockshaft. These should be cleaned and the lockshaft should be lubricated every six months.
5. Do NOT clean the heads during PM.

5.6.3.2 Magnetic Tape Drives

To check magnetic tape drives:

1. Inspect the head area for cleanliness and wear. Clean head area if necessary.

NOTE

Use the cleaning solution recommended for the device. Otherwise, the tape head may be damaged (refer to the appropriate Service Manual).

2. Explain to the customer that the drive head must be cleaned periodically between PM calls.

5.6.3.3 System Console (TERMINET)

To check the system console:

1. Check for accumulation of dust and dirt inside the printer. Any buildup should be removed with a cloth dampened in alcohol or dry compressed air (if available).

CAUTION

Do NOT get alcohol inside of the bearing surfaces. Do NOT lubricate the clutches.

2. Check all the mechanical parts to see if any are loose or worn.
3. Install shutdown kits whenever possible.

5.6.3.4 Printers

To check the printers:

1. Clean and lubricate all mechanical parts. Use a vacuum cleaner and a soft brush to clean the print face.

2. Check for parts which are wearing out. Also check for loose parts and wires caused by vibration.

3. Make any necessary electrical and mechanical adjustments.

4. Explain to the customer that the printer should be cleaned periodically between PM calls, to maintain quality printing.

5.6.3.5 Terminals (CRTS)

Care for terminals as follows:

1. Adjust monitors as necessary.

2. Clean keyboards as needed using a Kim-wipe dampened with household cleaner. Do this carefully to avoid damaging the logic circuits underneath the keys.

5.7 ENVIRONMENTAL CHECKOUT

Inspect the computer room to make sure that the system environmental specifications listed in Chapter 2 of this manual are met. If not, notify the customer. Upon returning to the office, notify the Branch Manager. The Branch Manager will follow-up with the customer to resolve the problem.

5.8 SYSTEM STARTUP

Once PM is completed, have the operator bring up the system normally. Operate all peripherals to ensure that they are working properly. If any problems arise when bringing up the system, refer to the troubleshooting procedures in Chapter 6 of this manual.

CHAPTER 6
CORRECTIVE MAINTENANCE

6.1 CORRECTIVE MAINTENANCE OVERVIEW

This section contains a troubleshooting guide and adjustment procedures. The troubleshooting guide includes diagnostic operating procedures, a listing of error and warning messages, as well as a trouble isolation procedure. Maintenance tools and logic levels for the 50 Series systems are presented below.

6.1.1 MAINTENANCE TOOLS & MATERIALS

A standard Customer Service tool kit is required for proper maintenance and adjustment.

6.1.2 LOGIC LEVELS

The 50 Series systems use TTL logic levels. These logic levels are presented in Table 6-1.

TABLE 6-1: 50 SERIES SYSTEMS LOGIC LEVELS

LOGIC STATE	TTL LEVEL
True = 1	+2.5V to +5.5V
False = 0	0.0V to +0.4V

6.2 TROUBLESHOOTING GUIDE

This troubleshooting guide presents a logical approach to troubleshooting the 50 Series systems. System operations, along with troubleshooting information, are presented in the following order:

- General Troubleshooting Notes
- VCP Verification
- Micro-Verify Error Handling
- Troubleshooting System (PRIMOS) Halts
- Troubleshooting Common System Problems
- Troubleshooting With LOGREC

6.2.1 GENERAL TROUBLESHOOTING NOTES

The following are suggestions to aid the CSR in troubleshooting the 50 Series systems.

1. When isolating problems with multiple devices, reconfigure to a minimum configuration as with memory boards. Also remember that each physical FMD, SMD or CMD has its own I/O transmitters and receivers on the 4004/4005 controllers.

2. Many of the procedures and guides in this chapter give instructions to isolate a bad controller, CPU, etc., and replace it. Isolation, in most cases, means eliminating the good parts to get to the bad one. Elimination should be an orderly removal, one at a time of possible causes. If the removal of a PCB will affect the running of the system for verification, replace it with a known good board. Also, if removal of a PCB affects your ability to recreate the problem, replace it with a known good controller.

3. Return all original parts and PCBs to their original slot numbers and configuration after the faulty part has been replaced.

4. *DOS64 is the only version that will support the new file system effective at PRIMOS Rev. 14 and higher. In order to load and run *DOS64, the system must have a minimum of 128K bytes contiguous memory.

5. When troubleshooting problems with disks it is sometimes helpful to be able to copy from one device to another. If both devices are the same type (i.e. two storage modules) the COPY command may be used. If the devices are not the same (i.e. a storage module and a 12Mb MHD) FUTIL may be used. FUTIL can be used to copy files or whole UFDs.

6. All I/O controllers except the VCP have BPAPEL, BPAPER, BPDPEL and BPDPER lines disabled. Hence BUS parity errors will be detected and reported only by the VCP board.

6.2.2 VCP VERIFICATION

The VCP verify tests the dynamic memory RAMs and the High Speed Buffer (HSB). The VCP verify test is initiated by Master Clear or the VIRY instruction.

6.2.2.1 VCP Dynamic RAM Test

The VCP verify begins with a test of dynamic memory. This test makes four passes with each pass doing the following:

Pass 1 - Write all 0's (zeros)

Pass 2 - Write all 1's (ones)

Pass 3 - Write low-half and high-half of each address

Pass 4 - Write all 0's (zeros)

During the memory test the Remote Active indicator on the status panel is on and the Remote indicator is extinguished. The Stop indicator is on for all verify tests.

NOTE

Since the VCP tests dynamic memory before it tests the serial ports, these lights may be the only indication of a memory failure if the serial port is inoperative.

The dynamic memory is 32K x 8 bits and is addressed from 2000 to 9FFF (all addresses are in Hexadecimal). Each of the 8 bits is made up of one 16K x 1 chip so it is necessary to have two 16K x 1 chips for each bit.

The lower 16K is addressed from 2000 to 5FFF. The upper 16K of memory is addressed from 6000 to 9FFF. The VCP RZ PROM does not indicate the failing address, just the bit in error, which means any failing bit may be one of two chips. Memory failures appear on the system console in the form of:

Bad RAM # (# is the RAM in error)

The RAM number is the opposite of the data bit, see Table 6-2.

A message of BAD RAM #2 is interpreted as either a bad RAM at location 3M or 5M. Replace one RAM at a time to fix the problem.

TABLE 6-2: VCP RAM DECODE CHART

DATA BIT	0	1	2	3	4	5	6	7
LOWER 16K RAM LOCATION	9P	1L	3L	9L	7P	5M	7M	3N
UPPER 16K RAM LOCATION	5N	1M	5L	7L	7N	3M	9M	1N
BAD RAM #	7	6	5	4	3	2	1	0

6.2.2.2 VCP High Speed Buffer Test

The VCP uses a 22-bit High Speed Buffer (HSB). The HSB is composed of twenty-two (22) 82s11 (or 93425) ICs which are 1K words by 1 bit. Each 82s11 corresponds to 1 HSB bit. The HSB is broken into three parts: Low, Middle and High. The HSB High is bits 01 to 06, the HSB Middle is bits 07 to 14 and the HSB Low is bits 15 to 22.

The HSB is tested by the VCP verify routine which is invoked by either a Master Clear or by the VIRY instruction. An error message appears on the system terminal when an error is encountered.

The format for a data bit error follows:

BADHSB L 01000000 AT 0000

BADHSB is the error type, L indicates HSB Low, the next 8 bits (6 for the HSB High) are the data bits and the last four bits are the address. Any data bit which is non-zero is the failing bit.

An address failure is reported as follows:

BADHSB ADDRESS AT 0000

If there is a data or address failure, replace the VCP PCB.

6.2.3 MICRO-VERIFY ERROR HANDLING

The micro-verify feature provides 50 Series processors with a self-test capability. These microcode routines are structured so they will verify successively larger portions of the hardware.

Micro-verify runs two passes. The first pass is with Machine Check mode disabled. The second pass is with Machine Check mode enabled. Certain tests will only fail in pass two. These tests are defined in Tables 6-3, 6-4 and 6-5.

6.2.3.1 Micro-Verify Initialization

Micro-verify can be initialized two ways. The first is by pressing the Master Clear switch. After successfully completing micro-verify the address lights will contain an octal 1000. If micro-verify failed the address lights will contain 177777 and the data lights will contain the failing test number. The failing test number can also be found in the Diagnostic Status Register (DSWSTAT) low side, bits 10 through 16.

Micro-verify can also be initialized by the VIRY instruction. In the Machine Check mode a verify error will cause an interrupt to a specific location in segment four. Refer to the load map for the revision of software in use (RING0.MAP or RING3.MAP located in PRIRUN).

6.2.3.2 P850/P750 Micro-Verify Differences

The micro-verify tests run by the P850 microcode are almost identical to the P750. There are some differences, however.

Upon Power-up, depressing Master Clear, or issuing a VIRY/SYSCLR instruction, the Master Clear sequence is initiated. The first set of microcoded instructions, called APEIN, is a routine which initializes the SSU. After completion of APEIN and SYSVRY, micro-verify begins. In Uni-mode, the ISU selected is the only stream operating, and therefore microverifies much like a P750. However in Multi-mode, micro-verify sequencing is handled differently.

In Multi-mode, ISU-1 will be the first of the two streams to execute microverify, followed immediately by ISU-2 (ISU Slave). Since ISU-1 is the only stream to perform device driver operations, the Slave will bypass the I/O related tests. Once ISU-1 (I/O Master) has successfully completed microverification, it will delay for approximately one second to allow the other processor to finish. After pausing, the Master will check the contents of the Slave State Cell. This cell will indicate whether or not the Slave passed microverify. If the Slave State Cell contains '1000, then the message "***CPU VERIFIED***" will be displayed, otherwise "$$$CPU DID NOT VERIFY$$$" will be displayed. If microverify should fail, the Slave State Cell should be accessed to determine which ISU failed. If the cell contains an '1000, then the Master has failed. Otherwise the cell should contain the failing test number or zero (0) indicating that the Slave never completed micro-verify. If the Master has failed, then DSWSTAT should be dumped and the failing test number noted.

In any case, if micro-verify should fail, the suspected CPU should be tested in its respective Uni-mode by Master Clear and the appropriate diagnostic.

Since the Slave does not do an I/O, it will jump around all I/O related micro-verify tests (i.e. test #34, #47, #50, #51, and #52). The ISUs will also use different memory locations for BMD tests #53 and #54 (ISU-1 => '100, ISU-2 => '102). Also BD SHIFT and ROTATE tests have been merged into a single test to create a test number for #60, the Micro-second Timer test.

TABLE 6-3: MICRO-VERIFY TESTS, P350/P400

TEST P1 P2	FUNCTION	POSSIBLE CAUSE (Highest First)
0 40	Test INCREA and REAL16	1) CPU A-bd. 2) CPU B-bd.
1 41	Test control unit stack	1) CPU B-bd. 2) CPU A-bd.
2 42	Test adder paths (CPU)	1) CPU A-bd. 2) CPU B-bd.
3 43	Machine Check following adder test	1) CPU (either board)
4 44	Machine Check resettable	1) CPU B-bd. 2) CPU A-bd.
5 45	Rd = 0 test	1) CPU B-bd. 2) CPU A-bd.
6 46	RMA = 0 test	1) CPU B-bd. 2) CPU A-bd.
7 47	REA = 0 test	1) CPU A-bd. 2) CPU B-bd.
10 50	RP(P-Counter) = 0 test	1) CPU A-bd. 2) CPU B-bd.
11 51	RD = -1 test	1) CPU B-bd. 2) CPU A-bd.
12 52	RMA = -1 test	1) CPU B-bd. 2) CPU A-bd.
13 53	REA = -1 test	1) CPU A-bd. 2) CPU B-bd.
14 54	RP = -1 test	1) CPU A-bd. 2) CPU B-bd.
15 55	Machine Check following register tests	1) CPU (either board)
16 56	Test not used	
17 57	Register file parity	1) CPU A-bd. 2) CPU B-bd.
20 60	Cache data parity test	1) CPU B-bd. 2) CPU A-bd.
21 61	BMA(memory address bus) parity test	1) CPU B-bd. 2)Memory-1st bd. 3) CPU A-bd.
22 62	BMD(memory data bus) parity test	1) CPU B-bd. 2)Memory-1st bd. 3) CPU A-bd.
23 63	RPA parity test	1) CPU A-bd. 2)I/O controller 3) CPU B-bd.
24 64	RDX parity test	1) CPU A-bd. 2) CPU B-bd.
25 65	Cache (index) tests	1) CPU B-bd. 2) CPU A-bd.
26 66	Machine Check following cache tests	1) CPU (either bd.) 2)I/O controller
27 67	BPA data test - 052525	1) I/O controller 2) CPU
30 70	BPA data test - 125252	1) I/O controller 2) CPU
31 71	BPD data test - 052525	1) I/O controller 2) CPU
32 72	BPD data test - 125252	1) I/O controller 2) CPU
33 73	Machine Check following I/O tests	1) CPU (A or B) 2) I/O controller
34 74	BMD data test - 052525	1) Memory 2) CPU (A or B bd.)
35 75	BMD data test = 125252	1) Memory 2) CPU
36 76	Machine Check following memory tests	1) CPU (A or B bd.) 2) Memory

TABLE 6-3: MICRO-VERIFY TESTS, P350/P400 (Cont.)

NOTE

1. When Micro-verify errors occur, the failing Micro-verify test number will be displayed in the Data lights. All 1s (177777) will be displayed in the Address lights.

2. P1 = pass 1, without Machine Check mode enabled. P2 = pass 2, with Machine Check mode enabled. 'Machine check following -----tests' indicates that if the tests fail, they should only fail on the second pass (P2).

3. When Micro-verify fails, the "bad" data pattern is contained in TR5 (refer to Chapter 3).

TABLE 6-4: MICRO-VERIFY TESTS, P500

TEST P1	P2	FUNCTION	POSSIBLE CAUSE (Highest First)
0	40	TEST INCREA and REAL16	1) CPU A-bd. 2) CPU B-bd.
1	41	Test control unit stack	1) CPU B-bd. 2) CPU A-bd.
2	42	Test adder paths	1) CPU A-bd. 2) CPU B-bd.
3	43	Machine check resettable	1) CPU B-bd. 2) CPU A-bd.
4	44	RD = 0 test	1) CPU B-bd. 2) CPU A-bd.
5	45	RMA = 0 test	1) CPU B-bd. 2) CPU A-bd.
6	46	REA = 0 test	1) CPU A-bd. 2) CPU B-bd.
7	47	RP(P-Counter) = 0 test	1) CPU A-bd. 2) CPU B-bd.
10	50	RD = -1 test	1) CPU B-bd. 2) CPU A-bd.
11	51	RMA = -1 test	1) CPU B-bd. 2) CPU A-bd.
12	52	REA = -1 test	1) CPU A-bd. 2) CPU B-bd.
13	53	RP = -1 test	1) CPU A-bd. 2) CPU B-bd.
14	54	Machine Check following register tests	1) CPU (either bd.)
15	55	Register file parity	1) CPU A-bd. 2) CPU B-bd.
16	56	Cache data parity test	1) CPU B-bd. 2) CPU A-bd.
17	57	BMA parity test	1) CPU B-bd. 2) Memory 3) CPU A-bd.
20	60	BMD parity test	1) CPU B-bd. 2) Memory 3) CPU A-bd.
21	61	RPA parity test	1) CPU (either) 2) I/O controller
22	62	RDX parity test	1) CPU A-bd. 2) CPU B-bd.
23	63	Cache (index) tests	1) CPU B-bd. 2) CPU A-bd.
24	64	BPA data test - 052525	1) I/O controller 2) CPU
25	65	BPA data test - 125252	1) I/O controller 2) CPU
26	66	BPD data test - 052525	1) I/O controller 2) CPU

TABLE 6-4: MICRO-VERIFY TESTS, P500 (Cont.)

TEST P1 P2	FUNCTION	POSSIBLE CAUSE (Highest First)
27 67	BPD data test - 125252 and Machine Check following I/O tests	1) I/O controller 2) CPU 1) CPU 2) Memory
30 70	BMD data test - 052525	1) Memory (loc. 100) 2) CPU
31 71	BMD data test - 125252 and Machine Check following memory tests	1) Memory (loc. 100) 2) CPU 1) CPU 2) Memory
32 72	XIS load/unload test	1) CPU XIS 2) CPU A 3) CPU B
33 73	XIS adjust and normalize	1) CPU XIS 2) CPU A 3) CPU B
34 74	XIS binary multiply	1) CPU XIS 2) CPU A 3) CPU B
35 75	XIS binary divide	1) CPU XIS 2) CPU A 3) CPU B
36 76	XIS decimal arithmetic	1) CPU XIS 2) CPU A 3) CPU B
37 77	All tests not run	1) CPU (either boards)

NOTE

1. When Micro-verify errors occur, the failing Micro-verify test number will be displayed in the Data lights. All 1s ('177777) will be displayed in the Address lights.

2. P1 = pass 1, without Machine Check mode enabled. P2 = pass 2, with Machine Check mode enabled. 'Machine Check following -----tests' indicates that if the tests fail, they should only fail on the second pass (P2).

3. When Micro-verify fails, the "bad" data pattern is contained in TR5 (refer to Chapter 3).

TABLE 6-5: P750/850 MICROVERIFY TESTS

TEST NUMBER		
PASS1	PASS2	DESCRIPTION
0	100	Test of INCREA and JUMP REAL16
1	101	Test of 16 locations in CU STACK
2-5	102-105	A Board ALU tests: Logical functions of ALU, 16 and 32 bit increments, carrys in and out, condition codes, link & Cbit settings.
6	106	Machine Check following ADDER tests
7	107	Machine Check resettable
10	110	RD = 0
11	111	RMA = 0
12	112	REA = 1
13	113	RP = 0
14	114	RD = -1
15	115	RMA = -1
16	116	REA = -1
17	117	RP = -1

TABLE 6-5: P750/850 MICROVERIFY TESTS (Cont.)

TEST NUMBER		
PASS1	PASS2	DESCRIPTION
20	120	Machine Check following Register tests
21-23	121-123	DECREA and INCREA, DECREA by 2
24-25	124-125	INCRP and RP backup 1 after INCRP
26-27	126-127	INCRP by 2 and RPBACKUP 2 after INCRP by 2
30-31	130-131	REAH tests
32	132	Register File Parity
33	133	REA Parity
34	134	RPA Parity
35	135	BMA Parity
36	136	RDX Parity
37	137	BMD Parity
40	140	CACHE Parity
41	141	Prefetch test of Generic
42	142	Prefetch Buffer Address Parity test
43	143	Prefetch test of short MR
44	144	Prefetch test of short Indirect
45	145	Prefetch test of long, two word Indirect
46	146	CACHE tests
47-50	147-150	BPA data test '52525, & '125252
51	151	BPD data test '52525
52	152	BPD data test '125252 and Machine Check
53	153	BMD data test '52525
54	154	BMD data test '125252 and Machine Check
55	155	Load all 128 locations of RF
56	156	32 bit CACHE read even and odd boundary
57	157	BD SHIFT/ROTATE tests
60	160	Go 100 U-SEC TIMER tests
61-62	161-162	STLB tests
63-64	163-164	XIS load/unload tests
65	165	Loading RS emitting constants to RFE
66	166	Zeroing
67	167	RF addressing
70-71	170-171	XALU tests
72-73	172-173	Normalize and Adjust tests
74	174	Multiply
75	175	Divide
76	176	Normalize backshift case
77	177	Decimal Arithmetic
		ALL TESTS RUN

6.2.4 TROUBLESHOOTING SYSTEM (PRIMOS) HALTS

The System (PRIMOS) Halts are listed and defined in Table 6-6. Four of these halts MCHK, MEMPA, PWRFL and MMOD are discovered by system hardware. The rest of the halts, are less common and are spotted by either system software or firmware.

The following items and related information are required to troubleshoot system halts:

- Hardware Diagnostic Status Registers
- General System Halt Handling
- Memory ECCU Error Handling
- Machine Checks Handling
- Troubleshooting Flowcharts

NOTE

The locations at which PRIMOS halts occur are defined in the PRIMOS load maps (RING0.MAP and RING3.MAP). These maps are in the UFD in which PRIMOS was built and from which it is normally RESUMED (usually UFD PRIRUN). To determine the actual halt location, check the address within the correct segment. System halts, along with their locations, are listed in Table 6-6.

TABLE 6-6: SYSTEM (PRIMOS) HALTS

HALT	LOCATION	DEFINITION
AMLCI_	*	Spurious AMLC interrupt.
BOOT0_	*	SHUTDN ALL stops here.
IFLTB_	*	Bad fault in interrupt process.
INTRT_	*	Too many returns in interrupt process.
IPAGF_	*	Bad page fault in interrupt process.
MCHK_	4/305	Machine check.
MEMH2_	*	Halt after auto mapping out page.
MEMPA_	4/276	Memory parity halt (non ECCC). When an uncorrectable parity error is detected during normal operations the system halts. The halt location is called MEMPA and the actual halt location may be unique to the revision of software. Refer to the ECCU Error Handling in this chapter for corrective action.
MMOD_	4/315	Missing memory check.
PAGFB_	*	Page fault when not allowed.
PWRFL_	4/204	Power failure.
REFL0_	*	Flex, UII or PSU when not allowed.
RCMF0_	*	Restrict mode fault when not allowed.

TABLE 6-6: SYSTEM (PRIMOS) HALTS (Cont.)

HALT	LOCATION	DEFINITION
SVCF4_	*	SVC when not allowed.
XRNG0_	*	Illegal ring number in supervisor.

* Halt locations change between revisions. See the load maps (RING0.MAP and RING3.MAP) for your specific system.

6.2.4.1 Hardware Diagnostic Status Registers

The two diagnostic status word registers that are used to troubleshoot the four system halts listed previously are DSWSTAT and DSWPARITY. These registers contain machine state and parity error information. Each register is 32 bits long and is divided into a high and low side composed of sixteen bits each. DSWSTAT and DSWPARITY word formats are shown in Tables 6-7 through 6-10. Refer to these tables when using the machine halt error handling routines in the next subsections.

TABLE 6-7: DSWSTAT WORD FORMAT: HIGH SIDE

BITS	CONTENTS WHEN 1	DEFINITION
1	CHECK IMMEDIATE	The check was taken as soon as the trap was taken in the microcode.
2	MACHINE CHECK	The cause of the check was a machine check.
3	MEMORY PARITY	The cause of the check was a memory parity error on incoming data from memory.
4	MISSING MEMORY	The cause of the check was a missing memory module trap.
5-7	MACHINE CHECK CODE	111 = Register File Data Parity 110 = BMA Parity 101 = External Data Register Parity 100 = BPA Parity 011 = Cache Data 010 = BMD Parity 001 = BPA Parity 000 = BPD Parity
8	NOT RCM	Not Register Control Memory.
9	ECCU	Together with Bit 3, means that the memory parity error was an ECC uncorrectable.
10	ECCC	Together with Bit 3, means that the memory parity error was an ECC correctable.
11	BUP INV	RP backup count invalid.
12-14	RP BAK	RP backup count (subtract from DSWPB).
15	DMX	A direct memory transfer was in progress at the time of the error.
16	IO	An Input/Output operation was in progress at the time of the error.

TABLE 6-8: DSWSTAT WORD FORMAT: LOW SIDE

BITS	CONTENTS WHEN 1	DEFINITION
1	SYNDROME 4	ECC Syndrome Bits. If caused by a memory parity error, the syndrome bits describe the error. Refer to the ECCC Memory Error Handling Guide in this chapter to interpret the syndrome bits.
2	SYNDROME 3	
3	SYNDROME 2	
4	SYNDROME 1	
5	SYNDROME 0	
6	OP	Overall parity.
7	--	Not used.
8	MOD #	Low order address bit of module in error.
9	RMA VAL	DSWRMA is not valid.
10-16	--	Micro-Verify Test number

TABLE 6-9: DSWPARITY WORD FORMAT: HIGH SIDE

BIT	SIGNAL NAME	PCB	PURPOSE
1	RPARERR1+	CS	DMX Input E6: BPD or BURST- R0,R2 : BPD or BURST- R0,R1,R2,R3 DMX Output : BMD
2	RPARERR2+	CS	DMX Input E6: BPD or BURST- R1,R3 : BPD DMX Output : BMA
3	FBDMX+	CS	BURST-MODE DMX Transfer
4	BURST-INPUT+	CS	0=DMX Input, 1=DMX Output
5 6 7			
0 0 0	FPDPE+	J	Peripheral reports BPD error (Output)*
0 0 1	FBRFHPE+	J	Base register file high*
0 1 0	FMDPE+	J	Memory reports BMD error (Write)*
0 1 1	FIPBAPE+	J	Prefetch buffer address*
1 0 0	FPAPE+	J	Peripheral reports BPS error (Output)*
1 0 1	FBRFLPE+	J	Base register file low*
1 1 0	FMAPE+	J	Memory reports BMA error*
1 1 1	FIPBIPE+	J	Prefetch buffer instruction*
8	RCMPE-	A	RCM parity if no board reported error**
9	FMDECCU+	J	Memory reports ECC uncorrectable error on read**
10	FDPDPE-	J	Prefetch board detected error**
11	BPAIPE+	A	BPA input error (DMX or Interrupt)**
12	FRDXPE+	A	RDX error when most recently closed**
13	FRFPE+	A	Register file error**
14	FREAPE+	A	REAH or REAL error**
15	FDMX+	J	DMX cycle at time of error**
16	APERR+	AP	AP board detected error**

* Bit 10 = 1
** Bit 10 = 0

TABLE 6-10: DSWPARITY WORD FORMAT: LOW SIDE

BIT	SIGNAL NAME	PCB	PURPOSE
1	GCBDPE-	C	C board detected error
2	FBMDEVPE+	C	BMD input even word
3	FBMDODPE+	C	BMD input odd word
4	LMMOD+	C	Missing memory module at CACHE-MISS
5	LBMAPE+	C	Memory reports BMA error at CACHE-MISS
6	LFERNEXT-	C	RMA was incremented at time of error (CACHE-MISS)
7	LFLRMA15+	C	Indicator of BMA15 at time of error (CACHE-MISS)
8	LMISFL16+	C	Indicator of BMA16 at time of error (CACHE-MISS)
9	LBMDECCU+	C	Memory reports ECC uncorrectable on CACHE-MISS
10	LBMDECCC+	C	Memory reports ECC correctable on CACHE-MISS
11	LRCIAPE+	C	CACHE-INDEX error on CACHE-READ
12	LRCDODPE+	C	CACHE-DATA odd word error on CACHE-READ
13	LRCDEVPE+	C	CACHE-DATA evev word error on CACHE-READ
14	LFSERVDBD	C	Purpose if CACHE CYCLE: 1=Execute, 0=Prefetch
15	Not Used		
16	Not Used		

6.2.4.2 General System Halt Handling

Locations at which PRIMOS halts are defined in the PRIMOS load maps (RING0.MAP and RING3.MAP). These maps are in the UFD in which PRIMOS was built and from which it is normally RESUMED (usually UFD PRIRUN). To determine the actual halt location, check the address within the correct segment.

For effective use of system halt handling, familiarize yourself with VCP operations as described in Chapter 3. Refer to the troubleshooting flowcharts for additional troubleshooting tips.

NOTE

DO NOT Master Clear or SYSCLR at this point.

The following steps outline system halt handling:

1. Note the halt location that appears on the system console. This will contain the segment number and address of the halt.

2. Go to the load maps for PRIMOS (RING0.MAP and RING3.MAP). Look up the halt location in the map. The address or previous address should indicate a recognized halt location. Use the troubleshooting flow charts to aid in isolating the cause of the halt.

3. If the halt is not identifiable, then consult your Branch's assigned specialist or Regional Support Group for aid in identifying the halt.

4. Dump and record the register settings.

NOTE

DSWPARITY is a register which has been designated for the P750/850 systems to contain detailed parity information and it, not DSWSTAT, should be your main source of information for these two systems.

A) CP> D DSWRMA (register 34)
B) CP> D DSWSTAT (register 35)
C) CP> D DSWPB (register 36)
D) CP> D DSWPARITY (register 27)

5. If possible, take a memory-to-tape dump as follows:

A) Mount a scratch tape on MT1 (MT0 if Rev 19 or greater).
B) CP> SYSCLR
C) CP> RUN 776 (775 if Rev 19 or greater)

Memory will be dumped to tape, indicated by tape motion, and the program will halt.

D) Record the time & date of the halt and the density of the tape (800bpi, 1600bpi, etc.) on the tape and set it aside along with all other information recorded on this halt.

6. Refer to the troubleshooting flowcharts to correct the problem if possible at this time.

7. Cold Start or Warm Start as required:

A) Cold Start, reboot the system from scratch.
B) Warm Start as follows:

```
CP> SYSCLR
CP>RUN
HALTED AT:  1001:  000010
CP> RUN
***WARM START***
```

6.2.4.2.1 850 Halts

Procedures for handling 850 and SSU halts follow.

When dealing with unexpected halts on an 850 system, first figure out which ISU caused the halt. This can be determined by accessing the LAST_CPU register which contains the unique bit pattern of the ISU that caused/detected the malfunction (refer to Table 6-11). If the bit pattern indicates ISU-1 then the diagnostic Status Words (DSWPB, DSWRMA, DSWSTAT and DSWPARITY), and registers 0, 1 and 3, should be dumped and examined. If the Slave is implicated, then the Slave's Status Words should be obtained.

Bit #16 of the register AP_CTRL is provided for swapping I/O Mastership. This function will allow examination of the Slave's registers after a system halt (refer to Table 6-11). Once the identity of the reporting ISU is known, the failure can be isolated in a manner similar to the P750.

NOTE

In certain cases I/O Mastership can't be changed. If this happens, access the following SSU locations for ISU 2:

A 14/2556/7 (DSWPARITY)

A 14/2570/1 (DSWRMA)

A 14/2572/3 (DSWSTAT)

A 14/2574/5 (DSWPB)

A 14/2704/5 (L)

A 14/2717 (X)

A 14/2750 (KEYS)

TABLE 6-11: 850 DEBUG REGISTERS

LOCATION	REGISTER NAME	PURPOSE
4/176100	SLV_RUN	Slave Run Cell '0000 ISU-2 did not start
4/176104	SLV_STATE	Slave State Cell '1000 Slave passed micro-verify '0000 Slave hung in micro-verify '0 - '177 Failing Test #
4/176106*	LAST_CPU	CPUNUM of last CPU to HALT '041004 ISU-1 (I/O Master) '102010 ISU-2 (I/O Slave)
4/176400	AP_CTRL	850 Control Register '000014 VCP talks to ISU-1 '000015 VCP talks to ISU-2

*If this location contains an '041004, then the top ISU (Master) halted and the HALT location printed at the systems console is correct. If the location contains '102010, the bottom ISU (Slave) halted and the HALT location must be obtained by examining the crash save area of PRIMOS. The Slave's HALT address is contained in locations 14/2516 (segment) and 14/2517 (word).The Slave's DSWPARITY can be examined at location 14/2556 and 14/2557.

6.2.4.2.2 SSU Halts

Located at the rear of the SSU board are four LEDs that indicate current board status. From left to right they are SSU Parity Error, Multi-mode, Uni-mode Top and Uni-mode Bottom. If the SSU Parity Error LED should glow continuously, this indicates that the SSU has detected a parity error in its internal bus structure. APT1 should be run at this time to determine the nature of the failure. Replace the SSU if necessary. This LED will flash momentarily during Master Clear indicating that the microcode routine APEIN is forcing bad parity within the SSU. This is considered normal.

6.2.4.3 Memory ECCU Error (MEMPA) Handling

Uncorrectable errors halt the system, requiring immediate intervention by the operator or Customer Service Representative if on-site. (Memory ECCC errors do not halt the system but are recorded on LOGREC. See the LOGREC Troubleshooting subsection in this chapter for information on handling ECCC errors.)

NOTE

Never use the MASTER CLEAR button or the SYSCLR and VIRY commands before recording the halt location in the system logbook and determining all of the recovery actions to be performed. Some recovery actions are ineffective unless they are taken before using MASTER CLEAR, SYSCLR, or VIRY.

1. When the system halts, do not Master Clear or SYSCLR. Fetch and record registers 0, 1 and 2 in mapped memory mode. These registers contain the following information:

   Register 0 = Current User Number
   Register 1 = PPN (Physical Page Number)
   Register 2 = WN (Word number displacement

2. Note the Diagnostic Status Word (DSWSTAT) that appears on the system console.

3. If the user number recorded in Step 1 is a 0 or 1, the system has to be cold started because the error is in the operating system and must not be locked out. If the system is to be cold started, this may be a good time to repair or replace the memory board.

4. If the user number (Register 0) is greater than one, the page may be automatically locked out in memory by going back to run by entering RUN (do not Master Clear). This locks out the page (1024K words) to system use, in memory only. If the system is ever reloaded (Cold Started) subsequent to this, the page will not be locked out anymore. Now Master Clear and Warm Start the system.

NOTE

Inform the system operator of the user number indicated in Register 0. This user will be affected by the lock out and should not continue the job, but should restart the job.

5. If the system (PRIMOS) stays up for one minute after Warm Starting, the memory parity error is recorded in LOGREC. Otherwise, a SHUTDN ALL has to be done in order to get the error recorded.

6. Using the information from LOGREC or the registers (recorded in step 2), isolate the bad memory chip as outlined under the Troubleshooting with LOGREC subsection in this chapter.

6.2.4.4 Machine Check Handling

Machine checks occur when the CPU detects bad parity on one of its internal data paths or one of the external buses (BPD, BPA, BMA or BMD out). Machine checks can be caused by the CPU, controllers or memory.

Machine checks during PRIMOS operation are detectable by system halts at location 4/305 (segment 4, location 305 octal). On PRIMOS, the first halt after a Cold Start causes the entire register file set to be saved in memory. This save is not disturbed until the next Cold Start. Reference the memory maps for revision of PRIMOS being run, for the location of these saved registers, if they are needed.

Upon detecting the machine check halt, the CPU reports the status of the check in its diagnostic status word (DSWSTAT) located in the register files at location "abs" (absolute), 5 octal, high and low side. Use the following steps to isolate the cause for a machine check.

NOTE

Never use the MASTER CLEAR button or the SYSCLR and VIRY commands before recording the halt location in the system logbook and determining all the recovery actions to be performed. Some recovery actions are ineffective unless they are taken before using MASTER CLEAR, SYSCLR or VIRY.

1. Note the DSWSTAT that appears on the system console.

2. Use the information obtained from diagnostic status word high side (DSWSTATH) and Table 6-12 to aid in isolation of the bad component of the system.

3. A Warm Start is not recommended after a Machine Check halt. However, in order to get the halt recorded in LOGREC, you must Warm Start and keep up the system for one minute or do a SHUTDN ALL. It is recommended that no user activity be reinitiated after a Machine Check, until a Cold Start is possible.

TABLE 6-12: MACHINE CHECK CODES DEFINED

DSWSTATH (ABS loc. 35 octal)

Bit =	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
	C	M	M	M	MCC			R	E	E	B	RPBUP			D	I
	I	C	P	M	MACH			C	C	C	U				M	/
					CHK			M	C	C	N				X	O
					CODE				U	C	V					
								*								

MC= set - indicates a Machine Check error.
Look at MCC and RCM to identify the source of error.

MCC = (5-7)	Type of Failure	Possible Cause (In order of likelihood)
000 0	None	---
001 1	BPD	1-CPU, 2-controller
010 2	BMD	1-CPU, 2-Memory
011 3	Cache data	1-CPU
100 4	BPA parity	1-CPU, 2-controller
101 5	STLB	1-CPU, 2-controller
110 6	BMA parity	1-CPU, 2-Memory
111 7	A-Board parity	1-CPU

*NOTE: RCM (bit 8)=RESET - indicates the CPU has a microcode parity error. MCC is invalid.
= SET - no RCM parity. MCC is valid.

6.2.4.5 Troubleshooting Flowcharts

Figures 6-1 through 6-5 and Tables 6-13 through 6-17 explain troubleshooting procedures for each of the following conditions:

- The system will not boot.
- The system halted while running PRIMOS.
- The system has halted and cannot MASTER CLEAR.
- The system has a valid PRIMOS halt.
- The system halted during a cold start.

TABLE 6-13: SYSTEM WILL NOT BOOT

CONDITION	
System won't boot (see Figure 6-1).	
NOTE When troubleshooting disks, it is helpful to copy from one device to another. If both devices are the same type (i.e., two storage modules) the COPY command may be used. If the devices are not the same type (i.e., a storage module and a 12 MB MHD) FUTIL is used. FUTIL can be used to copy files or whole UFDs.	
ACTIONS	NOTES
1. Proceed to the appropriate service manual for disk drives. 2. Use boot tape to load PRIMOS II and necessary partitions. Restore customer software and rebuild the system pack. 3. Refer to the appropriate service manual for that particular drive. 4. Replace controller. 5. If a bad power supply is found, replace it. 6. Replace bad controller. 7. Check the boot sense switches.	1. Check for loose cables or dirty connectors. Reseat boards and top hats. See that memory chassis is configured properly and disk address is '26 or '27. 2. Check that these conditions exist: • Local/remote switch set to local • BOOT drive has plug 0 in it • No fault lights lit • Disk pack has not crashed CAUTION If pack appears crashed DO NOT put the pack in another drive. DO NOT put another pack into a drive that appears crashed until you have determined that it did not crash. If the carriage does not move on BOOT attempt, there may be an access control problem. 3. Use boot tape or boot from another drive. To boot from another drive refer to the switch table in Chapter 3 of this manual. 4. Use the second disk controller if available or boot from magnetic tape.

TABLE 6-13: SYSTEM WILL NOT BOOT (Cont.)

ACTIONS	NOTES
	5. Remove all controllers except the controller that was booted from. Replace controllers one at a time or until the bad one has been isolated.

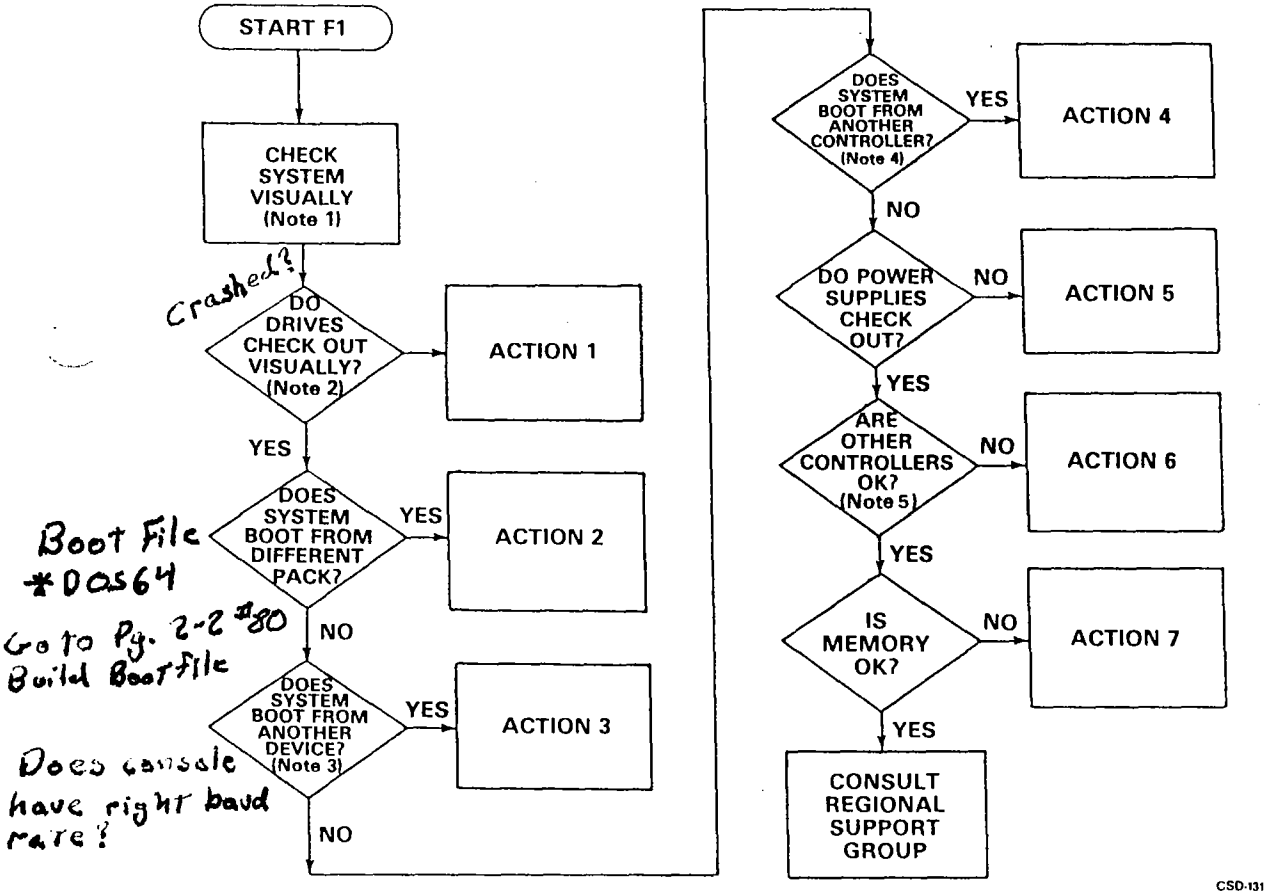

FIGURE 6-1: SYSTEM WILL NOT BOOT FLOWCHART

TABLE 6-14: SYSTEM HALTS DURING PRIMOS

CONDITION	
System halted while running PRIMOS. (See Figure 6-2.)	
ACTIONS	NOTES
1. The HALT may be due to changes to customer programs, revisions of changes and/or revisions to software system configuration. Run original configuration and software or run AUTO PRIMOS. If patches are required contact the Systems Analyst.	1. At system HALT, VCP prints a halt location (segment/location: contents). No printout may mean a bad power supply. Go to F3.
2. Check if any external programs were started prior to HALT. If so run the system without the program. If the system runs, contact the Systems Analyst.	2. Dump the contents of the following registers: DSWSTAT DSWRMA DSWPARITY DSWPB A 0,1,3 Refer to Memory ECCU Error (MEMPA) Handling in this chapter.
3. Check Repair Center Bulletin #11 for the latest board revisions.	3. Although it is stressed to NOT WARM START after a Machine Check, this should be done to get HALT recorded in LOGREC. After running more than a minute, LOGREC is updated. Do a SH ALL, cold start and spool LOGREC. If a Warm Start is impossible, access LOGLST saving register information even if the last update was not made. Earlier failures give clues about recent ones.
4. Check the HALT location in the system load map. The HALT could have been in a semaphore or driver for a controller of the CPU. With help from Regional Support Group, replace the suspected controller, CPU, memory or power supply. Go to F3 START if the system does not come back up. Monitor the system after board replacement to see if problem recurs.	4. More common halts (MEMPA, MCHK,MMOD) are in LOGREC. If halt not in LOGREC see system load map. This leads to an area where the problem may be.
5. Reseat loose boards, ICs, cables and hard hats. Clean dirty edge connectors.	5. Depending on register analysis, if spooler is active suspect URC. If mag tape is active suspect tape controller. If synchronous communications are involved suspect SMLC, HSSML, MDLC or ICS1.
	6. Refer to PRIMOS Halt Handling Guide step #5 to do a tape dump. Do a cold

TABLE 6-14: SYSTEM HALTS DURING PRIMOS (Cont.)

ACTIONS	NOTES
	or warm start as directed by Regional Support. Have tape analyzed to determine problem's cause.

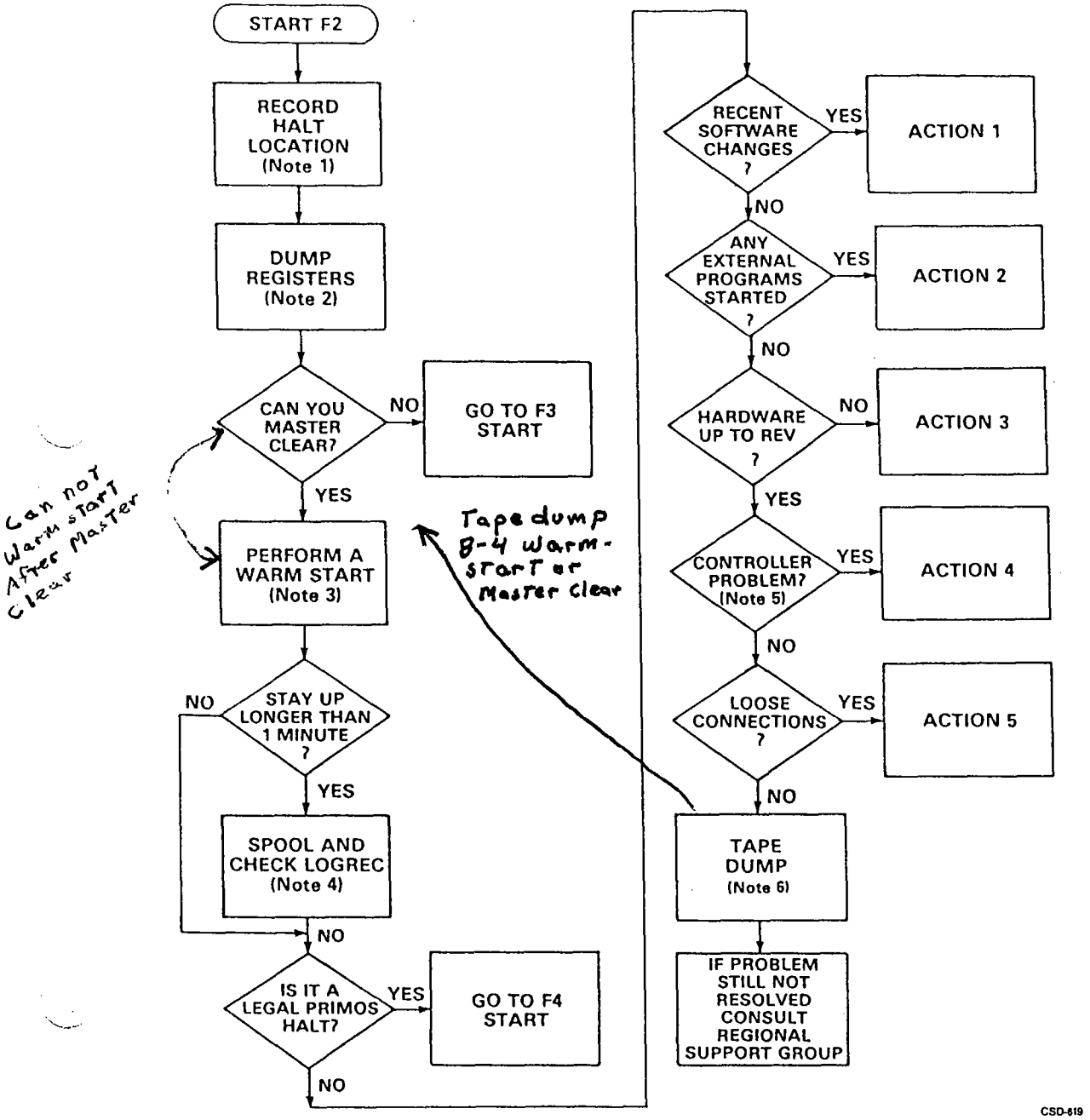

FIGURE 6-2: SYSTEM HALTS FLOWCHART

TABLE 6-15: SYSTEM HALTS & DOES NOT MASTER CLEAR

CONDITIONS
1. The system has halted. 2. The system does not Master Clear. (See Figure 6-3.)
NOTE When troubleshooting a Master Clear problem, check the dc voltages from all Prime power supplies and their power fail line (PSRLY). Unplug all PCBs in the system that are not required for a Master Clear. Only the CPU, VCP, status panel and 2MB of memory are required to Master Clear a system.

ACTIONS	NOTES
1. Refer to POWER SUPPLY CHECKS & ADJUSTMENTS to check the power supply. If power supply is bad, replace it and Cold Start system.	1. If DSWSTAT doesn't appear on the system console, suspect the VCP and run the microdiagnostics.
2. If a controller is bad, check for obvious problems (broken wire, lifted IC, etc.). Else, replace the controller and restart.	2. Are ERR075 or ERR350 shown? No lights or blinking lights may also indicate a power supply problem. VCP on = 5V OK, VCP flashing = Low P.S. in Lower chassis
3. Pull all but one memory board. If problem corrected, locate the bad memory board by running memory tests to give you the information to find the board.	3. Remove all controllers except VCP. If the system Master Clears, add controllers, one at a time, until the bad one is found. Load P.S. with at least 12.1 amps Or remove P.S. VCP = 15 Amps.
4. If the backplane is bad, replace the backplane.	4. To isolate a backplane problem, first configure a minimum system in the top 17 slots and then in the bottom 17 slots. Be sure to unplug the unused power supplies from ac power and the backplane. When moving boards up or down to previously unused slots, do not overload the power supplies or break the interrupt or DMX priority nets (see Priority Networks Chapter 4).
5. Run the Micro-verify tests. If the problem still exists, contact your regional support office.	5. The CPU can be swapped on a board-by-board basis as long as the replacement boards are the same revision level.

If DSWSTAT shows a 140000. check: Top hats and Mem. Board Switches

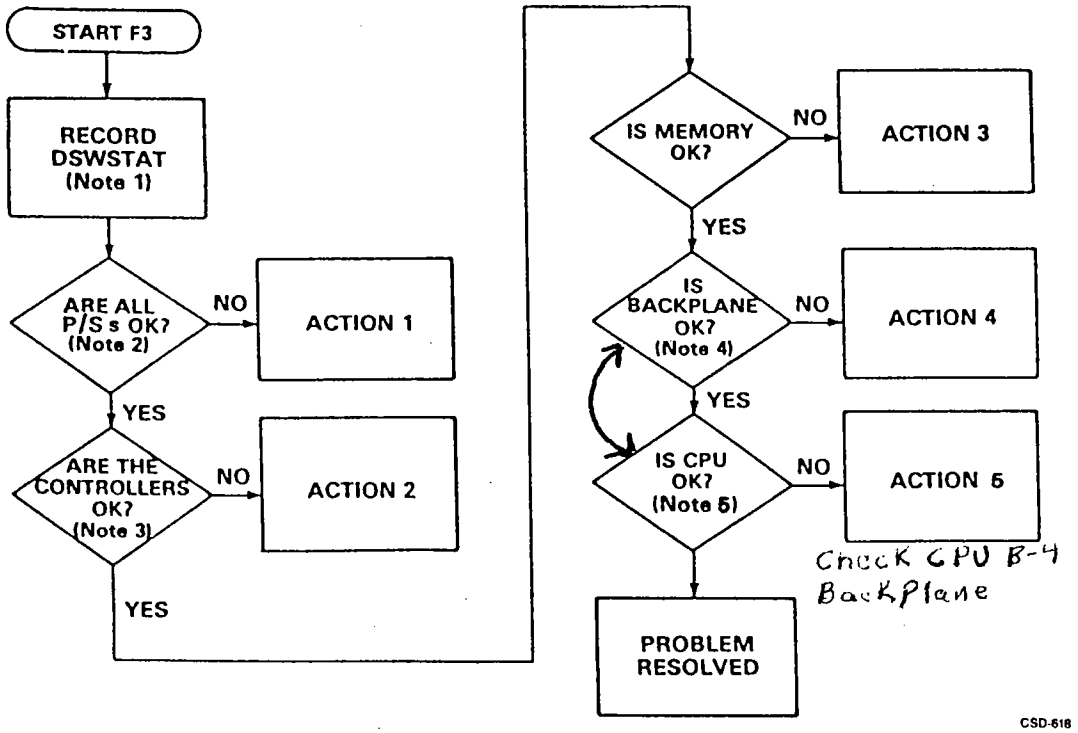

FIGURE 6-3: SYSTEM HALTS AND DOES NOT MASTER CLEAR FLOWCHART

TABLE 6-16: VALID SYSTEM HALTS

CONDITIONS	
1. System has halted. 2. Halt is a valid PRIMOS halt. (See Figure 6-4.)	
ACTIONS	NOTES
1. This is a Memory Parity halt (MEMPA_). Usually this error is a bad bit.	1. Suspect the following: a. Memory Board b. I/O Controller c. Power Supply
2. This is a Machine Check halt (MCHK_). If halt is recorded in the LOGREC, use error message to determine what caused the halt. Refer to the Machine Check Handling Guide in this chapter.	2. Suspect the following: a. CPU b. Controller c. Memory d. Backplane Assembly
3. This is a Missing Memory Trap (MMOD_). Obtain PPN/WW information by doing a Warm Start and a SH ALL. There is a good chance that a fuse has blown.	3. Suspect the following: a. Memory b. CPU c. AMLC, ICS1, ICS2 (could be a bad address)
4. This is a Power Fail halt (PWRFL_). Suspect bad power supply or bad input power.	4. Use the map RING0.MAP (located in PRIRUN) for actual halt locations. Note that a new release of software could cause a halt.

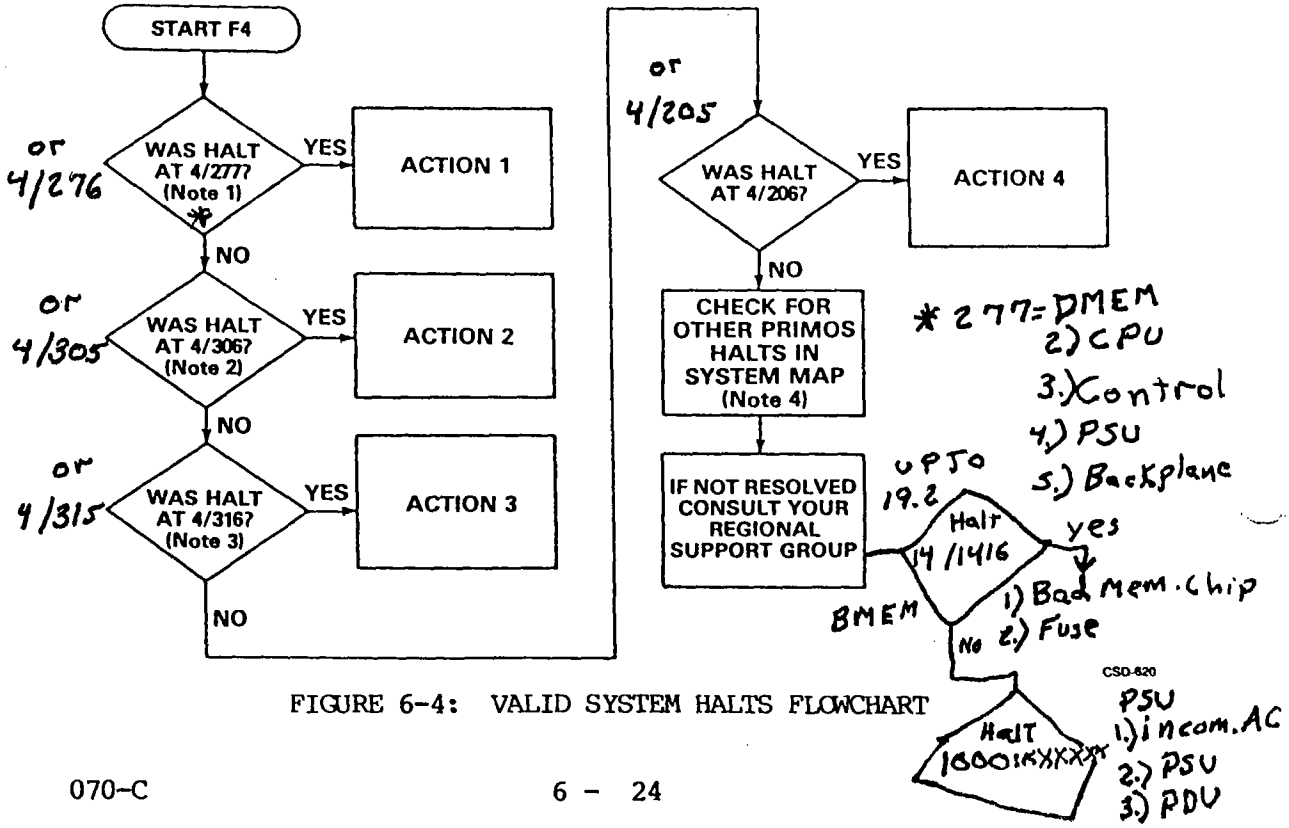

FIGURE 6-4: VALID SYSTEM HALTS FLOWCHART

TABLE 6-17: SYSTEM HALT DURING COLD START

CONDITION	
System halts during a Cold Start. (See Figure 6-5)	
ACTIONS	NOTES
1. Fix the configuration file.	1. Check configuration file for a "GO" statement. Be sure that CMDNCO is in COMDEV, partition PAGDEV is formatted and drive is not write protected. See that MAX-PAG correctly reflects memory size. Make sure that sure that the necessary partitions are "MADE" and that software libraries are installed.

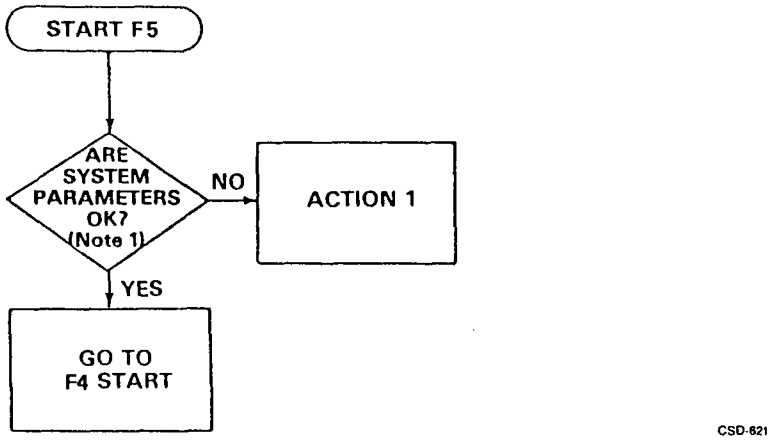

FIGURE 6-5: SYSTEM HALTS DURING COLD START FLOWCHART

6.2.5 TROUBLESHOOTING COMMON SYSTEM PROBLEMS

Some common system problems are:

- No indicator lights
- System hangs
- System console is dead
- Slow system
- System crashes

Troubleshooting procedures for these conditions are provided in Tables 6-18 through 6-24 and Figures 6-6 to 6-11.

TABLE 6-18: NO LEDS

CONDITION	
No indicator lights are lit when the Power On button is pressed. (See Figure 6-6.)	
ACTIONS	NOTES
1. Check PDU ac Circuit breaker; power to cabinet; power cord. See if fans are plugged into PDU. 2. Check ac power to 1045/1051 power supply. Check PDU fuse. 3. Check cable to status panel. Check status panel.	None.

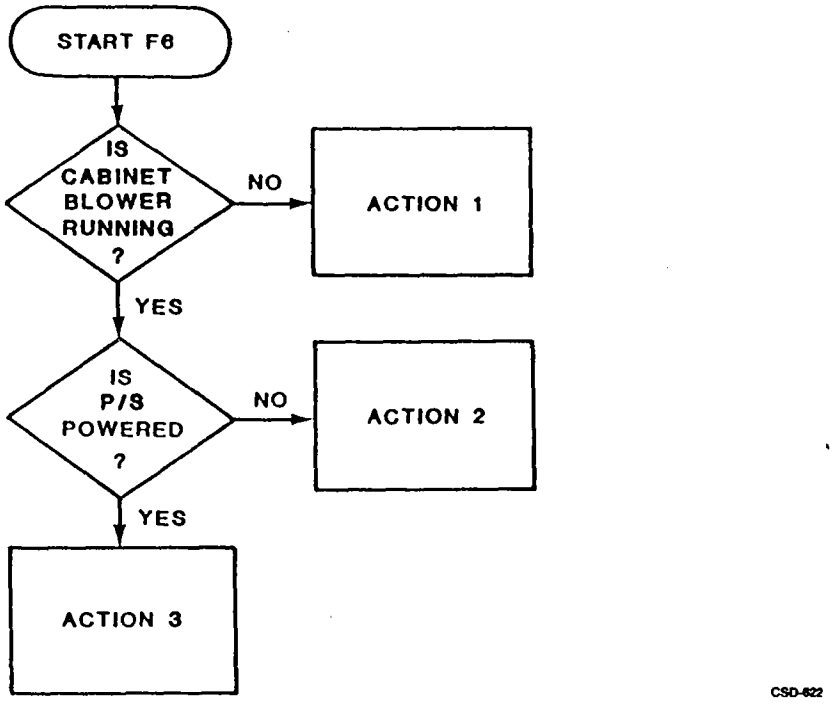

FIGURE 6-6: NO LEDS LIGHT FLOWCHART

TABLE 6-19: SYSTEM HANGS

CONDITIONS	
1. System hangs. 2. System was running PRIMOS and was on-line to users. 3. No ongoing problems present. (See Figure 6-7.)	
ACTIONS	NOTES
1. Use the MCLUP command. This releases the shared lock that any MIDAS process might have hung. If unsuccessful, run system without MIDAS, consult Systems Analyst. 2. If PRIMOS has been altered, run a known good PRIMOS pack and see if machine still hangs. Repair Centers should have a PRIMOS Pack (try AUTO PRIMOS). If unsuccessful consult your Regional Support Group. 3. See if any attempts have been made to log into the system just prior to the hang. 4. Some PRIMOS revisions can cause these problems. Check with Systems Analyst to see if patches are needed on your current revision of PRIMOS. 5. Check RCB #11 Board Revision Summary, to find latest revisions. Make sure boards match revision levels. CPUs and memory boards must be at latest revisions. 6. When bad controller is found, check for obvious problems (dirty contacts, broken address jumpers, loose wires, and loose PROMs). If an MDLC is being used, make sure the cable is plugged into the modem and the modem is working. If not, this can cause a hang. 7. Reseat CPU PCBs, cables and hard hats. Make sure all contacts are clean and check for broken wires on CPU boards. Try to finish flowchart before swapping CPU. Run the Micro-verify tests. 8. Check all PSU test points at the time of the hang. Note that input	1. Remove all controllers not needed to run a system (only run a BMSMC and a VCP). Add controllers one at a time until the bad PCB is found. 2. CPU sets can be mixed as long as the replacement boards are at the same revision level as the boards that are being replaced.

TABLE 6-19: SYSTEM HANGS (Cont.)

ACTIONS	NOTES
power can cause system hangs. 9. Run one pair of memory boards. If the system runs, swap in pairs until the bad board is found. If no problem is found, run memory in non-Burst mode.	

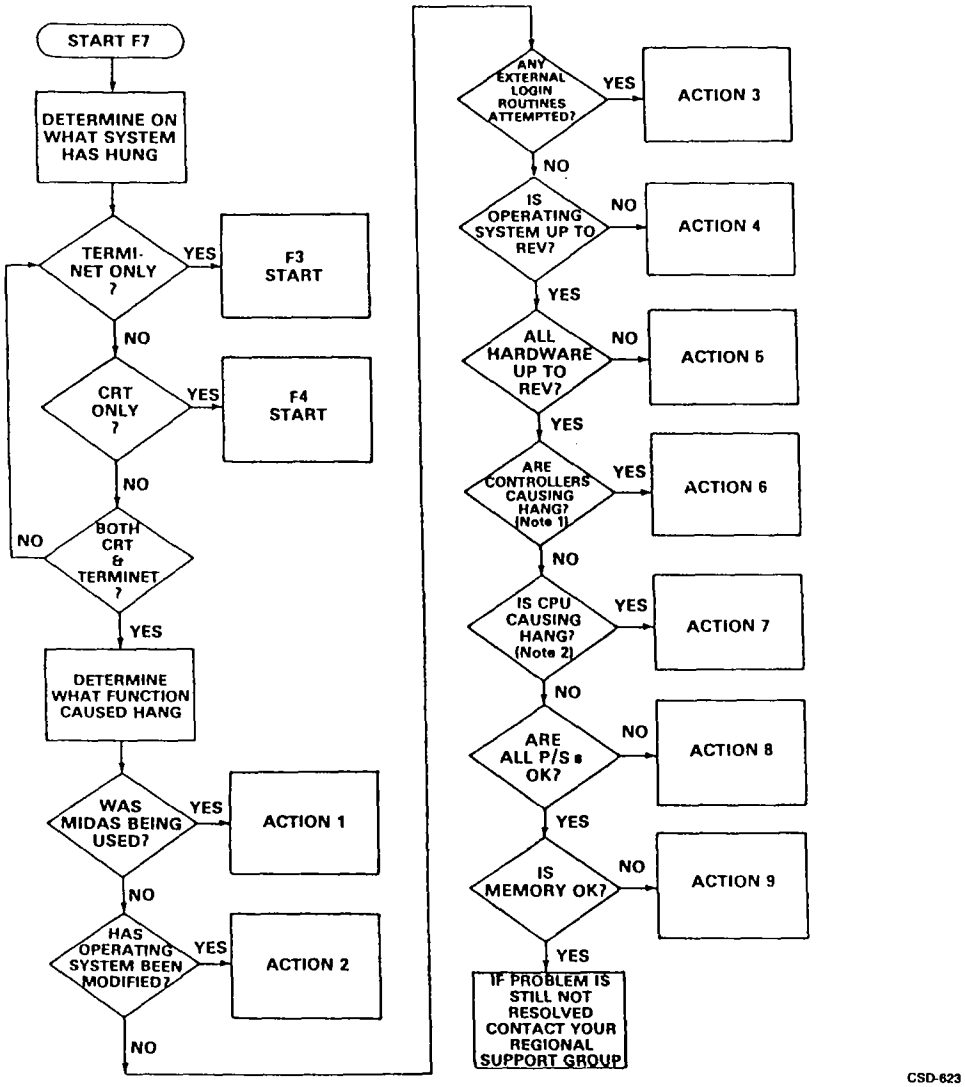

FIGURE 6-7: SYSTEM HANGS FLOWCHART

TABLE 6-20: SYSTEM CONSOLE DOES NOT RESPOND

CONDITIONS	
1. System console does not respond. 2. PRIMOS is apparently running. 3. User terminals are active. (See Figure 6-8.)	
ACTIONS	NOTES
1. Problem most likely in system console. Refer to appropriate SM to fix problem. If system console is a Terminet make sure the correct operation button is on (i.e. the Trans Key isn't depressed). 2. Check all connectors for any bent or damaged pins. If no problem is found, replace the cable.	1. At this point, if no error code can be displayed, replace the VCP.

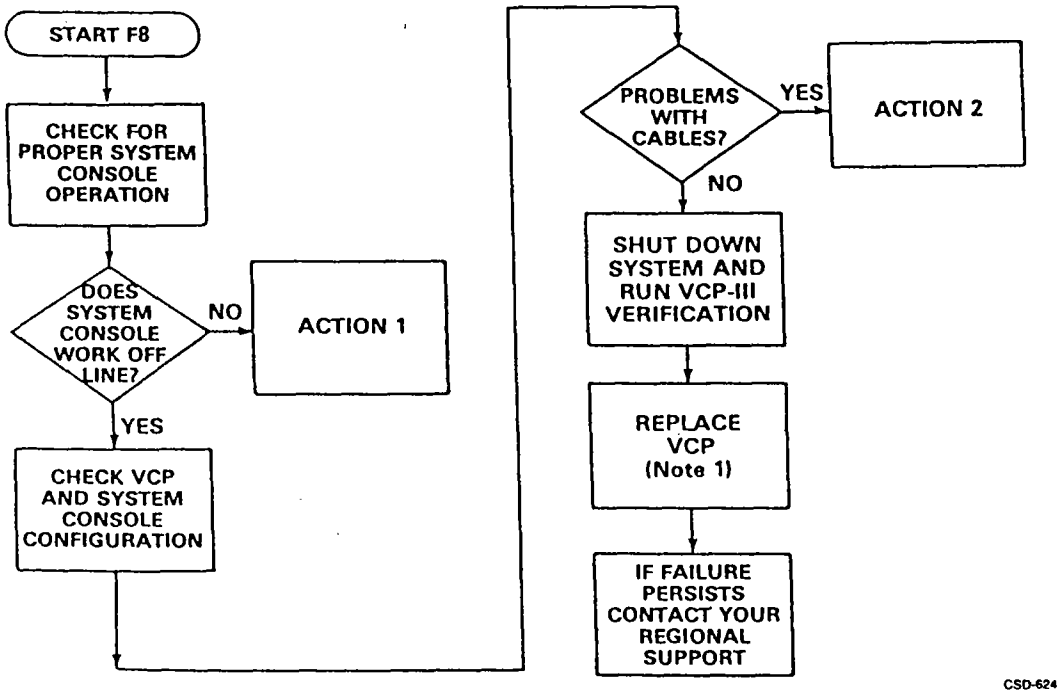

FIGURE 6-8: SYSTEM CONSOLE DOES NOT RESPOND FLOWCHART

TABLE 6-21: SLOW SYSTEM - STEP A

CONDITIONS	
1. System appears to have slowed down drastically. 2. System running PRIMOS IV. 3. No known hardware problems. (See Figure 6-9.)	
ACTIONS	NOTES
1. Replace the appropriate controller (if no change, enter the flowchart at B). 2. Replace the ICS controller. 3. Increase MAXSCH to a value between 4 and 7. (If no change perform action 4 below). 4. Eliminate CPU (clean edge connectors, reseat ICs, replace boards). (If no change, perform Tape Dump and contact Regional Support.)	1. Refer to CSMM #80 for usage. 2. Snapshot of usage should be done while the system is not running slow for comparison (refer to CSMM #80 for more information). 3. %AMLC should run approximately 1 to 1.2% per ALMC board.

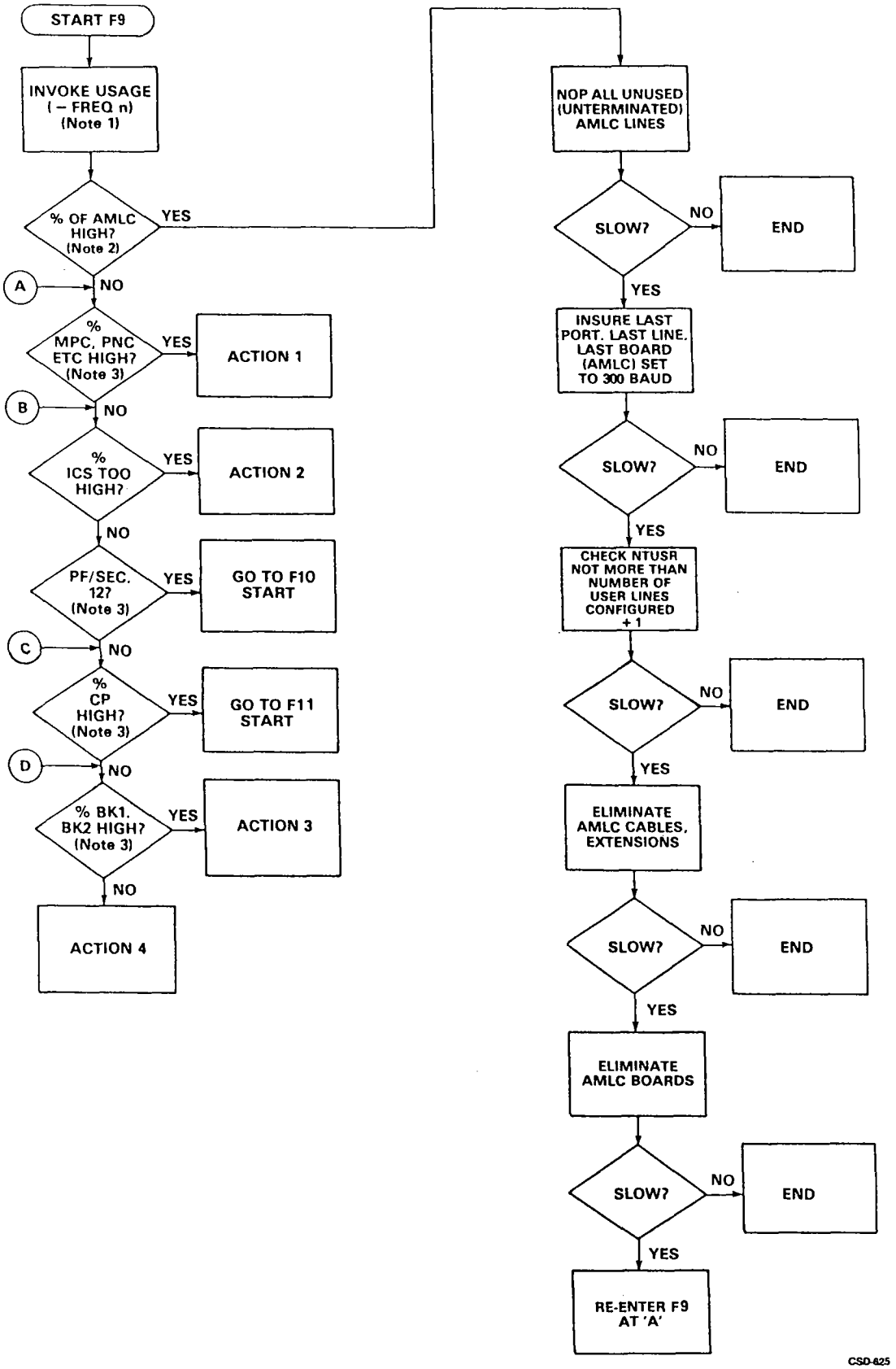

FIGURE 6-9: SLOW SYSTEM - STEP A FLOWCHART

TABLE 6-22: SLOW SYSTEM - STEP B

CONDITIONS	
1. Directed to this procedure from troubleshooting flowchart Figure 6-9. 2. System appears to have slowed down drastically. 3. System running PRIMOS IV. 4. No known hardware problems. (See Figure 6-10.)	
ACTIONS	**NOTES**
1. Set MAXPAG (in CONFIG) to equal physical memory in the system (i.e. octal 200 per quarter Megabyte). 2. With the aid of Regional Support or a Systems Analyst, determine if NUSEG can be lowered. If so, lower NUSEG. If a lower NUSEG has no effect, have the Analyst or Regional Support group discuss Alternate Paging. If this is impossible or makes no difference, re-enter F10 at A. 3. Check for AMLBUF statements entered properly. If correct, or makes no difference, re-enter F10 at B.	None.

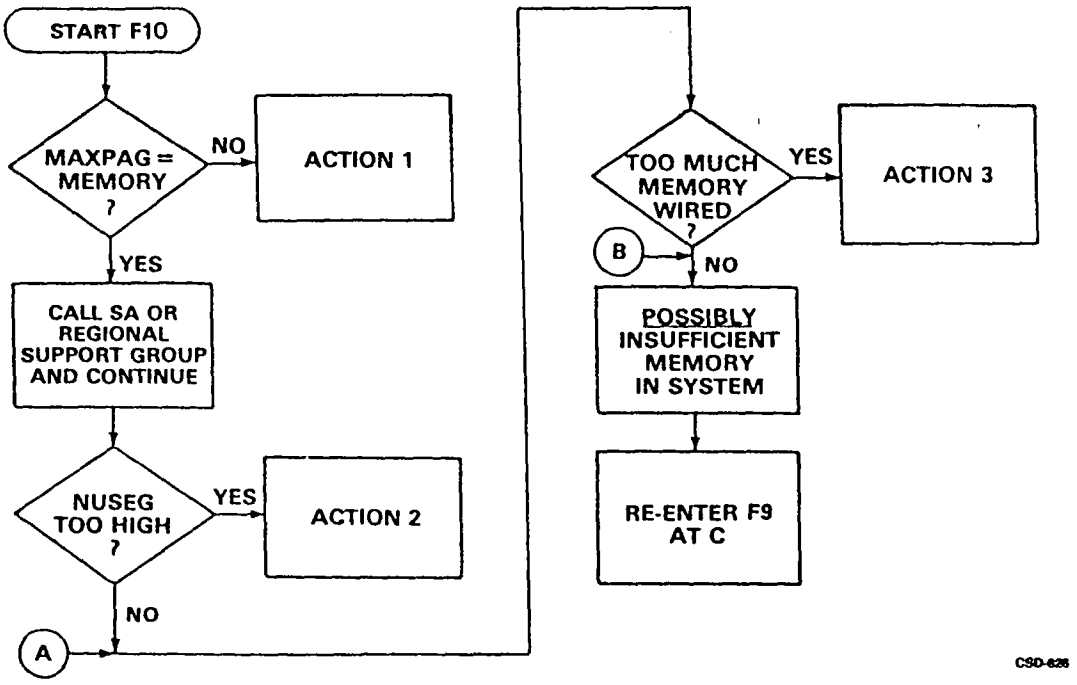

FIGURE 6-10: SLOW SYSTEM - STEP B FLOWCHART

TABLE 6-23: SLOW SYSTEM - STEP C

CONDITIONS	
1. Directed to this procedure from troubleshooting flowchart Figure 6-9. 2. System appears to have slowed down drastically. 3. System running PRIMOS IV. 4. No known hardware problems. (See Figure 6-11.)	
ACTIONS	NOTES
1. Re-enter flowchart F2 at location D. Snapshot of usage should be done while the system is not running slowly for comparison (refer to #80 service manual for details).	1. After Systems Analyst or Regional Support Group has determined MIDAS is or is not at fault, continue with this flowchart.

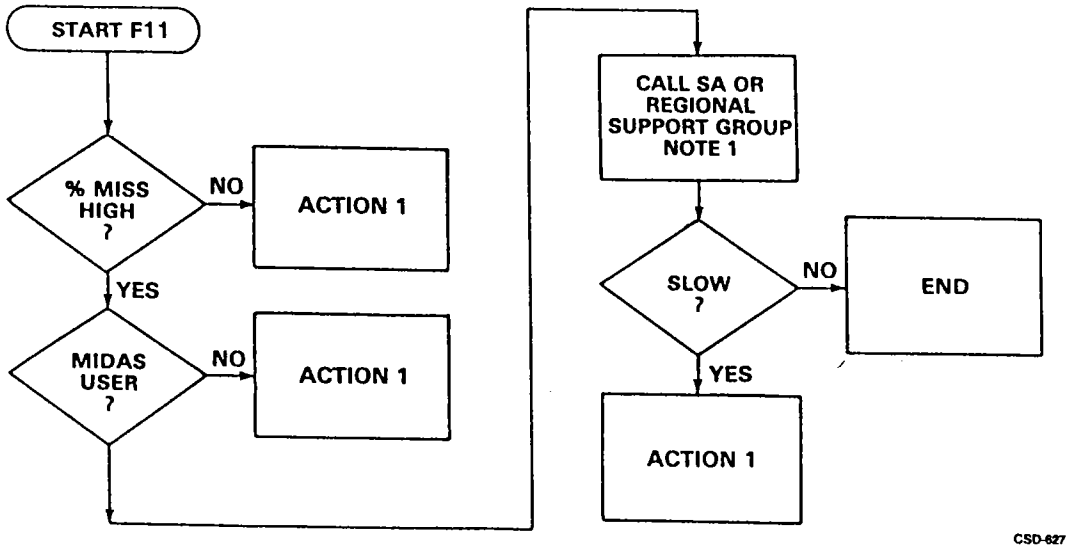

FIGURE 6-11: SLOW SYSTEM - STEP C FLOWCHART

TABLE 6-24: SYSTEM CRASH

CONDITION	
System has crashed.	
ACTIONS	NOTES
1. DO NOT MASTER CLEAR.	1. Part of this procedure is necessary to obtain the proper "historical" information in order to reconstruct cause of the the crash.
2. Record the halt location.	2. The halt mnemonic, DSWSTAT (location '35), DSWPARITY (location '27) DSWRMA (location '34) and DSWPB (location '30) are displayed on the system operator console.
3. Access and record the contents of location 0, 1 and 3.	
4. Attempt a warm start by typing "WARM" at the system operators console.	3. If a warm start is successful (stays up indefinitely) dump and spool the PRIMOS Event Log file and contact the Prime Customer Support Center (PCSC). If a warm start is unsuccessful, contact the PCSC.

6.2.6 TROUBLESHOOTING WITH LOGREC

Disk errors or machine checks are detected by the Operating System PRIMOS and reported via the system console as Systems Console Error Messages. If LOGREC is enabled, PRIMOS also records the messages on disk as LOGREC Error Messages. The disk can be accessed later for reference.

An event logger is part of the operating system that records significant events such as disk errors, Warm Starts and parity errors. During normal system operations, LOGREC is automatically updated with information not associated with system crashes. Such information includes correctable memory parity errors, correctable disk errors and adding/starting disks.

Errors that cause system crashes are added only after the system has successfully Warm Started. (An exception is PWRFL which is logged before HALT.) The system must remain running for at least one minute before LOGREC can be updated with crash information and spooled. Any information required such as diagnostic words can be acquired at this time.

The format of LOGREC is LOG.mm/dd/yy. It is recommended that the CSR periodically check LOGREC, preferably when a PM is done. LOGREC should be spooled and filed for future reference. The following information is provided by the LOGREC:

- Disk Errors
- Machine Checks
- Memory Parity (ECCC or ECCU)
- Missing Memory
- Power Fail

The LOGREC formats used to present each of these types of information are presented in detail below.

6.2.6.1 LOGREC Disk Errors

The possible LOGREC disk errors, their formats and descriptions are presented in Table 6-25.

TABLE 6-25: LOGREC DISK ERRORS

ERROR	DESCRIPTION
DISK xx ERROR	Type of operation: RD for READ, WT for WRITE.
DEVICE NUMBER=xx	The device or partition number.
TYPECODE	The controller type (4004/5) and device type (MHD, SMD, FHD).
CRA=xx	The current record address. This is separated into the record address, the head and cylinder number.
CYL=xx	The cylinder where the error was detected (in decimal).
HEAD=xx	The head number (in decimal) within the partition.
RECORD =xx	The record number (in decimal).
RCRA=xx	The current record address when the CRA is in error.
STATUS(ACCUM)=xx	The OR of all status bits obtained during retries.
STATUS(LAST)=xx	The status of the last operation. Status explanations are listed in Chapter 3 of the disk service manual.

TABLE 6-25: LOGREC DISK ERROR (Cont.)

ERROR	DESCRIPTION
RETRIES=xx yy	The number of retries attempted. If less than ten, the operation was completed successfully, yy will be recovered. If equal to ten, and the error could not be corrected by ECC, yy is Uncorrectable. If an ECC error has been successfully corrected by the software, yy is WORD NUMBER - 'xx, which gives that word number in the record and the 32 bit correction pattern used. If RETRIES equals ten, the error was unrecovered.

6.2.6.2 LOGREC Machine Checks

The possible LOGREC Machine Checks, their formats and descriptions are presented in Table 6-26. For further information refer to the Machine Check Handling Guide in this chapter.

TABLE 6-26: LOGREC MACHINE CHECKS

ERROR	DESCRIPTION
MACHINE CHECK:xx	If DSWPARITY is NOT present, an encoding of the Machine Check code is presented.
DSWSTAT=xx	Diagnostic Status Word (32 bits long) that contains a comprehensive status of the system at the time the error was detected.
DSWRMA=xx	Diagnostic Status Word Memory Address Register (32 bits) contains the address in the memory address register.
DSWPB=xx	Diagnostic Status Word Procedure Base that contains the address where the fault was detected.
DSWPARITY=xx	Diagnostic Status Word Parity (32 bits) reports board and signal name.

6.2.6.3 LOGREC Memory Parity

Memory parity errors are either correctable (ECCC) or uncorrectable (ECCU). ECCC errors are recorded in the LOGREC file during PRIMOS operation. ECCU errors are forcing the system to a Halt during PRIMOS operation, at location 4/276 octal (segment 4, location 276). This shows up as octal 277 in the address lights. The LOGREC memory parity format and a detailed ECCC Handling Guide follow.

6.2.6.3.1 LOGREC Memory Parity Format

All possible memory parity errors, their format and descriptions are presented in Table 6-27. Refer to ECCU Handling in this chapter for further information on ECCU parity errors.

TABLE 6-27: LOGREC MEMORY PARITY ERRORS

ERROR	DESCRIPTION
MEMORY PARITY (ECCC)	Indicates the error was correctable. ECCU indicates the error was uncorrectable.
DSWSTAT=xx DSWRMA=xx DSWPB=xx DSWPARITY=xx	Information is the same as for Machine Checks, except the Machine Check code does not appear and DSWPARITY is not decoded.
PPN=xx	Physical Page Number for an ECCC error followed by BIT=xx, where xx identifies the bit in error: 1-15 for bits 1-15, RP for Right Parity, C2,C4,C5 for other check bits, MB for Multibit, NE for No Error. Following the bit identification is Overall Parity=xx, where xx is 0 or 1, reflecting the setting of DSWSTATL bit 6.
WN=xx	Word number within the page where the error occurred.
REAL ADDRESS=xx	Address in Real Memory where parity error occurred.
CACHE ADDRESS=xx	Address in Cache Memory where parity error occurred.

6.2.6.3.2 Memory ECCC Error Handling

Memory ECCC errors do not halt operation, but can be a problem during system operation. Isolate and repair the bad memory board, as soon as system operation makes it convenient. If memory errors occur at random on different page numbers and different bits, a refresh problem is indicated and the board has to be replaced.

- To identify the failing chip on the memory board, use the procedure outlined below. An example using this procedure follows the outline.

1. Locate the ECCC error recorded in the LOGREC printout.
2. Note the value of the Physical Page Number (PPN) and the Word Number (WN).
3. Form the Real Address using the PPN for the first twelve Most Significant Bits (MSBs) and the WN for the ten Least Significant Bits (LSBs).
4. Check bit number 24 of DSWSTAT to determine which board of the interleaved pair holds the failing chip.

5. Use the decode charts, Tables 6-28 through 6-30 to find the board and RAM in error. Figure 6-12 shows the locations of the RAMs on the E6,E7, E8 or E9 memory board.

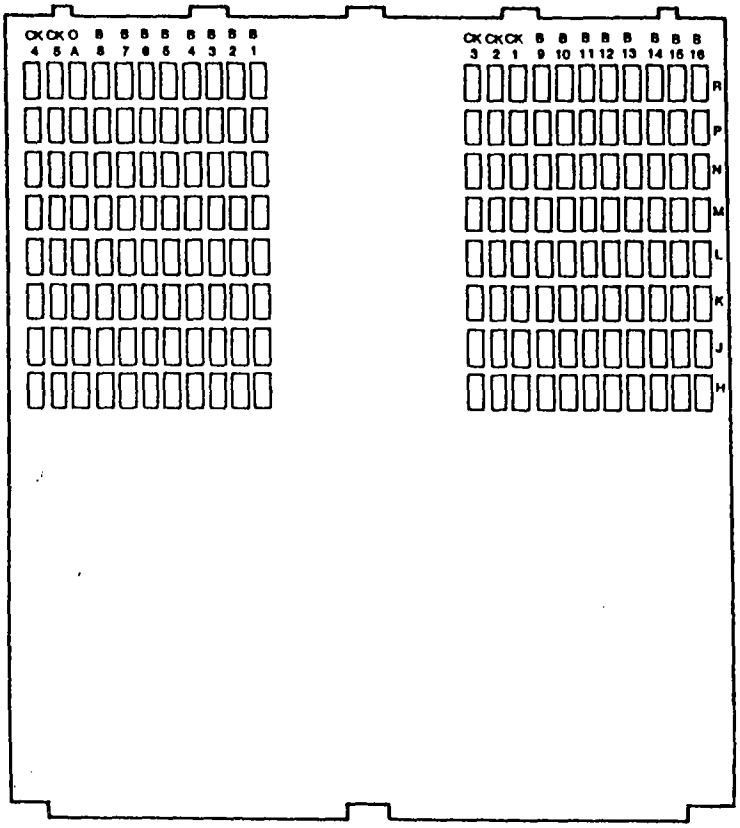

FIGURE 6-12: E6, E7, E8 AND E9 MOS RAM LOCATIONS

A typical ECCC error, as recorded in LOGREC, is shown in Figure 6-13. The following example uses the information in Figures 6-12, 6-13 and the procedure outlined previously to detail how to isolate the failing RAM on an E6, E7, E8 or E9 memory board.

```
                    13:55:00 MON 13 FEB 1984
MEMORY PARITY (ECCC) DSWSTAT= 020104 024400 DSWRMA= 000006 017654
          DSWPB= 000006 023540 PPN,WN= 000016 001654 BIT= 14
```

Note: PPN, WN, and ADDRESSES are octal numbers.

FIGURE 6-13: MEMORY ECCC ERROR

1. Locate the ECCC error recorded in the LOGREC printout (Figure 6-13).

2. Note the value of the PPN, 000016, and the WN, 001654.

3. Form the 24 bit Real Address as follows:

A) Note that the first twelve MSBs of the Real Address is the PPN and that the ten LSBs of the address is the WN.
B) Convert the WN to binary:
'001654 = 000 000 001 110 101 100
C) The ten LSBs of the WN (1 110 101 100) become the ten LSBs of the Real Address.
D) Convert the PPN to binary:
'000016 - 000 000 000 000 001 110
E) The twelve LSBs of the WN (000 000 001 110) become the twelve MSBs of the Real Address.
F) Convert the Real Address to octal:
0 000 000 011 101 110 101 100 =
'035654

4. To determine which board of the interleaved pair holds the failing chip, check the value of DSWSTAT bit #24 as follows:

A) Note DSWSTAT high and low: Even #, Larger than zero = True

DSWSTATH = 020104
DSWSTATL = 024400

B) Convert DSWSTAT high and low to 16 bit numbers:

DSWSTATH = 0 010 000 001 000 100
DSWSTATL = 0 010 100 100 000 000

C) Determine the value of DSWSTAT bit #24: 0.

5. Refer to the decode charts (Tables 6-28 through 6-30) to find the board and RAM in error using:

- Real Address
- Physical Page Number (PPN)
- Value of DSWSTAT Bit #24

Figure 6-12 shows the RAM locations on the E6, E7, E8 or E9 memory board.

6. Bit = 14 of the error message (see Figure 6-13) indicates the bad bit for the location. Obtain a copy of the error message from LOGREC to turn in with the board for repair.

TABLE 6-28: 256KB INTERLEAVED DECODE (12128-E6)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
00000000	00037777	0000	0017	TOP	2ND	H
00040000	00077777	0020	0037	TOP	2ND	J
00100000	00137777	0040	0057	TOP	2ND	K
00140000	00177777	0060	0077	TOP	2ND	L

TABLE 6-28: 256KB INTERLEAVED DECODE (12128-E6) (Cont.)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
00200000	00237777	0100	0117	TOP	2ND	M
00240000	00277777	0120	0137	TOP	2ND	N
00300000	00337777	0140	0157	TOP	2ND	P
00340000	00377777	0160	0177	TOP	2ND	R
01000000	01037777	0400	0417	3RD	4TH	H
01040000	01077777	0420	0437	3RD	4TH	J
01100000	01137777	0440	0457	3RD	4TH	K
01140000	01177777	0460	0477	3RD	4TH	L
01200000	01237777	0500	0517	3RD	4TH	M
01240000	01277777	0520	0537	3RD	4TH	N
01300000	01337777	0540	0557	3RD	4TH	P
01340000	01377777	0560	0577	3RD	4TH	R
02000000	02037777	1000	1017	5TH	6TH	H
02040000	02077777	1020	1037	5TH	6TH	J
02100000	02137777	1040	1057	5TH	6TH	K
02140000	02177777	1060	1077	5TH	6TH	L
02200000	02237777	1100	1117	5TH	6TH	M
02240000	02277777	1120	1137	5TH	6TH	N
02300000	02337777	1140	1157	5TH	6TH	P
02340000	02377777	1160	1177	5TH	6TH	R
03000000	03037777	1400	1417	7TH	8TH	H
03040000	03077777	1420	1437	7TH	8TH	J
03100000	03137777	1440	1457	7TH	8TH	K
03140000	03177777	1460	1477	7TH	8TH	L
03200000	03237777	1500	1517	7TH	8TH	M
03240000	03277777	1520	1537	7TH	8TH	N
03300000	03337777	1540	1557	7TH	8TH	P
03340000	03377777	1560	1577	7TH	8TH	R

TABLE 6-29: 512KB INTERLEAVED DECODE (12256-E7)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
00000000	00177777	0000	0077	TOP	2ND	H
00200000	00377777	0100	0177	TOP	2ND	J
00400000	00577777	0200	0277	TOP	2ND	K
00600000	00777777	0300	0377	TOP	2ND	L
01000000	01177777	0400	0477	TOP	2ND	H
01200000	01377777	0500	0577	TOP	2ND	J
01400000	01577777	0600	0677	TOP	2ND	K
01600000	01777777	0700	0777	TOP	2ND	L
02000000	02177777	1000	1077	3RD	4TH	H
02200000	02377777	1100	1177	3RD	4TH	J
02400000	02577777	1200	1277	3RD	4TH	K
02600000	02777777	1300	1377	3RD	4TH	L

TABLE 6-29: 512KB INTERLEAVED DECODE (12256-E7) (Cont.)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
03000000	03177777	1400	1477	3RD	4TH	H
03200000	03377777	1500	1577	3RD	4TH	J
03400000	03577777	1600	1677	3RD	4TH	K
03600000	03777777	1700	1777	3RD	4TH	L
04000000	04177777	2000	2077	5TH	6TH	H
04200000	04377777	2100	2177	5TH	6TH	J
04400000	04577777	2200	2277	5TH	6TH	K
04600000	04777777	2300	2377	5TH	6TH	L
05000000	05177777	2400	2477	5TH	6TH	H
05200000	05377777	2500	2577	5TH	6TH	J
05400000	05577777	2600	2677	5TH	6TH	K
05600000	05777777	2700	2777	5TH	6TH	L
06000000	06177777	3000	3077	7TH	8TH	H
06200000	06377777	3100	3177	7TH	8TH	J
06400000	06577777	3200	3277	7TH	8TH	K
06600000	06777777	3300	3377	7TH	8TH	L
07000000	07177777	3400	3477	7TH	8TH	H
07200000	07377777	3500	3577	7TH	8TH	J
07400000	07577777	3600	3677	7TH	8TH	K
07600000	07777777	3700	3777	7TH	8TH	L

TABLE 6-30: 1024KB INTERLEAVED DECODE (12512-E8) (7615-902)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
00000000	00177777	0000	0077	TOP	2ND	H
00200000	00377777	0100	0177	TOP	2ND	J
00400000	00577777	0200	0277	TOP	2ND	K
00600000	00777777	0300	0377	TOP	2ND	L
01000000	01177777	0400	0477	TOP	2ND	M
01200000	01377777	0500	0577	TOP	2ND	N
01400000	01577777	0600	0677	TOP	2ND	P
01600000	01777777	0700	0777	TOP	2ND	R
02000000	02177777	1000	1077	TOP	2ND	H
02200000	02377777	1100	1177	TOP	2ND	J
02400000	02577777	1200	1277	TOP	2ND	K
02600000	02777777	1300	1377	TOP	2ND	L
03000000	03177777	1400	1477	TOP	2ND	M
03200000	03377777	1500	1577	TOP	2ND	N
03400000	03577777	1600	1677	TOP	2ND	P
03600000	03777777	1700	1777	TOP	2ND	R

TABLE 6-30: 1024KB INTERLEAVED DECODE (12512-E8) (7615-902) (Cont.)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
04000000	04177777	2000	2077	3RD	4TH	H
04200000	04377777	2100	2177	3RD	4TH	J
04400000	04577777	2200	2277	3RD	4TH	K
04600000	04777777	2300	2377	3RD	4TH	L
05000000	05177777	2400	2477	3RD	4TH	M
05200000	05377777	2500	2577	3RD	4TH	N
05400000	05577777	2600	2677	3RD	4TH	P
05600000	05777777	2700	2777	3RD	4TH	R
06000000	06177777	3000	3077	3RD	4TH	H
06200000	06377777	3100	3177	3RD	4TH	J
06400000	06577777	3200	3277	3RD	4TH	K
06600000	06777777	3300	3377	3RD	4TH	L
07000000	07177777	3400	3477	3RD	4TH	M
07200000	07377777	3500	3577	3RD	4TH	N
07400000	07577777	3600	3677	3RD	4TH	P
07600000	07777777	3700	3777	3RD	4TH	R
10000000	10177777	4000	4077	5TH	6TH	H
10200000	10377777	4100	4177	5TH	6TH	J
10400000	10577777	4200	4277	5TH	6TH	K
10600000	10777777	4300	4377	5TH	6TH	L
11000000	11177777	4400	4477	5TH	6TH	M
11200000	11377777	4500	4577	5TH	6TH	N
11400000	11577777	4600	4677	5TH	6TH	P
11600000	11777777	4700	4777	5TH	6TH	R
12000000	12177777	5000	5077	5TH	6TH	H
12200000	12377777	5100	5177	5TH	6TH	J
12400000	12577777	5200	5277	5TH	6TH	K
12600000	12777777	4700	4777	5TH	6TH	L
13000000	13177777	5400	5477	5TH	6TH	M
13200000	13377777	5500	5577	5TH	6TH	N
13400000	13577777	5600	5677	5TH	6TH	P
13600000	13777777	5700	5777	5TH	6TH	R
14000000	14177777	6000	6077	7TH	8TH	H
14200000	14377777	6100	6177	7TH	8TH	J
14400000	14577777	6200	6277	7TH	8TH	K
14600000	14777777	6300	6377	7TH	8TH	L
15000000	15177777	6400	6477	7TH	8TH	M
15200000	15377777	6500	6577	7TH	8TH	N
15400000	15577777	6600	6677	7TH	8TH	P
15600000	15777777	6700	6777	7TH	8TH	R
16000000	16177777	7000	7077	7TH	8TH	H
16200000	16377777	7100	7177	7TH	8TH	J
16400000	16577777	7200	7277	7TH	8TH	K
16600000	16777777	7300	7377	7TH	8TH	L

TABLE 6-30: 1024KB INTERLEAVED DECODE (12512-E8) (7615-902) (Cont.)

ADDRESS: FROM	TO	PPN: FROM	TO	BOARD: BIT 24 =0	=1	ROW:
17000000	17177777	7400	7477	7TH	8TH	M
17200000	17377777	7500	7577	7TH	8TH	N
17400000	17577777	7600	7677	7TH	8TH	P
17600000	17777777	7700	7777	7TH	8TH	R

6.2.6.4 LOGREC Missing Memory Errors

When a missing memory module check occurs and the operating system finds an error, the following format appears on the system console:

```
MISSING MEMORY, DSWSTAT = xx DSWRMA = xx
DSWPB = xx DSWPARITY =xx
```

The information reported is the same as for a machine check except that the machine check code does not appear and DSWPARITY is not decoded.

6.3 1045/1051 POWER SUPPLY MEASUREMENTS AND ADJUSTMENTS

To check the 1045/1051 voltages on the system, turn the system on and check that all voltages are present and within specification on the correct pins (see Tables 6-31, 6-32, and 6-33). The +5 volts is the only adjustment that can be made in the field (see Figure 6-14). Set this to +5.1 volts using a digital voltmeter. Any voltages missing or off specification require that the supply be replaced. If HPWRFL+, HSYCLR+ or PS60CY+ are missing, replace the unit.

TABLE 6-31: 1045/1051 POWER SUPPLY TEST POINTS

SIGNAL	BACKPLANE PIN NOS.
+5VDC	CA-01, CA-02, CA-49 CA-50, CB1-01, CB1-02
HPWRFL+	CB1-25
HSYSCLR+	CB1-41
PS60CY+	CA1-54*
+12VDC	CB1-90, CB1-91
-12VDC	CB1-76, CB1-77
+16.2VDC	CB1-97, CB1-98

*Use an oscilloscope.

TABLE 6-32: POWER SUPPLY RIPPLE

VOLTAGE	RIPPLE
+ 5.0VDC	100mV peak to peak (20KHz)
+12.0VDC	50mV peak to peak (60KHz)
-12.0VDC	50mV peak to peak (60KHz)
+16.2VDC	50mV peak to peak (60KHz)

TABLE 6-33: POWER SUPPLY OVER/UNDER VOLTAGE SPECIFICATIONS

VOLTAGE	UNDERVOLTAGE	OVERVOLTAGE
+ 5.0V	4.6 ±0.1V	6.3 ±0.2V
+12.0V	10.0 ±1.0V	15.0 ±0.5V
-12.0V	-10.0 ±1.0V	-15.0 ±0.5V
+16.2V	13.6 ±1.0V	20.2 ±0.5V

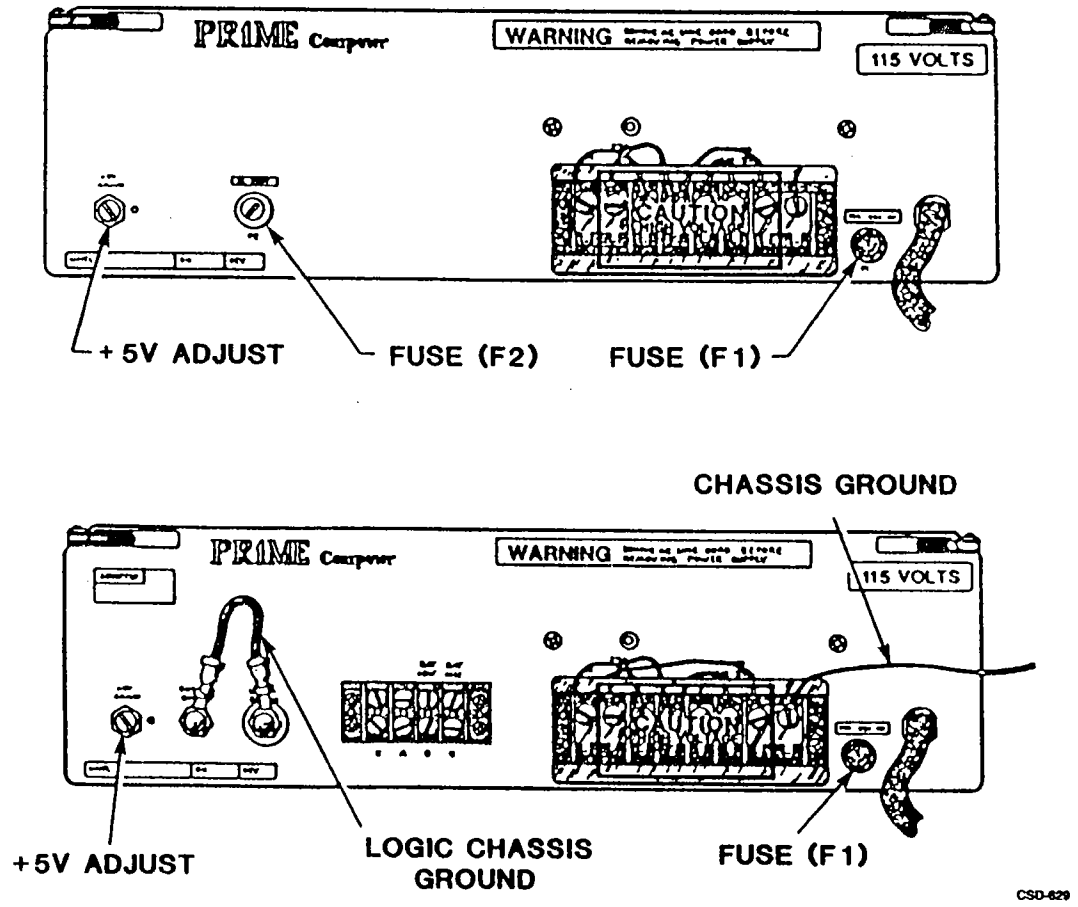

FIGURE 6-14: POWER SUPPLY ADJUSTMENT

To measure and adjust the 1045/1051 power supply voltages, proceed as follows:

1. Power down the system.

2. Open the front door and remove the backplane cover.

3. Connect a digital voltmeter between chassis/logic GND and the dc voltage to be checked at the slot farthest from the power supply (use oscilloscope to check ripple).

CAUTION

Be very careful when connecting the voltmeter leads to the backplane pins. These pins are very close together and it is extremely easy to short the voltage pin to an adjacent signal pin causing damage to many of the PCBs in the system.

4. Apply power to the system and check the voltmeter for the proper voltage reading according to Tables 6-32 and 6-33.

5. If a voltage is out of specification, take the following action:

   A) The +5 volts (VCC1 and VCC2) is adjustable. Reference Figure 6-14 for the location of the adjusting screw. Loosen the locknut and adjust the +5VDC to proper specification. Retighten the locknut and recheck the voltage for proper specification. If the +5VDC cannot be adjusted to specification go to step 6.
   B) If any other voltage is out of specification (+12V, -12V, or +16.2V), go to step 6.

6. For any voltage that is not within specification per Tables 6-32 and 6-33, take the following action:

   A) Power down the system.
   B) Unplug all PCBs, except two for a minimum load, from the backplane serviced by the power supply.
   C) Apply power to the system and check the faulty voltage. If it is now good, isolate the board that may have been loading it down and replace it.
   D) If the voltage is still faulty, power down and unplug the two remaining boards. Plug in two others, power-up and recheck the voltage. If the voltage is still faulty replace the power supply as outlined under the 1045/1051 Power Supply Replacement Procedure in this chapter.

CHAPTER 7
PARTS REMOVAL AND REPLACEMENT

7.1 FRU REMOVAL/REPLACEMENT PROCEDURES

The parts removal/replacement procedures for the 50 Series systems are presented in this chapter. These procedures consist of:

- PCB Removal/Replacement
- Memory Board RAM Removal/Replacement
- Non-FCC Cabinet FRU Removal/Replacement
- FCC Cabinet FRU Removal/Replacement

Table 7-1 lists the system FRUs.

7.1.1 PRINTED CIRCUIT BOARD (PCB) REMOVAL/REPLACEMENT

The 50 Series system PCBs located in the CPU/Memory, and I/O chassis are plugged horizontal into the appropriate backplane and are accessed from the rear of the cabinet.

CAUTION

The system must be powered down before removing or installing a PCB, otherwise the board will be damaged.

7.1.1.1 PCB Removal

To remove a PCB, proceed as follows (refer to Figure 7-1):

1. Power down the system.
2. Open the rear door of the cabinet.
3. From the rear of the cabinet, locate the PCB to be replaced and unplug any soft hats or cables.
4. Grasp the PCB ejector tabs on each side of the PCB. Pull the tabs toward you so that the PCB pops out of the backplane as shown in Figure 7-1.
5. Remove the PCB from the slot. When removing the PCB be sure not to scrape the PCB against adjacent PCBs.

7.1.1.2 PCB Replacement

To install a PCB refer to Figure 7-1 and proceed.

1. Ensure that the system is powered down.

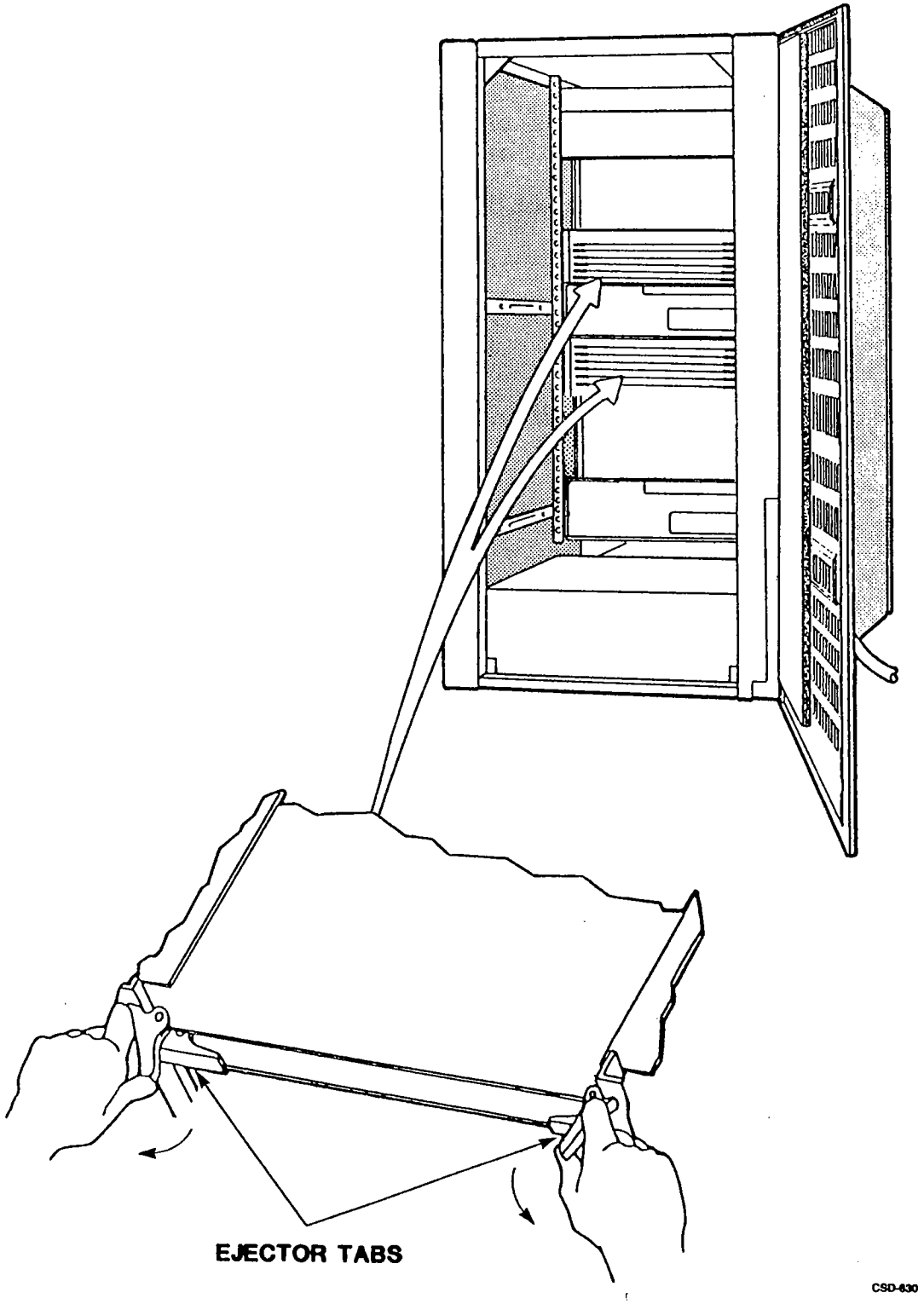

FIGURE 7-1: BOARD REMOVAL

2. Slide the PCB into its slot making sure that the board is in the proper rail on both sides of the chassis. Exercise care when inserting the PCB. Do not scrape the PCB against adjacent PCBs. Line up the PCB with the backplane connectors and make sure that the PCB is properly seated.

3. Grasp the ejector tabs on either side of the PCB. Push the tabs arms until the PCB is firmly set into the backplane.

4. Plug in any soft hats or cables that were removed.

NOTE

CPU PCBs require an extra push in order to seat them properly into the backplane.

CAUTION

To avoid damaging the PCB or the backplane connectors, be careful not to exert undue pressure. If the PCB does not insert easily, realign the PCB and try installing it again.

7.1.2 MEMORY BOARD RAM REMOVAL/REPLACEMENT

Metal oxide semiconductor RAMs are located on the E6, E7, E8 and E9 memory boards. The Field Service Grounding Kit, Prime number TEATTFSKIT, should be used when removing these RAMs. The kit consists of:

- Ground cord (15 feet)
- Work surface
- Wrist strap (5-foot cord)

To prevent static-build-up handle all static-sensitive components at a static-safe work area. Also be sure to transport all static-sensitive components in static-shielding containers or packages.

1. Complete the memory board removal procedures as outlined in this chapter.

2. Remove the RAMs by easing them out of the board using a standard screwdriver.

3. Reverse the two steps to replace the RAMs.

7.1.3 NON-FCC CABINET FRU REMOVAL/REPLACEMENT PROCEDURES

FRU removal/replacement procedures for non-FCC cabinets are presented in this subsection. These procedures consist of:

- PDU Removal/Replacement

- Cabinet Blower Removal/Replacement
- Power Supply Removal/Replacement
- 16-slot and 19-Slot Backplane Removal

7.1.3.1 PDU Removal/Replacement

The PDU is attached to the cabinet base assembly. To remove a PDU:

1. Power down the system and turn the PDU main ac breaker to off.
2. Unplug all power cords from the PDU ac duplexes and the ac input power cord. Disconnect all other connectors and the green chassis ground wire.
3. Remove the six screws attaching the PDU panel to the cabinet base assembly.
4. Start removing the panel from the base. Unplug the blower ac power cord from the ac outlet at the rear of the panel to allow complete removal of the panel.
5. To replace the PDU, reverse steps one through four above.

7.1.3.2 Cabinet Blower Removal/Replacement

The cabinet blower is attached to the right top cover plate of the cabinet base assembly. To remove the cabinet blower:

1. Power down the system and turn off the main ac breaker on the PDU.
2. Disconnect the main ac input power cord to the cabinet.
3. Remove the 12 screws holding the left top cover plate to the cabinet base assembly and remove the plate. The right top plate has the blower assembly attached to it.
4. Remove the remaining four screws that hold the right top cover plate and blower assembly on the base assembly.
5. Unplug the blower ac power cord from the connector on the rear of the PDU panel.
6. Remove the blower assembly and right cover plate from the base assembly.
7. Replace the blower assembly by reversing steps one through six above.

7.1.3.3 Power Supply Removal/Replacement

There can be up to three power supplies in a cabinet and they must be located in slots 0, 00 or 000. This is the lower slot in each backplane. To remove a power supply:

1. Power down the system and turn off the main ac breaker on the PDU.

2. Unplug the ac cable of the failing power supply from the PDU.

3. Grasp the extractor arms of the power supply and pull them toward the rear of the cabinet.

4. Remove the power supply from the cabinet.

5. To replace the power supply, reverse steps 1 through 4 above.

7.1.3.4 16-Slot and 19-Slot Backplane Removal/Replacement

To remove a 16-slot or 19-slot backplane, proceed as follows:

1. Power down the system and unplug the cabinet from the main power source.

2. Open the rear door and unseat all the PCBs and the power supply plugged into the backplane to be replaced.

3. Open the front door of the cabinet and remove the cover of the backplane to be replaced.

4. Using a Phillips screw driver, remove the screws that hold the backplane to the cardcage.

5. Remove the backplane.

6. To replace the backplane reverse steps 1 throuch 5 above.

7.1.4 FCC CABINET FRU REMOVAL/REPLACEMENT PROCEDURE

FRU removal/replacement procedures for FCC cabinets are presented in this subsection. These procedures consist of:

- Blower Front Air Filter Removal/Replacement
- Blower Bottom Air Filter Removal/Replacement
- Cabinet Blower Removal/Replacement
- Blower Belt Removal/Replacement
- Blower Vane Switch Removal/Replacement
- Power Supply Removal/Replacement
- PDU Removal/Replacement
- 16-Slot and 19-Slot Backplane Removal/Replacement

7.1.4.1 Blower Front Air Filter Removal/Replacement

Each blower has a front and a bottom filter. To remove the front filter:

1. Power down the system.

2. Disconnect the main ac input power cord to the system.

3. Open the front door to the cabinet.

4. Locate and remove the silver Velcro-lined front filter from the bottom of the cabinet by pulling on the plastic tab as shown in Figure 7-2.

5. To replace the front filter, reverse steps 1 through 4 above.

7.1.4.2 Blower Bottom Air Filter Replacement

The blower bottom filter is located underneath the blower. To remove the bottom filter:

1. Open the cabinet rear door and locate the bottom filter as shown in Figure 7-3.

2. Remove the filter by sliding it to the right.

3. To replace the filter, reverse steps 1 through 3 above.

7.1.4.3 Cabinet Blower Assembly Removal/Replacement

The cabinet blower is removed and replaced as follows:

1. Complete steps 1 through 4 of the front filter removal procedure.

2. Go to the rear of the cabinet and open the rear door.

3. Locate and disconnect the two plugs from the left side of the blower as shown in Figure 7-2.

4. Using a Phillips screwdriver, locate and loosen the screw from the right rear of the blower as shown in Figure 7-3.

5. Return to the front of the cabinet.

6. Locate and remove the two front blower screws shown in Figure 7-3 using a Phillips screwdriver.

7. Reach into the rear right corner of the blower. Locate and loosen the knurled nut shown in Figure 7-3.

8. Facing the front of the cabinet, slide the blower to the right and pull the whole assembly straight towards you, until the blower has cleared the cabinet.

9. To replace the blower, reverse the above eight steps.

7.1.4.4 Blower Belt Removal/Replacement

Each blower has three blower belts. To remove the cabinet blower belts:

1. Complete steps 1 through 4 of the blower front filter removal procedure outlined above.

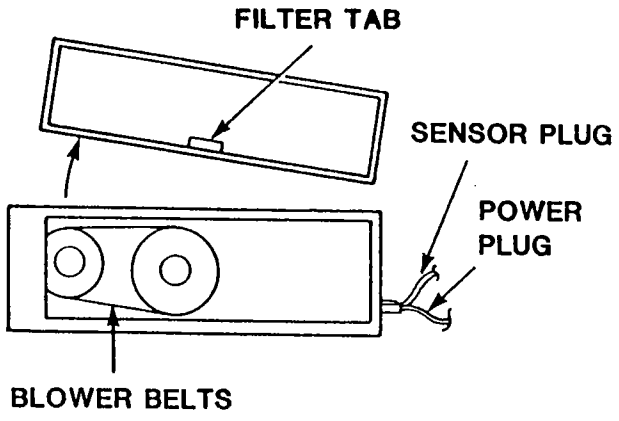

FIGURE 7-2: FCC CABINET FRONT FILTER AND BELT REMOVAL

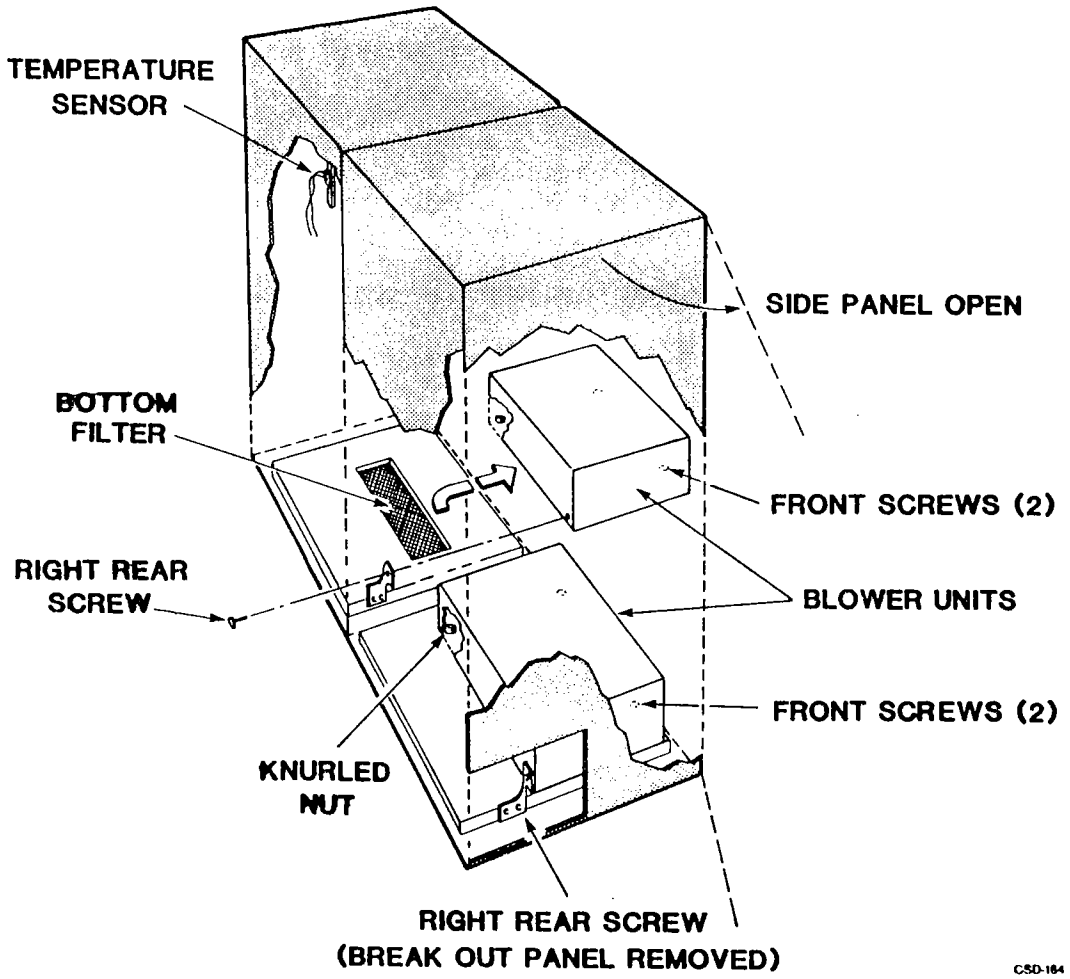

FIGURE 7-3: FCC CABINET BLOWER UNIT REMOVAL

2. Locate and remove the blower belt as shown in Figure 7-2.

3. To replace the belt, slip the new belt over the blower and into the proper groove as shown in Figure 7-2 and reverse steps 1 through 4 of the blower front filter removal procedure.

7.1.4.5 Blower Vane Switch Removal/Replacement

A vane switch located in the blower measures the amount of air circulation available in the cabinet. To remove and replace the vane switch:

1. Remove the cabinet blower as outlined in steps 1 through 7 of the blower assembly removal procedure above.

2. Locate and remove the two allen screws and nuts holding the vane switch to the blower as shown in Figure 7-4.

3. Label the two vane switch wires and pull the vane switch from the wire.

4. Replace the vane switch by reversing steps 1 through 3 above.

7.1.4.6 Power Supply Removal/Replacement

There can be up to three power supplies in a cabinet and they must be located in slots 0, 00 or 000. This is the lower slot in each backplane. To remove a power supply:

1. Power down the system and turn off the main ac breaker on the PDU.

2. Unplug the ac cable of the failing power supply from the PDU.

3. Grasp the extractor arms of the power supply and pull them toward the rear of the cabinet.

4. Remove the power supply from the cabinet.

5. To replace the power supply, reverse steps 1 through 4 above.

7.1.4.7 Power Distribution Unit (PDU) Removal/Replacement

To remove and replace the PDU:

1. Power down the system.

2. Unplug the system from its power source.

CAUTION

Power is still active to the system if the system is not unplugged from the power source.

3. Label and unplug all connections to the PDU.

4. Locate and remove the two screws from the left top of the PDU as shown in Figure 7-5 using a Phillips screwdriver.

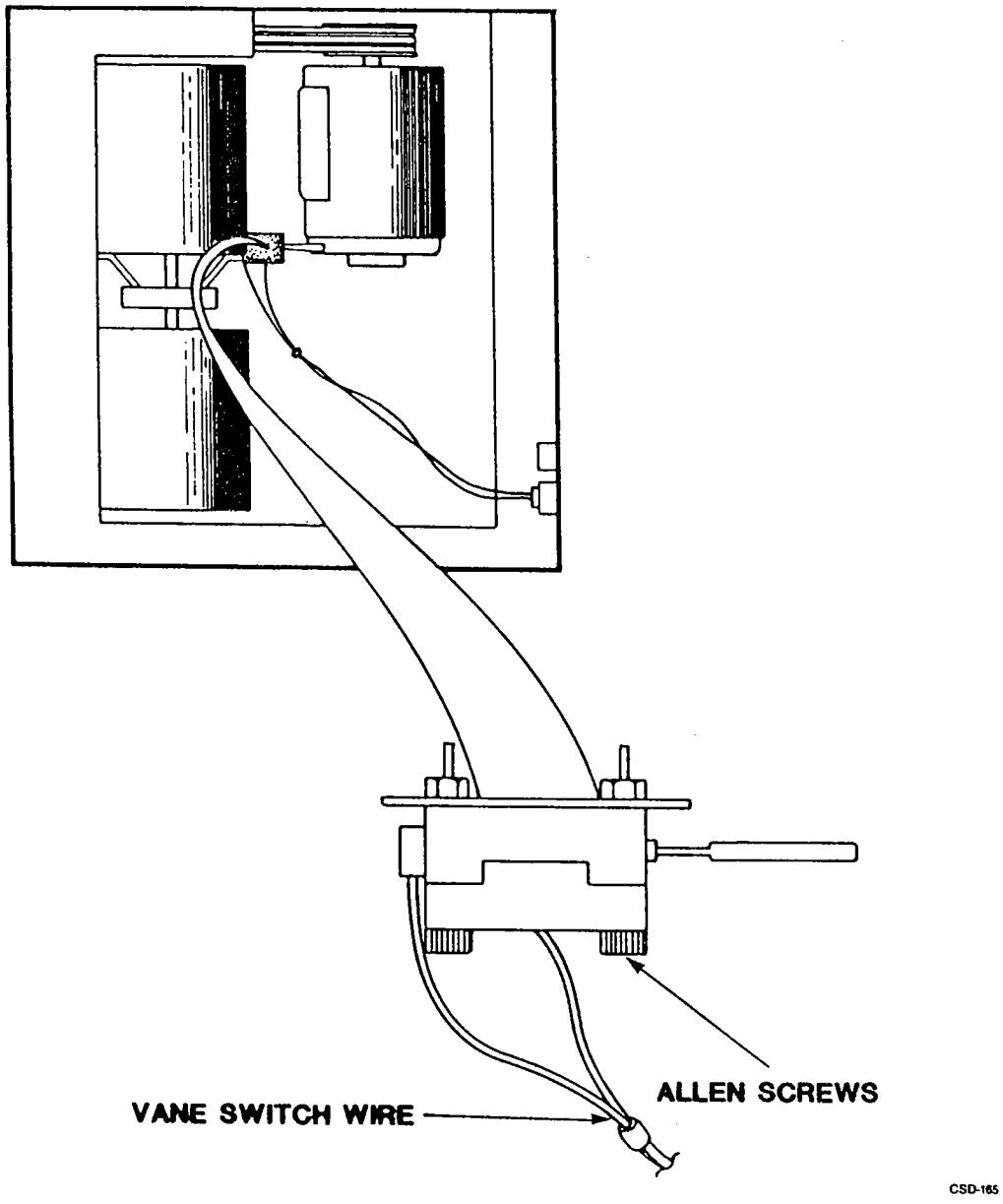

FIGURE 7-4: FCC CABINET VANE SWITCH REMOVAL

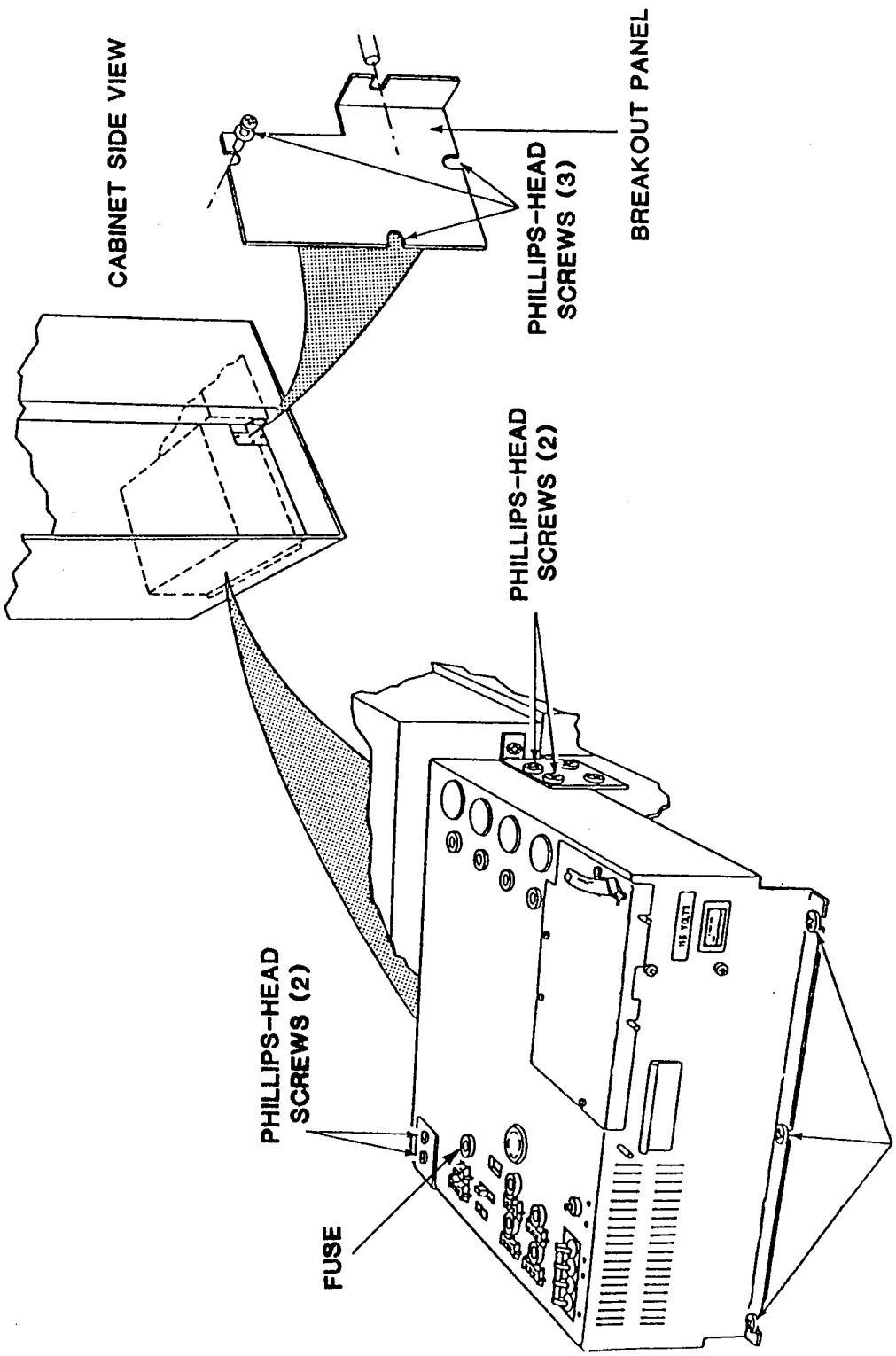

FIGURE 7-5: FCC CABINET PDU REPLACEMENT

5. Using a Phillips screwdriver, remove the front three screws.

6. Go to the side of the cabinet and open the side door.

7. Locate the breakout panel in the bulkhead as shown in Figure 7-5.

8. Using a Phillips screwdriver remove the breakout panel.

9. Reach through the bulkhead door and remove the two remaining screws from the PDU as shown in Figure 7-5.

10. Return to the rear of the cabinet and pull the PDU towards the rear until it has cleared the system.

11. To replace the PDU reverse steps 1 through 10 above.

7.1.4.8 16-slot and 19-Slot Backplane Removal/Replacement

To remove a 16-slot or 19-slot backplane, refer to Figure 7-6 and proceed as follows:

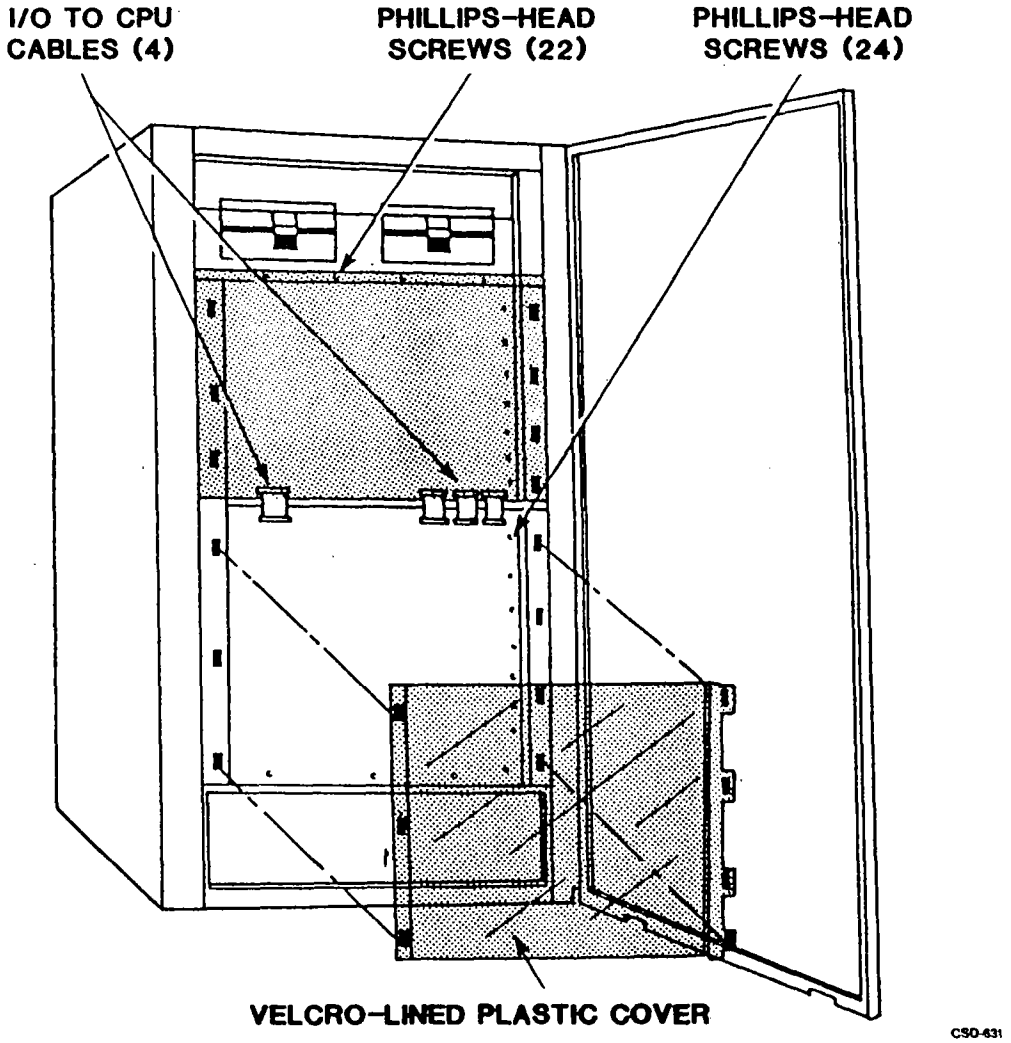

FIGURE 7-6: FCC CABINET BACKPLANES

1. Power down the system and unplug the cabinet from the main power source.

2. Open the rear door and unseat all the PCBs and the 1051 power supply plugged into the backplane to be replaced.

3. Open the front door of the cabinet and remove the Velcro-lined cover of the backplane to be replaced.

4. Using a Phillips screw driver, remove the screws that hold the backplane to the cardcage.

5. Remove the backplane.

6. To replace the backplane reverse steps 1 through 5 above.

7.2 50 SERIES FRUS

Table 7-1 lists all the 50 series FRUs.

TABLE 7-1: 50 SERIES FRUS

DESCRIPTION	FRU NUMBER
CPUs	
P850 SSU Board	2029-901
P450-II B Board	2210-902
P400 A Board	2241-902
P400 B Board	2242-902
P350 A Board	2243-901
P350 B Board	2245-901
P450 A Board	2246-901
P150/250-II A Board	2247-901
P150/250-II B Board	2248-901
P500 A Board	2251-901
P500 B Board	2252-901
P500,550-II XIS Board	2253-902
P750 A Board	2259-902
P750 C Board	2262-902
P750 CS Board	2263-902
P750 XIS Board	2264-901
P750 J Board	2268-901
P850 J Board	2273-901
P850 C Board	2274-901
P850 CS Board	2275-901
P550-II A Board	2278-901
P550-II B Board	2279-901
P850 A Board	2285-901
P850 XIS Board	2286-901
B Board Replacement For 150/250-II, 450, 550	2287-901
B Board Replacement For P350	2290-901
B Board Replacement For P400	2291-901
P450-II A Board	2292-901

TABLE 7-1: 50 SERIES FRUS (Cont.)

DESCRIPTION	FRU NUMBER
CPUs	
P250-II Top Hat W/FEP	ESA2495-902
P550-II Top Hat W/FEP	ESA2495-903
P750/850 Top Hat W/O FEP	ESA2495-905
P750/850 Top Hat W/FEP	ESA2495-906
P250-II Top Hat W/O FEP	ESA2495-908
P550-II Top Hat W/O FEP	ESA2495-909
MEMORIES	
Memory, 256Kb With ECC	12128-E4
Memory, 256Kb ECC Board Wide Word	12128-E6
Memory, 512Kb ECC Board Wide Word	12256-E7
Memory, 64Kb WITH Byte Parity	1232-D85
Memory, 1024Kb ECC Board Wide Word	12512-E8
Memory, 1024Kb ECC Board Wide Word(E9)	7615-902
CONTROLLERS	
Control Panel With PROM (Pre-50 Series)	1032-901
P750 Memory Extender, Main Board	2021-902
P750 Memory Extender, Extender Board	2022-902
Magtape Controller, Burst Mode	2023-901
Interprocessor Communicator (Obsolete)	2028-901
Mag Tape Controller 45/75 IPS Formatter, PE Only	2081-901
Mag Tape Controller 45/75 IPS Formattter, PE/NRZI	2081-902
Memory Extender, Main Board	2082-901
Memory Extender, Extender Board Assy.	2083-901
Primenet Node Controller	2257-902
(Junction Box)	ESA3174-901
VCP PCB Assembly	2265-902
Mag Tape Formatter	2269-901
DDF MPC	2270-901
Mag Tape Integrated Formatter Assy.	2271-901
SOC RTC/AL/PTRP/DMA/PIC	3006-901
SOC SCL Option	3006-902
SOC WDT Option	3006-903
SOC SCL/WDT OptionS	3006-904
SOC BPIOC	3007-901
SOC BPIOC W/SLC Option	3007-902
SOC BPIOC W/WDT Option	3007-903
SOC BPIOC W/2ND BPIOC	3007-904
SOC BPIOC W/SLC & WDT	3007-905
SOC BPIOC W/SLC & 2nd BPIOC	3007-906
SOC BPIOC W/WDT & 2nd BPIOC	3007-907
SOC BPIOC W/SLC & WDT & 2nd BPIOC	3007-908
SOC Gould Controller	3008-902
SOC Versatec Controller	3009-902
URC, 1 CR/2 LP (UP TO 600 LPM)	3156-901
URC 1 CR/P, 1 CR/P And 1 LP (UP TO 600 LPM)	3156-902
URC, 1 CR And 1 LP (UP TO 1200 LPM)	3156-903
URC, 1 CR/P And 1 LP (UP TO 1200 LPM)	3156-904
URC3 Controller, 1 Card Processor	3156-905

TABLE 7-1: 50 SERIES FRUS (Cont.)

DESCRIPTION	FRU NUMBER
CONTROLLERS	
OPT B' MHD Disk Controller	4002-901
Universal Disk Controller	4003-902
CMD/SMD/MMD Controller, 1 Device (Round Cable)	4004-941
CMD/SMD/MMD Controller, 2 Devices	4004-942
CMD/SMD/MMD Controller, 3 Devices	4004-943
CMD/SMD/MMD Controller, 4 Devices	4004-944
Burst Mode Controller, 1 Device (Flat Cable)	4005-901
Burst Mode Controller, 2 Devices	4005-902
Burst Mode Controller, 3 Devices	4005-903
Burst Mode Controller, 4 Devices	4005-904
Dual Port Kit 80Mb	4008-901
Dual Port Kit 300Mb	4009-901
Mag Tape Controller, NRZI Only	4020-902
Mag Tape Controller, 75IPS, NRZI	4021-901
Diskette Controller	4030-902
Diskette Controller W/Formatter	4031-901
AMLC 8 Line, RS232C, FDSC	5002-901
AMLC 16 Line, RS232C, FDSC	5004-901
AMLC 8 Line, RS232C, LDSC	5052-902
AMLC 16 Line, RS232C, LDSC	5054-902
AMLC 8 Line, Current Loop	5072-901
AMLC 8 Line, 20MA	5072-912
AMLC 16 Line, Current Loop	5074-902
AMLC 16 Line, 20MA	5074-912
AMLC 8 Line, DCD	5075-902
AMLC 8-EIA, 8-20MA	5075-912
QAMLC 16 Line, RS232C, FDSC	5104-901
QAMLC 8 Line, RS232C, LDSC	5152-901
QAMLC 16 Line, RS232C LDSC	5154-901
QAMLC 8 Line, 20MA	5172-901
QAMLC 16 Line, 20MA	5174-901
AMLC 16 Line 8-EIA, 8-20MA	5175-901
HSSMLC, RS232C	5302-901
HSSMLC, RS232C 2 Line Expansion	5304-901
HSSMLC, 303 Modem	5312-901
HSSMLC, 303 Modem 2 Line Expansion	5314-901
HSSMLC, DSU Modem	5322-901
HSSMLC, 303 Modem 2 Line Expansion	5324-901
HSSMLC, Bisync. Procedures	5346-901
HSSMLC, Packet Protocol	5347-901
HSSMLC, UT200	5350-901
HSSMLC, UT200 ICL7020	5351-901
Options 5324/46/47/50 &51 Also Apply To Types 5302 & 5312	
MACI, 4 Lines	5402-001
MACI, 6 Lines	5403-001
MACI, 8 Lines	5404-001
MDLC, 2 EIA Modems	5602-902
MDLC, 2 Line Exp. For 5602	5604-902

TABLE 7-1: 50 SERIES FRUS (Cont.)

DESCRIPTION	FRU NUMBER
CONTROLLERS	
MDLC, W/2 EIA Bysync And HDLC/X.25	5602-903
MDLC, W/2 EIA Bysync And Packet	5602-904
MDLC, W/2 EIA Bysync And UT200/UNIVAC1004/ICL7020	5602-905
MDLC, W/2 EIA HDLC/X.25, UT200/UNIVAC1004/ICL7020	5602-906
MDLC, W/2 EIA Packet, UT20/UNI1004/ICL7020	5602-907
MDLC, W/2 EIA Packet And HDLC/X.25	5602-908
MDLC, W/4 EIA	5602-910
MDLC, W/4 EIA, Bysync And HDLC/X.25	5602-913
MDLC, W/2 EIA And 2 DSU	5602-920
MDLC, 2 Line DSU	5622-902
MDLC, 2 Line EXP. FOR 5622	5624-902
MDLC, W/2 DSU Bysync And HDLC/X.25	5622-903
MDLC, W/2 DSU Bysync And Packet	5622-904
MDLC, W/2 DSU Bysync, UT200/UNIVAC1004/ICL7020	5622-905
MDLC, W/2 DSU HDLC/X.25, UT200/UNI1004/ICL7020	5622-906
MDLC, W/2 DSU Packet, UT200/UNI1004/ICL7020	5622-907
MDLC, W/2 DSU Packet And HDLC	5622-908
MDLC, W/2 DSU And 2 EIA	5622-910
MDLC, W/4 DSU	5622-920
MDLC, W/4 DSU Bysync And HDLC/X.25	5622-923
AIS, 16 Channels	6000-901
AIS, Additional 16 Channels	6001-001
PRIMAD, HS AIS	6005-901
AIS, Current/Voltage Signal Cond.	6013-001
SDO, Photo Isolated Outputs	6040-002
SDO, TTL Outputs	6041-002
SDO, SIG. CON. Photo ISL. Outputs	6042-001
SDO, SIG. CON. Photo ISL. Outputs	6043-001
AOS(DAC) 2 Channel	6060-001
Interprocessor Communicator (IPC)	7030-901
Interprocessor Communicator Expander	7031-901
POWER SUPPLIES	
Diskette Power Supply 60Hz	1024-001
Fuse 5.0A 250V Slo-Blo	FUS0224-030
Diskette Power Supply 50Hz	1024-002
Fuse 2.5A 250V Slo-Blo	FUS0224-025
Power Supply 120AMP 60Hz	1045-901
Fuse 3.0A 250V Slo-Blo	FUS0224-027
Fuse 15A 250V Slo-Blo	FUS0224-035
Power Supply 120A 50Hz	1045-A-901
Fuse 1.5A 250V Slo-Blo	FUS0224-022
Fuse 10A 250V Slo-Blo	FUS0224-034
Power Supply 120A 60Hz W/Surge Limiter	1051-901
Fuse 3.0A 250V Slo-Blo	FUS0224-027
Fuse 15A 250V Slo-Blo	FUS0224-035
Power Supply 120A 50Hz W/Surge Limiter	1051-902
Fuse 2.0A 250V Slo-Blo	FUS6215-007
Fuse 10A 250V Slo-Blo	FUS6215-012

TABLE 7-1: 50 SERIES FRUS (Cont.)

DESCRIPTION	FRU NUMBER
NON-FCC CABINET PDUS	
PDU Mainframe 115/208V	ESA3962-901
Fuse 1.0A 250V Slo-Blo	FUS0224-019
Fuse 15A 250V Norm-Blo	FUS0224-037
PDU Mainframe/Peripheral 230V	ESA3962-902
Fuse 1.0A 250V Slo-Blo	FUS0224-019
Fuse 15A 250V Norm-BLO	FUS0224-037
PDU Peripheral 115V	ESA3963-901
Fuse 15A 250V Norm-BLO	FUS0224-037
PDU 850 I/O 115V	ESA4161-901
Fuse 1.0A 250V Slo-Blo	FUS0224-019
Fuse 15A 250V Norm-BLO	FUS0224-037
PDU 850 I/O 230V	ESA4162-901
Fuse 1.0A 250V Slo-Blo	FUS0224-019
Fuse 15A 250V Norm-Blo	FUS0224-037
PDU Four (4) Channel 115V	ESA4647-901
Fuse 1.0A 250V Slo-Blo	FUS0224-019
Fuse 15A 250V Norm-Blo	FUS0224-037
FCC CABINET PDUS	
PDU Four (4) Channel 60Hz	ESA6401-901
Fuse 0.5A 250V Slo-Blo	FUS0224-014
PDU Four (4) Channel 50 Hz	ESA6215-004
Fuse .25A 250V Slo-Blo	FUS6215-004
MISCELLANEOUS	
16-Slot Backplane	MEC4166-001
19-Slot Backplane	MEC4167-001
Status Panel PCB	ESA6442-001
Blower 60Hz	MEC2649-001
Blower 50Hz	BWR6663-901
Blower 60Hz	BWR6663-902
Blower Belt (set of three)	MEC6529-001
Vane Switch	MEC6513-001
Air Filter, Front, Inside	MEC2684-001
Air Filter, Front	MEC2684-002
Air Filter, Bottom	MEC5579-902
Cover Backplane 16 Slot	MEC6502-001
Cover Backplane 19 Slot	MEC6503-001
Level Leg Non-skid	MEC6695-001
Air Baffle Board (I/O Chassis)	MEC7584-001
Power Supply Filler Assembly	MSA7938-001
16-slot Chassis Assembly (750)	MSA4537-901
16-slot Chassis Assembly (850)	MSA4537-902
19-slot Chassis Assembly (750)	MSA4396-901
19-slot Chassis Assembly Main Bay (850)	MSA4396-902
19-slot Chassis Assembly I/O Bay (850)	MSA4396-903

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PRIME

Field Engineering

FEB 251
Rev 1
Date 11/22/82

BULLETIN

450's use E4's (4116's)

Decode Chart for 1232, E4, E6, E7 and E8 Memories

The attached charts are corrected versions of those found in FESM #70

1. Table G - 3, page G-12 and G-13

2. Tables 6-4B, 6-4D, 6-4F, 6-4H
   pages 6-31 through 6-36

Thanks to Graham Lovell, Bryan Shugrue and Mike Morris of Prime U.K. for the above information.

TABLE G-3: 64KB NON-INTERLEAVED MEMORY (1232)

PPN FROM	PPN TO	BOARD SLOT	ROW
0	7	TOP	E
10	17	TOP	F
20	27	TOP	G
30	37	TOP	H
40	47	TOP	J
50	57	TOP	K
60	67	TOP	L
70	77	TOP	M
100	107	2ND	E
110	117	2ND	F
120	127	2ND	G
130	137	2ND	H
140	147	2ND	J
150	157	2ND	K
160	167	2ND	L
170	177	2ND	M
200	207	3RD	E
210	217	3RD	F
220	227	3RD	G
230	237	3RD	H
240	247	3RD	J
250	257	3RD	K
260	267	3RD	L
270	277	3RD	M
300	307	4TH	E
310	317	4TH	F
320	327	4TH	G
330	337	4TH	H
340	347	4TH	J
350	357	4TH	K
360	367	4TH	L
370	377	4TH	M
400	407	5TH	E
410	417	5TH	F
420	427	5TH	G
430	437	5TH	H
440	447	5TH	J
450	457	5TH	K
460	467	5TH	L
470	477	5TH	M

TABLE G-3: 64KB NON-INTERLEAVED MEMORY (Cont.)

500	507	6TH	E
510	517	6TH	F
520	527	6TH	G
530	537	6TH	H
540	547	6TH	J
550	557	6TH	K
560	567	6TH	L
570	577	6TH	M
600	607	7TH	E
610	617	7TH	F
620	627	7TH	G
630	637	7TH	H
640	647	7TH	J
650	657	7TH	K
660	667	7TH	L
670	677	7TH	M
700	707	8TH	E
710	717	8TH	F
720	727	8TH	G
730	737	8TH	H
740	747	8TH	J
750	757	8TH	K
760	767	8TH	L
770	777	8TH	M

TABLE 6-4B: 256KB INTERLEAVED DECODE (12128-E4)
Use 4116's

ADDRESS FROM	ADDRESS TO	PPN FROM	PPN TO	SLOT DSWSTAT BIT 24=0	SLOT DSWSTAT BIT =1	ROW
00000000	00037,777	0000	0017	TOP	2ND	G or 0
00040,000	00077,777	0020	0037	TOP	2ND	H or 1
00100,000	00137,777	0040	0057	TOP	2ND	J or 2
00140,000	00177,777	0060	0077	TOP	2ND	K or 3
00200,000	00237,777	0100	0117	TOP	2ND	L or 4
00240,000	00277,777	0120	0137	TOP	2ND	M
00300,000	00337,777	0140	0157	TOP	2ND	N
00340,000	00377,777	0160	0177	TOP	2ND	P
00400,000	00437,777	0200	0217	TOP	2ND	G
00440,000	00477,777	0220	0237	TOP	2ND	H
00500,000	00537,777	0240	0257	TOP	2ND	J
00540,000	00577,777	0260	0277	TOP	2ND	K
00600,000	00637,777	0300	0317	TOP	2ND	L
00640,000	00677,777	0320	0337	TOP	2ND	M
00700,000	00737,777	0340	0357	TOP	2ND	N
00740,000	00777,777	0360	0377	TOP	2ND	P

TABLE 6-4B: 256KB INTERLEAVED DECODE (12128-E4) (Cont.)

01000000	01037777	0400	0417	3RD	4TH	G
01040000	01077777	0420	0437	3RD	4TH	H
01100000	01137777	0440	0457	3RD	4TH	J
01140000	01177777	0460	0477	3RD	4TH	K
01200000	01237777	0500	0517	3RD	4TH	L
01240000	01277777	0520	0537	3RD	4TH	M
01300000	01337777	0540	0557	3RD	4TH	N
01340000	01377777	0560	0577	3RD	4TH	P
01400000	01437777	0600	0617	3RD	4TH	G
01440000	01477777	0620	0637	3RD	4TH	H
01500000	01537777	0640	0657	3RD	4TH	J
01540000	01577777	0660	0677	3RD	4TH	K
01600000	01637777	0700	0717	3RD	4TH	L
01640000	01677777	0720	0737	3RD	4TH	M
01700000	01737777	0740	0757	3RD	4TH	N
01740000	01777777	0760	0777	3RD	4TH	P
02000000	02037777	1000	1017	5TH	6TH	G
02040000	02077777	1020	1037	5TH	6TH	H
02100000	02137777	1040	1057	5TH	6TH	J
02140000	02177777	1060	1077	5TH	6TH	K
02200000	02237777	1100	1117	5TH	6TH	L
02240000	02277777	1120	1137	5TH	6TH	M
02300000	02337777	1140	1157	5TH	6TH	N
02340000	02377777	1160	1177	5TH	6TH	P
02400000	02437777	1200	1217	5TH	6TH	G
02440000	02477777	1220	1237	5TH	6TH	H
02500000	02537777	1240	1257	5TH	6TH	J
02540000	02577777	1260	1277	5TH	6TH	K
02600000	02637777	1300	1317	5TH	6TH	L
02640000	02677777	1320	1337	5TH	6TH	M
02700000	02737777	1340	1357	5TH	6TH	N
02740000	02777777	1360	1377	5TH	6TH	P
03000000	03037777	1400	1417	7TH	8TH	G
03040000	03077777	1420	1437	7TH	8TH	H
03100000	03137777	1440	1457	7TH	8TH	J
03140000	03177777	1460	1477	7TH	8TH	K
03200000	03237777	1500	1517	7TH	8TH	L
03240000	03277777	1520	1537	7TH	8TH	M
03300000	03337777	1540	1557	7TH	8TH	N
03340000	03377777	1560	1577	7TH	8TH	P
03400000	03437777	1600	1617	7TH	8TH	G
03440000	03477777	1620	1637	7TH	8TH	H
03500000	03537777	1640	1657	7TH	8TH	J
03540000	03577777	1660	1677	7TH	8TH	K
03600000	03637777	1700	1717	7TH	8TH	L
03640000	03677777	1720	1737	7TH	8TH	M
03700000	03737777	1740	1757	7TH	8TH	N
03740000	03777777	1760	1777	7TH	8TH	P

TABLE 6-4D: 256KB INTERLEAVED DECODE (12128-E6)

ADDRESS FROM	ADDRESS TO	PPN FROM	PPN TO	SLOT DSWSTAT BIT 24=0	SLOT DSWSTAT BIT =1	ROW
00000000	00037777	0000	0017	TOP	2ND	H
00040000	00077777	0020	0037	TOP	2ND	J
00100000	00137777	0040	0057	TOP	2ND	K
00140000	00177777	0060	0077	TOP	2ND	L
00200000	00237777	0100	0117	TOP	2ND	M
00240000	00277777	0120	0137	TOP	2ND	N
00300000	00337777	0140	0157	TOP	2ND	P
00340000	00377777	0160	0177	TOP	2ND	R
00400000	00437777	0200	0217	TOP	2ND	H
00440000	00477777	0220	0237	TOP	2ND	J
00500000	00537777	0240	0257	TOP	2ND	K
00540000	00577777	0260	0277	TOP	2ND	L
00600000	00637777	0300	0317	TOP	2ND	M
00640000	00677777	0320	0337	TOP	2ND	N
00700000	00737777	0340	0357	TOP	2ND	P
00740000	00777777	0360	0377	TOP	2ND	R
01000000	01037777	0400	0417	3RD	4TH	H
01040000	01077777	0420	0437	3RD	4TH	J
01100000	01137777	0440	0457	3RD	4TH	K
01140000	01177777	0460	0477	3RD	4TH	L
01200000	01237777	0500	0517	3RD	4TH	M
01240000	01277777	0520	0537	3RD	4TH	N
01300000	01337777	0540	0557	3RD	4TH	P
01340000	01377777	0560	0577	3RD	4TH	R
01400000	01437777	0600	0617	3RD	4TH	H
01440000	01477777	0620	0637	3RD	4TH	J
01500000	01537777	0640	0657	3RD	4TH	K
01540000	01577777	0660	0677	3RD	4TH	L
01600000	01637777	0700	0717	3RD	4TH	M
01640000	01677777	0720	0737	3RD	4TH	N
01700000	01737777	0740	0757	3RD	4TH	P
01740000	01777777	0760	0777	3RD	4TH	R

TABLE 6-4D: 256KB INTERLEAVED DECODE (12128-E6) (Cont.)

02000000	02037777	1000	1017	5TH	6TH	H
02040000	02077777	1020	1037	5TH	6TH	J
02100000	02137777	1040	1057	5TH	6TH	K
02140000	02177777	1060	1077	5TH	6TH	L
02200000	02237777	1100	1117	5TH	6TH	M
02240000	02277777	1120	1137	5TH	6TH	N
02300000	02337777	1140	1157	5TH	6TH	P
02340000	02377777	1160	1177	5TH	6TH	R
02400000	02437777	1200	1217	5TH	6TH	H
02440000	02477777	1220	1237	5TH	6TH	J
02500000	02537777	1240	1257	5TH	6TH	K
02540000	02577777	1260	1277	5TH	6TH	L
02600000	02637777	1300	1317	5TH	6TH	M
02640000	02677777	1320	1337	5TH	6TH	N
02700000	02737777	1340	1357	5TH	6TH	P
02740000	02777777	1360	1377	5TH	6TH	R
03000000	03037777	1400	1417	7TH	8TH	H
03040000	03077777	1420	1437	7TH	8TH	J
03100000	03137777	1440	1457	7TH	8TH	K
03140000	03177777	1460	1477	7TH	8TH	L
03200000	03237777	1500	1517	7TH	8TH	M
03240000	03277777	1520	1537	7TH	8TH	N
03300000	03337777	1540	1557	7TH	8TH	P
03340000	03377777	1560	1577	7TH	8TH	R
03400000	03437777	1600	1617	7TH	8TH	H
03440000	03477777	1620	1637	7TH	8TH	J
03500000	03537777	1640	1657	7TH	8TH	K
03540000	03577777	1660	1677	7TH	8TH	L
03600000	03637777	1700	1717	7TH	8TH	M
03640000	03677777	1720	1737	7TH	8TH	N
03700000	03737777	1740	1757	7TH	8TH	P
03740000	03777777	1760	1777	7TH	8TH	R

TABLE 6-4F: 512KB INTERLEAVED DECODE (12256-E7)

ADDRESS		PPN		SLOT DSWSTAT BIT		
FROM	TO	FROM	TO	24=0	=1	ROW
00000000	00177777	0000	0077	TOP	2ND	H
00200000	00377777	0100	0177	TOP	2ND	J
00400000	00577777	0200	0277	TOP	2ND	K
00600000	00777777	0300	0377	TOP	2ND	L
01000000	01177777	0400	0477	TOP	2ND	H
01200000	01377777	0500	0577	TOP	2ND	J
01400000	01577777	0600	0677	TOP	2ND	K
01600000	01777777	0700	0777	TOP	2ND	L

TABLE 6-4F: 512KB INTERLEAVED DECODE (12256-E7) (Cont.)

02000000	02177777	1000	1077	3RD	4TH	H
02200000	02377777	1100	1177	3RD	4TH	J
02400000	02577777	1200	1277	3RD	4TH	K
02600000	02777777	1300	1377	3RD	4TH	L
03000000	03177777	1400	1477	3RD	4TH	H
03200000	03377777	1500	1577	3RD	4TH	J
03400000	03577777	1600	1677	3RD	4TH	K
03600000	03777777	1700	1777	3RD	4TH	L
04000000	04177777	2000	2077	5TH	6TH	H
04200000	04377777	2100	2177	5TH	6TH	J
04400000	04577777	2200	2277	5TH	6TH	K
04600000	04777777	2300	2377	5TH	6TH	L
05000000	05177777	2400	2477	5TH	6TH	H
05200000	05377777	2500	2577	5TH	6TH	J
05400000	05577777	2600	2677	5TH	6TH	K
05600000	05777777	2700	2777	5TH	6TH	L
06000000	06177777	3000	3077	7TH	8TH	H
06200000	06377777	3100	3177	7TH	8TH	J
06400000	06577777	3200	3277	7TH	8TH	K
06600000	06777777	3300	3377	7TH	8TH	L
07000000	07177777	3400	3477	7TH	8TH	H
07200000	07377777	3500	3577	7TH	8TH	J
07400000	07577777	3600	3677	7TH	8TH	K
07600000	07777777	3700	3777	7TH	8TH	L

TABLE 6-4H: 1024KB INTERLEAVED DECODE (12512-E8)

7106 (

ADDRESS		PPN		SLOT DSWSTAT BIT		
FROM	TO	FROM	TO	24=0	=1	ROW
00000000	00177777	0000	0077	TOP	2ND	H
00200000	00377777	0100	0177	TOP	2ND	J
00400000	00577777	0200	0277	TOP	2ND	K
00600000	00777777	0300	0377	TOP	2ND	L
01000000	01177777	0400	0477	TOP	2ND	M
01200000	01377777	0500	0577	TOP	2ND	N
01400000	01577777	0600	0677	TOP	2ND	P
01600000	01777777	0700	0777	TOP	2ND	R
02000000	02177777	1000	1077	TOP	2ND	H
02200000	02377777	1100	1177	TOP	2ND	J
02400000	02577777	1200	1277	TOP	2ND	K
02600000	02777777	1300	1377	TOP	2ND	L
03000000	03177777	1400	1477	TOP	2ND	M
03200000	03377777	1500	1577	TOP	2ND	N
03400000	03577777	1600	1677	TOP	2ND	P
03600000	03777777	1700	1777	TOP	2ND	R

TABLE 6-4H: 1024KB INTERLEAVED DECODE (12512-E8) (cont.)

04000000	04177777	2000	2077	3RD	4TH	H
04200000	04377777	2100	2177	3RD	4TH	J
04400000	04577777	2200	2277	3RD	4TH	K
04600000	04777777	2300	2377	3RD	4TH	L
05000000	05177777	2400	2477	3RD	4TH	M
05200000	05377777	2500	2577	3RD	4TH	N
05400000	05577777	2600	2677	3RD	4TH	P
05600000	05777777	2700	2777	3RD	4TH	R
06000000	06177777	3000	3077	3RD	4TH	H
06200000	06377777	3100	3177	3RD	4TH	J
06400000	06577777	3200	3277	3RD	4TH	K
06600000	06777777	3300	3377	3RD	4TH	L
07000000	07177777	3400	3477	3RD	4TH	M
07200000	07377777	3500	3577	3RD	4TH	N
07400000	07577777	0600	3677	3RD	4TH	P
07600000	07777777	3700	3777	3RD	4TH	R
10000000	10177777	4000	4077	5TH	6TH	H
10200000	10377777	4100	4177	5TH	6TH	J
10400000	10577777	4200	4277	5TH	6TH	K
10600000	10777777	4300	4377	5TH	6TH	L
11000000	11177777	4400	4477	5TH	6TH	M
11200000	11377777	4500	4577	5TH	6TH	N
11400000	11577777	4600	4677	5TH	6TH	P
11600000	11777777	4700	4777	5TH	6TH	R
12000000	12177777	5000	5077	5TH	6TH	H
12200000	12377777	5100	5177	5TH	6TH	J
12400000	12577777	5200	5277	5TH	6TH	K
12600000	12777777	5300	5377	5TH	6TH	L
13000000	13177777	5400	5477	5TH	6TH	M
13200000	13377777	5500	5577	5TH	6TH	N
13400000	13577777	5600	5677	5TH	6TH	P
13600000	13777777	5700	5777	5TH	6TH	R
14000000	14177777	6000	6077	7TH	8TH	H
14200000	14377777	6100	6177	7TH	8TH	J
14400000	14577777	6200	6277	7TH	8TH	K
14600000	14777777	6300	6377	7TH	8TH	L
15000000	15177777	6400	6477	7TH	8TH	M
15200000	15377777	6500	6577	7TH	8TH	N
15400000	15577777	6600	6677	7TH	8TH	P
15600000	15777777	6700	6777	7TH	8TH	R
16000000	16177777	7000	7077	7TH	8TH	H
16200000	16377777	7100	7177	7TH	8TH	J
16400000	16577777	7200	7277	7TH	8TH	K
16600000	16777777	7300	7377	7TH	8TH	L
17000000	17177777	7400	7477	7TH	8TH	M
17200000	17377777	7500	7577	7TH	8TH	N
17400000	17577777	7600	7677	7TH	8TH	P
17600000	17777777	7700	7777	7TH	8TH	R