Prime Computer, Inc.
Technology Drive
Milford, Massachusetts 01757-9911
617-478-8600

4050/4150 COMPUTER SYSTEMS

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SMN710-01

FOREWORD

Prime Computer Corporation is committed to a policy of providing the best possible service for our products and our customers. This manual, prepared for Customer Service Representatives, functions as a training aid and as a guide for installation, preventive, and corrective maintenance.

The manual is organized into chapters based on tasks Customer Service Engineers perform at the customer's site. Complex and time-consuming tasks are beyond the scope of this handbook.

Through experience and necessity, Customer Service Engineers develop methods that simplify installation and maintenance procedures. Since the best manuals consist of these field-proven shortcuts, Customer Service Documentation encourages you to forward any such procedures or comments to the following address:

Prime Computer, Inc.
Customer Service Documentation Manager
Technology Drive, M.S. 23B-13
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A self-addressed comment form is also included at the end of the manual for your reporting convenience.

Use of Warning, Caution and Note is as follows:

WARNING - To warn the operator of a potentially hazardous condition that may cause physical injury.

CAUTION - To caution the operator of a condition that could cause damage to the equipment.

NOTE - To provide additional information.

CREDITS

Technical Writer	Lisa Walker
Sr. Technical Editor	Patrice Wiggins
Technical Illustrator	Chuck Manning
Documentation Specialist	Robin Flood

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INDEX OF SERVICE MANUALS

SYSTEMS	PART NUMBER
MODEL TLA10113 POWER SUPPLY	APP010
50 SERIES COMPUTER SYSTEMS	SMN070-C
1ST UPDATE TO SMN070-C: UPDATED FRU PARTS LIST	SMN070-C1
PW90 SERIES WORKSTATIONS	SMN150
2250 COMPUTER SYSTEM	SMN200-A
1ST UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN200-A1
CAD GRAPHICS WORKSTATION (PW200)	SMN210
9000-ECL-CPU SYSTEMS	SMN230-B
1ST UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN230-B1
2550, 2655, AND 2755 COMPUTER SYSTEMS	SMN270
1ST UPDATE: INCLUDES 2655 COMPUTER SYSTEM INFO.	SMN270-01
2ND UPDATE: INCLUDES 2755 COMPUTER SYSTEM INFO.	SMN270-02
3RD UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN270-03
2550/2655 SYSTEM TO 2755 SYSTEM UPGRADE	UPG270
PRIME PRODUCER WORKSTATION (PW100)	SMN290
1ST UPDATE TO SMN290: UPDATED FRU PARTS LIST	SMN290-01
9650 AND 9655 COMPUTER SYSTEMS	SMN360
1ST UPDATE: INCLUDES 9655 COMPUTER SYSTEM INFO.	SMN360-01
2ND UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN360-02
2350, 2450 AND 2455 COMPUTER SYSTEMS: VOLUME 1	SMN380-A-V1
2350, 2450 AND 2455 COMPUTER SYSTEMS: VOLUME 2	SMN380-A-V2
1ST UPDATE: INCLUDES 258MB DISK DRIVE INFO.	SMN380-A1
2ND UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN380-A2
3RD UPDATE: INCLUDES 258MB DISK DRIVE	SMN380-A3
PERFORMER PERSONAL COMPUTER	SMN410-A
1ST UPDATE TO SMN410-A: UPDATED FRU PARTS LIST	SMN410-A1
7564S PERIPHERAL CABINET	SPM460
6000 SERIES COMPUTER SYSTEMS (BINDER)	SMN700
6000 SERIES COMPUTER SYSTEMS	SMN700-A
6350 TO 6550 SYSTEM UPGRADE	UPG700
4050/4150 COMPUTER SYSTEMS	SMN710
1ST UPDATE	SMN710-01
EXL 316 COMPUTER SYSTEM	SPM730
MODEL 4450 COMPUTER SYSTEM (PRELIMINARY)	SMN760-P
WS-3600 CAD WORKSTATION	SPM910

DISK DRIVES

CDC 40 & 80 MBYTE SMD	SMN040
1ST UPDATE TO SMN040: UPDATED FRU PARTS LIST	SMN040-01
CDC 32, 64 & 96 MBYTE CMD	SMN090
300 MEGABYTE STORAGE MODULE DRIVE	SMN120-A
1ST UPDATE TO SMN120-A: UPDATED FRU PARTS LIST	SMN120-A1
CDC 160 MBYTE MMD	SMN170
1ST UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN170-01
CDC 600 MBYTE FMD	SMN220
1ST UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN220-01
300 MEGABYTE FIXED MODULE DISK	SMN320
1ST UPDATE: INCLUDES UPDATED FRU PARTS LIST	SMN320-01
315MB FIXED MODULE DISK SUPPLEMENT	SSP320
258MB DISK DRIVE UPGRADE	UPG380
328MB DISK DRIVE UPGRADE	UPG380-01
MODEL 4835 DISK DRIVE	SPM390
496MB FIXED MODULE DISK SUBSYSTEM	SPM470

TAPE DRIVES

KENNEDY MAGNETIC TAPE	SMN020
TELEX 6250 BPI TAPE	SMN130
MAGNETIC STREAMING TAPE SUBSYSTEM	SMN280
1ST UPDATE TO SMN280: UPDATED FRU PARTS LIST	SMN280-01
4590 GCR MAGNETIC TAPE SUBSYSTEM	SPM430
MODEL 9612 TAPE DRIVE	SPM920

PRINTERS

DATA PRINTER 300/600 LPM	SMN060
1ST UPDATE TO SMN060: UPDATED FRU PARTS LIST	SMN060-01
PRINTRONIX MODEL 300 PRINTER	SMN110
1ST UPDATE TO SMN110: UPDATED FRU PARTS LIST	SMN110-01
NEC SPINWRITER	SMN140
DATAPRODUCTS PRINTER 300/600 LPM	SMN160
LETTER QUALITY PRINTER (3185)	SMN340
1ST UPDATE TO SMN340: UPDATED FRU PARTS LIST	SMN340-01
MODEL 3410 LASER PRINTER	SPM730
MODEL 3280 - 1200 LPM BAND PRINTER	SPM930

MONITORS

GE TERMINET 30	SMN010
P.E. FOX AND OWL TERMINALS	SMN030
GE TERMINET 2030	SMN180
PRIME SYSTEM TERMINAL (PST100)	SMN240
PT200, PT200C & PT250 TERMINALS	SMN350-B

COMMUNICATIONS

INTELLIGENT COMMUNICATIONS SUBSYSTEMS (ICS)	SMN250-B
FIRST UPDATE TO SMN250-B: UPDATE PARTS LIST	SMN250-B1
SECOND UPDATE TO SMN250-B	SMN250-B2
COMMUNICATIONS (BINDER ONLY)	SMN600
PRIMENET NODE CONTROLLER	SMN601
ASYNCHRONOUS MULTI-LINE CONTROLLER BOARD	SMN602
1ST UPDATE TO SMN602: UPDATED FRU PARTS LIST	SMN602-01
LAN300 LOCAL AREA NETWORK	SMN603

CONTROLLER/MEMORY

CONTROLLER/MEMORY BOARDS (BINDER ONLY)	SMN500
APPENDIX A: MEMORY QUICK REFERENCE	SMN500-0
MODEL 6580 INTELLIGENT DISK CONTROLLER	SMN501
MMW1-2MB & MMW1-4MB MEMORY BOARDS	SMN550-A
MMW2-4MB & MMW2-8MB MEMORY ARRAY BOARDS	SMN551-A
MMW3-16MB & MMW3-32MB MEMORY BOARDS	SMN552

QUICK REFERENCE GUIDES

CUSTOMER SERVICE TECHNICAL HANDBOOK	SMN801
DATA COMMUNICATIONS BASICS: COMMUNICATIONS MODULE FOR C/S TECHNICAL HANDBOOK	SMN802

SOFTWARE GUIDES

PRIMOS AND UTILITIES SOFTWARE SERVICE GUIDE (BINDER)	SSG080
PRIMOS AND UTILITIES, OVERVIEW	SSG081-A
PRIMOS AND UTILITIES, INSTALLATION (REV. 21)	SSG082-21-A
PRIMOS AND UTILITIES, INSTALLATION (REV. 22)	SSG082-22
PRIMOS AND UTILITIES, OPERATING PROCEDURES	SSG083
DIAGNOSTSIC TESTING SYSTEM SOFTWARE SERVICE GUIDE	SSG400
FUNDAMENTALS OF UNIX	SSG750
TEST AND MAINTENANCE	SMN800

CHAPTER 1. GENERAL DESCRIPTION.................................. 1- 1

1.1 MODEL 4050/4150 NEW FEATURES.............................. 1- 2
1.2 SYSTEM OVERVIEW.. 1- 2
1.2.1 CPU BOARD SET.. 1- 4
1.2.2 VCP-V DIAGNOSTIC PROCESSOR............................. 1- 4
1.2.3 MODEL MMW3-8MB, MMW3-16MB, and MMW3-32MB MEMORY ARRAY BOARDS... 1- 4
1.2.4 STATUS PANEL... 1- 4
1.2.5 POWER SUPPLIES... 1- 4
1.2.6 BLOWER ASSEMBLY.. 1- 5
1.2.7 TILT BULKHEAD.. 1- 5
1.2.8 POWER DISTRIBUTION UNIT................................ 1- 5
1.3 OPTIONAL COMPONENTS...................................... 1- 5
1.4 SOFTWARE/HARDWARE DEPENDENCIES........................... 1- 6
1.5 CONFIGURATION GUIDELINES................................. 1- 6
1.6 SPECIFICATIONS... 1- 7
1.7 RELATED DOCUMENTATION.................................... 1- 9
1.8 FCO LOG.. 1-10
1.9 EQUIPMENT IDENTIFICATION................................. 1-10
1.10 MARKETING MODEL NUMBERS................................. 1-10

CHAPTER 2. INSTALLATION... 2- 1

2.1 INVENTORY AND INSPECTION................................. 2- 1
2.2 HANDLING PRECAUTIONS..................................... 2- 1
2.3 SITE SURVEY.. 2- 3
2.4 SYSTEM UNPACKING... 2- 5
2.4.1 SYSTEM CABINETS.. 2- 5
2.4.1.1 Unpacking Air Shipments.............................. 2- 6
2.4.1.2 Unpacking Ground Shipments........................... 2- 6
2.4.2 CABINET-MOUNTED AND FREE-STANDING PERIPHERALS.......... 2- 6
2.4.3 MISCELLANEOUS ITEMS AND SOFTWARE BOXES................. 2- 6
2.5 REPACKING.. 2- 9
2.6 VERIFYING AND CONVERTING VOLTAGES........................ 2- 9
2.6.1 VERIFYING VOLTAGE CONFIGURATION........................ 2- 9
2.6.2 CONVERTING THE TLA10113 POWER SUPPLIES................. 2-12
2.6.2.1 Converting 120 Vac Power Supply To 240 Vac........... 2-14
2.6.2.2 Converting 240 Vac Power Supply To 120 Vac........... 2-16
2.7 SYSTEM INSTALLATION...................................... 2-16
2.7.1 SYSTEM CONFIGURATION OVERVIEW.......................... 2-17
2.7.1 n mum Configuration Requirements..................... 2-17
2.7.1.2 System Configuration Guidelines...................... 2-17
2.7.1.3 System Interconnection Diagram....................... 2-19
2.7.2 CABLING AND VERIFYING THE POWER DISTRIBUTION UNIT...... 2-19
2.7.2.1 Installing the Main AC Power Cable................... 2-19
2.7.2.2 Verifying the PDU Cabling............................ 2-19
2.7.2.2.1 Verifying Mainbay PDU Cabling...................... 2-19
2.7.2.2.2 Verifying Peripheral Cabinet PDU Cabling........... 2-23
2.7.2.3 Daisy-Chaining Mainbay and Peripheral Cabinets....... 2-23
2.7.3 INSTALLING TLA10113 POWER SUPPLIES..................... 2-25

2.7.4 VERIFYING POWER SHUNT BOARD INSTALLATION............. 2-25
2.7.5 INSTALLING THE MEMORY BATTERY BACKUP UNIT (MBBU)..... 2-25
2.7.6 INSTALLING THE UNINTERRUPTIBLE POWER SUPPLY.......... 2-27
2.7.7 INSTALLING MEMORY BOARDS............................. 2-28
2.7.7.1 Memory Board Handling Precautions............ 2-28
2.7.7.2 Memory Board Configuration................... 2-28
2.7.8 CONFIGURING AND CABLING THE VCP-V.................... 2-29
2.7.8.1 Removing the Shipping Material............... 2-29
2.7.8.2 Configuring the Diagnostic Processor......... 2-29
2.7.8.3 Verifying the System Identification Board.... 2-34
2.7.8.4 Cabling the Diagnostic Processor............. 2-34
2.7.9 VERIFYING CPU BOARD INSTALLATION..................... 2-38
2.7.10 INSTALLING THE SYSTEM CONSOLE....................... 2-38
2.8 INSTALLING THE I/O SUBSYSTEM............................... 2-40
2.8.1 I/O CONFIGURATION GUIDELINES......................... 2-40
2.8.2 PERIPHERAL CABINET CONFIGURATION GUIDELINES.......... 2-43
2.8.3 CONTROLLER DEVICE ADDRESS SUMMARY.................... 2-44
2.8.4 INSTALLING THE INTELLIGENT DISK CONTROLLER (IDC1).... 2-46
2.8.4.1 Configuration Rules.......................... 2-46
2.8.4.2 Controller Settings.......................... 2-47
2.8.4.3 IDC1 Insertion and Cabling................... 2-47
2.8.5 INSTALLING THE SCSI TAPE CONTROLLER (MSTC)........... 2-49
2.8.5.1 Converting the 2382 Controller............... 2-51
2.8.5.2 Verifying MSTC Device Address and Revision Jumpers.. 2-51
2.8.5.3 Installing and Cabling the MSTC.............. 2-52
2.8.6 INSTALLING THE INTELLIGENT COMMUNICATIONS CONTROLLER (ICS3).. 2-53
2.8.6.1 Using This Installation Guide....:........... 2-53
2.8.6.2 Verifying ICS3 Configuration................. 2-55
2.8.6.2.1 Controller Board (ICS3)................. 2-56
2.8.6.2.2 Buffer Card (ICS3)...................... 2-58
2.8.6.2.3 LAC Bus Backplane (ICS3)................ 2-58
2.8.6.3 Installing the ICS3 Controller Board......... 2-61
2.8.6.4 Installing the ICS3 Card Cage................ 2-61
2.8.6.4.1 Installing an ICS3 in the Mainbay....... 2-61
2.8.6.4.2 Installing an ICS3 in a 30-Inch Peripheral Cabinet............................. 2-65
2.8.6.4.3 Installing an ICS3 in a 53-Inch Peripheral Cabinet............................. 2-68
2.8.6.5 Installing ICS3 Line Adapter Cards (LACs).... 2-72
2.8.6.6 Cabling Devices to the ICS3.................. 2-74
2.8.6.7 Transferring ICS3 Card Cage.................. 2-74
2.8.6.7.1 Card Cage Transfer From Mainbay to 30-Inch Peripheral Bay......................... 2-74
2.8.6.7.2 Card Cage Transfer From Mainbay to 53-Inch Peripheral Bay......................... 2-78
2.8.6.7.3 Card Cage Transfer From 30-Inch Peripheral Bay to Mainbay...................... 2-79
2.8.6.7.4 Card Cage Transfer From 30-Inch To 53-Inch Peripheral Bay......................... 2-80
2.8.7 CONFIGURING AND CABLING THE PRIMENET NODE CONTROLLER (PNC)... 2-81
2.8.7.1 Configuring the PNC Controller............... 2-82

2.8.7.2 Installing the PNC/PNC-II Controller Board... 2-82
2.8.7.3 Installing the PNC Modular Junction Box...... 2-82
2.8.8 INSTALLING THE LHC300 CONTROLLER.................... 2-85
2.8.9 INSTALLING THE MODEL 4735 (496 MB) DISK DRIVE........ 2-85
2.8.9.1 Installing a Premounted Drive................ 2-85
2.8.9.1.1 Verifying/Converting Drive Voltage...... 2-85
2.8.9.1.2 Verifying and Completing Premounted Drive Cabling.................................. 2-86
2.8.9.2 Installing An Add-On Drive.................. 2-89
2.8.9.2.1 Allocating Cabinet Space................ 2-89
2.8.9.2.2 Converting Drive Voltage................ 2-89
2.8.9.2.3 Organizing the Mounting Hardware........ 2-89
2.8.9.2.4 Assembling the T-Bar Mounting Hardware.. 2-91
2.8.9.2.5 Mounting the T-Bar in the Cabinet....... 2-91
2.8.9.2.6 Installing the Intermediate and Outer Rails.. 2-94
2.8.9.2.7 Installing the Filler Panel, Inner Rails, and Disk Drive......................... 2-95
2.8.9.2.8 Cabling the Disk Drive and Cabinets..... 2-97
2.8.10 INSTALLING THE MODEL 4835 (770 MB) DISK DRIVE....... 2-98
2.8.10.1 Installing a Premounted Drive............... 2-99
2.8.10.1.1 Verifying/Converting Drive Voltage..... 2-99
2.8.10.1.2 Verifying and Completing Premounted Drive Cabling.................................. 2-99
2.8.10.2 Installing An Add-On Drive..................2-102
2.8.10.2.1 Allocating Cabinet Space................2-102
2.8.10.2.2 Verifying/Converting Drive Voltage.....2-103
2.8.10.2.3 Organizing the Mounting Hardware.......2-103
2.8.10.2.4 Assembling the Tray....................2-104
2.8.10.2.5 Securing the Tray to the Cabinet.......2-106
2.8.10.2.6 Installing the Trim Panel..............2-108
2.8.10.2.7 Installing the Filler Panel............2-108
2.8.10.2.8 Installing and Cabling the Drive.......2-108
2.8.11 INSTALLING THE MODEL 4587 (QUAD DENSITY) TAPE DRIVE 2-111
2.8.11.1 Verifying/Converting Drive Voltage..........2-112
2.8.11.2 Verifying and Completing Premounted Tape Drive Cabling.....................................2-113
2.8.12 I/O SUBSYSTEM CABLING DIAGRAMS.......................2-113
2.9 HARDWARE INSTALLATION CHECKOUT............................2-113
2.10 SOFTWARE INSTALLATION...................................2-130
2.11 FINAL CHECKOUT...2-131
2.12 DAMAGED/MISSING EQUIPMENT CORRECTIVE PROCEDURES...........2-131
2.12.1 REPORTING DAMAGED EQUIPMENT.........................2-131
2.12.2 REPORTING WRONG EQUIPMENT SHIPPED..................2-132
2.12.3 REPORTING SHORT SHIPMENT............................2-132
2.12.4 ORDERING PARTS......................................2-132
2.12.4.1 Ordering Individual Parts...................2-132
2.12.4.2 Ordering Kit Parts..........................2-133

CHAPTER 3. OPERATING INSTRUCTIONS................................ 3- 1

3.1 CONTROLS AND INDICATORS.................................... 3- 1
3.1.1 STATUS PANEL CONTROLS AND INDICATORS................. 3- 2

3.1.2 POWER DISTRIBUTION UNIT (PDU) CONTROLS AND INDICATORS........ 3- 5
3.1.3 TLA10113 POWER SUPPLY CONTROLS AND INDICATORS........ 3- 7
3.1.4 FLOPPY DISK DRIVE CONTROLS AND INDICATORS........ 3- 8
3.1.5 MODEL 4735 DISK DRIVE CONTROLS AND INDICATORS........ 3- 8
3.1.6 MODEL 4835 DISK DRIVE CONTROLS AND INDICATORS........ 3- 9
3.1.7 MODEL 4587 TAPE DRIVE CONTROLS AND INDICATORS........ 3-10
3.1.8 PNC & MODULAR JUNCTION BOX CONTROLS AND INDICATORS... 3-14
3.1.8.1 PNC-II Controller........ 3-14
3.1.8.2 Modular Junction Box........ 3-15
3.1.9 ICS3 CONTROLS AND INDICATORS........ 3-16
3.1.9.1 ICS3 Controller Board Indicators........ 3-17
3.1.9.2 ICS3 Buffer Card Indicators........ 3-17
3.1.9.3 ICS3 Power Supply Controls and Indicators.... 3-17
3.1.10 OTHER SYSTEM AND BOARD INDICATORS........ 3-20
3.2 FLOPPY DISK DRIVE OPERATION........ 3-20
3.2.1 INSERTING THE FLOPPY DISK........ 3-20
3.2.2 REMOVING THE FLOPPY DISK........ 3-21
3.2.3 FLOPPY DISK CARE, HANDLING, AND STORAGE........ 3-22
3.3 PRIMENET NODE CONTROLLER OPERATIONS........ 3-22
3.4 INTELLIGENT COMMUNICATIONS SUBSYSTEM 3 (ICS3) OPERATIONS... 3-22
3.5 SYSTEM POWER-UP AND AUTOBOOT TO PRIMOS........ 3-23
3.6 SYSTEM POWER-DOWN........ 3-24
3.7 TERMINAL PORTS OPERATION........ 3-24
3.7.1 LOCAL 1 TERMINAL PORT........ 3-26
3.7.2 LOCAL 2 TERMINAL PORT........ 3-26
3.7.3 SPARE TERMINAL PORT........ 3-26
3.7.4 REMOTE TERMINAL PORT........ 3-26
3.8 VCP-V OPERATION........ 3-27
3.8.1 CONTROL PANEL MODE........ 3-27
3.8.1.1 Entering CP Mode........ 3-27
3.8.1.2 Exiting CP Mode........ 3-28
3.8.1.3 Control Panel Mode Commands........ 3-28
3.8.1.3.1 CP Operations Commands........ 3-29
3.8.1.3.2 Microdiagnostic File Operations Commands........ 3-41
3.8.1.3.3 Memory Display Commands........ 3-42
3.8.1.3.4 Memory Access Commands........ 3-43
3.8.2 SYSTEM TERMINAL MODE........ 3-43
3.8.3 USER MODE........ 3-43
3.8.4 PROCESSOR DIAGNOSTIC AID MODE........ 3-44
3.9 INFORMATIONAL MESSAGE SUMMARY........ 3-44
3.10 BASIC PRIMOS OPERATIONS........ 3-46
3.10.1 SENSE SWITCH SETTINGS........ 3-46
3.10.1.1 Sense Switch Boot Options........ 3-47
3.10.1.2 Boot Devices........ 3-48
3.10.1.3 Data Switch Boot Options........ 3-48
3.10.1.4 Sample Boot Option Words........ 3-49
3.10.2 BOOTING PRIMOS........ 3-49
3.10.2.1 Booting PRIMOS from Disk........ 3-49
3.10.2.2 Booting PRIMOS from Tape........ 3-51
3.10.3 PRIMOS UTILITIES........ 3-52
3.10.3.1 MTRESUME........ 3-52
3.10.3.2 BOOT_CREATE........ 3-53

3.10.3.3 MAKE.SAVE.................................... 3-54
3.10.3.4 FIX_DISK.SAVE................................ 3-55
3.10.3.5 COPY_DISK.SAVE............................... 3-57
3.10.3.6 MAGSAV/MAGRST................................ 3-58
3.10.4 CHANGES TO PRIMOS SINCE REVISION 20................. 3-59
3.10.4.1 Startup Messages............................. 3-59
3.10.4.2 Halt Messages................................ 3-59
3.10.4.3 Status Command............................... 3-60
3.10.4.4 SHUTDN -FORCE Option......................... 3-60
3.10.5 CHANGES TO PRIMOS AT REV. 21....................... 3-61
3.10.5.1 Coldstarting the System...................... 3-61
3.10.5.2 Partial Tape Dump............................ 3-62
3.10.5.3 New PRIMOS Commands.......................... 3-62
3.10.5.4 Physical Device Numbers...................... 3-63
3.11 DISTRIBUTED SYSTEM MANAGEMENT (DSM) OPERATIONS............ 3-63
3.11.1 START_DSM... 3-64
3.11.2 DSM OPERATIONS COMMANDS............................. 3-64
3.11.3 STOP_DSM.. 3-65

CHAPTER 4. PRINCIPLES OF OPERATION.............................. 4- 1

4.1 CENTRAL PROCESSING UNIT.................................... 4- 1
4.1.1 PROCESSOR OVERVIEW.................................... 4- 3
4.1.2 IS BOARD.. 4- 4
4.1.2.1 Pipeline Control Unit........................... 4- 6
4.1.2.1.1 Pipeline Functions.......................... 4- 6
4.1.2.1.2 Stage Clock Generation...................... 4- 6
4.1.2.2 Instruction Unit................................ 4- 7
4.1.2.2.1 Instruction Decoding........................ 4- 7
4.1.2.2.2 Effective Address Formation................. 4- 7
4.1.2.2.3 Register File Collisions.................... 4- 7
4.1.2.3 Storage Management Unit......................... 4- 7
4.1.2.3.1 Cache Logic................................. 4- 8
4.1.2.3.2 Cache Addressing............................ 4- 8
4.1.2.3.3 Branch Cache Operations..................... 4- 9
4.1.2.3.4 Segment Table Lookaside Buffer (STLB)....... 4- 9
4.1.2.3.5 Memory Traps................................ 4- 9
4.1.3 E BOARD... 4- 9
4.1.3.1 Execution Unit.................................. 4-11
4.1.3.1.1 Arithmetic Logic Unit (ALU) Slices.......... 4-11
4.1.3.1.2 Barrel Shifter.............................. 4-12
4.1.3.1.3 Register File Logic......................... 4-12
4.1.3.2 I/O Addressing Interface........................ 4-12
4.1.3.3 Timers.. 4-12
4.1.4 CMI BOARD... 4-12
4.1.4.1 Control Store Unit.............................. 4-14
4.1.4.1.1 Microsequencer Logic........................ 4-14
4.1.4.1.2 Control Store RAM........................... 4-14
4.1.4.1.3 Maintenance & Initialization Logic.......... 4-14
4.1.4.1.4 Decode Net.................................. 4-15
4.1.4.1.5 Modals...................................... 4-15
4.1.4.1.6 Effective Address Field (EAF) PROMs......... 4-15
4.1.4.1.7 Parity Checkers............................. 4-15

4.1.4.1.8 Bus Operand Source (BOPS) Logic........ 4-15
4.1.4.1.9 Opcode Latch........................... 4-15
4.1.4.1.10 BCYPDA Bus............................ 4-15
4.1.4.2 Memory Controller Unit...................... 4-15
4.1.4.2.1 Write Buffer (WB)....................... 4-16
4.1.4.2.2 Memory Timer (MT)....................... 4-16
4.1.4.2.3 I/O Data Interface...................... 4-16
4.1.5 VLSI REQUIREMENTS................................. 4-16
4.1.5.1 Microsequencer.............................. 4-17
4.1.5.2 Cache Address............................... 4-17
4.1.5.3 STLB Set Select............................. 4-17
4.1.5.4 Cache Set Select............................ 4-17
4.1.5.5 Execution ALU (PEALU)....................... 4-18
4.1.5.6 Barrel Shifter.............................. 4-18
4.1.5.7 Write Buffer Address........................ 4-18
4.1.5.8 Register File Address....................... 4-18
4.2 MAJOR SYSTEM BUSES.................................. 4-18
4.2.1 BUS BLEG (BB)..................................... 4-19
4.2.2 BUS DATA (BD)..................................... 4-19
4.2.3 BUS PERIPHERAL ADDRESS (BPA) AND BUS PERIPHERAL DATA (BPD).. 4-19
4.2.4 BUSES MEMORY ADDRESS (MA) AND MEMORY DATA (MD)....... 4-19
4.3 MEMORY SUBSYSTEM.................................... 4-20
4.3.1 MEMORY ARRAY LAYOUT............................... 4-20
4.3.2 MEMORY ARRAY SELECTION............................ 4-20
4.3.3 FUNCTIONAL DESCRIPTION............................ 4-21
4.3.4 MEMORY OPERATIONS................................. 4-24
4.3.4.1 Refresh Cycle............................... 4-24
4.3.4.2 Write Cycle................................. 4-25
4.3.4.2.1 39-Bit Write............................ 4-25
4.3.4.2.2 78-Bit Write............................ 4-25
4.3.4.2.3 Diagnostic Aid Lock Check Bits.......... 4-26
4.3.4.3 Read Cycle.................................. 4-26
4.3.5 BATTERY BACKUP UNIT FOR MEMORY SUBSYSTEMS.......... 4-26
4.4 I/O CONTROLLERS..................................... 4-26
4.4.1 PERIPHERAL CONTROLLERS............................ 4-28
4.4.2 COMMUNICATIONS CONTROLLERS........................ 4-28
4.4.2.1 Intelligent Communications Subsystem 3 (ICS3)....................................... 4-29
4.4.2.1.1 ICS3 Controller......................... 4-29
4.4.2.1.2 Sixteen-Slot Card Cage.................. 4-30
4.4.2.1.3 Buffer Card............................. 4-30
4.4.2.1.4 LAC Backplane........................... 4-30
4.4.2.1.5 Line Adapter Cards...................... 4-30
4.4.2.2 PRIMENET Node Controller (PNC-II)............ 4-30
4.4.2.2.1 Controller Assembly..................... 4-31
4.4.2.2.2 Functional Descriptions................. 4-35
4.4.2.3 Asynchronous Multi-Line Controller (AMLC).... 4-37
4.4.2.4 LAN300 Controller........................... 4-37
4.4.2.5 Multi-Data Link Controller (MDLC)............ 4-38
4.5 VCP-V DIAGNOSTIC PROCESSOR.......................... 4-39
4.5.1 VCP-V FUNCTIONAL DESCRIPTION....................... 4-39
4.5.1.1 Z80 Microprocessor.......................... 4-40
4.5.1.2 Memory...................................... 4-40

4.5.1.3 Serial Number And Identification PROMs....... 4-40
4.5.1.4 Serial Port Operation........................ 4-41
4.5.1.4.1 Local 1 Port Operation................... 4-42
4.5.1.4.2 Local 2 Port Operation................... 4-42
4.5.1.4.3 Remote Port Operation.................... 4-43
4.5.1.4.4 Spare Port Operation..................... 4-45
4.5.1.5 Floppy Disk Drive Interface.................. 4-46
4.5.1.5.1 CPU Microcode Diskette................... 4-46
4.5.1.5.2 Microdiagnostic Diskette................. 4-48
4.5.1.6 On-Board Modem............................... 4-48
4.5.1.7 Environmental Sensing Hardware............... 4-48
4.5.1.7.1 Air Flow Sensor Operation................ 4-50
4.5.1.7.2 CPU Board Temperature Sensor Operation.. 4-50
4.5.1.7.3 VCP-V Board Temperature Sensor.......... 4-51
4.5.1.8 VCP-V Power Systems Support.................. 4-52
4.5.1.8.1 PDU Support.............................. 4-52
4.5.1.8.2 UPS Support.............................. 4-53
4.5.1.8.3 MBBU Support............................. 4-54
4.5.1.8.4 Power Supply Support..................... 4-55
4.5.1.9 Soft Shut-Down Support....................... 4-60
4.5.1.10 Time of Day Clock........................... 4-61
4.5.2 VCP-V SELF-VERIFICATION TESTS AND POWER-UP PROCEDURES.. 4-61
4.5.2.1 VCP-V Memory Test............................ 4-61
4.5.2.2 Initial Environmental Sensor Test............ 4-62
4.5.2.3 System Power Test............................ 4-63
4.5.2.4 Second Environmental Sensor Test............. 4-63
4.5.2.5 Floppy Disk Check Sector Test................ 4-64
4.5.2.6 System Validation and VCP-V Application Software Load...................................... 4-64
4.5.2.7 Initial Time of Day Clock Test............... 4-65
4.5.2.8 System Configuration File Load............... 4-65
4.5.2.9 Second System Power Supplies Test............ 4-66
4.5.2.9.1 Power Down Test.......................... 4-67
4.5.2.9.2 Power Up Test............................ 4-67
4.5.2.9.3 Margin Low Test.......................... 4-68
4.5.2.9.4 Margin High Test......................... 4-69
4.5.2.9.5 Voltage Test............................. 4-69
4.5.2.9.6 PDU Sequencing Test...................... 4-70
4.5.2.10 Time Of Day Clock Test...................... 4-70
4.5.2.11 CPU Control Store Test...................... 4-70
4.6 POWER DISTRIBUTION UNIT............................. 4-71
4.6.1 CENTRAL PROCESSOR PDU............................ 4-71
4.6.2 PERIPHERAL CABINET PDU........................... 4-71
4.7 TLA10113 POWER SUPPLIES............................. 4-71
4.7.1 SYSTEM POWER SUPPLY DESCRIPTION.................. 4-72
4.7.2 POWER INPUTS..................................... 4-72
4.7.2.1 AC Input Connector........................... 4-72
4.7.2.2 BBU Connector................................ 4-72
4.7.3 POWER SUPPLY FRONT PANEL CONNECTOR............... 4-74
4.7.4 POWER SUPPLY SIGNAL INPUTS....................... 4-75
4.7.5 POWER SUPPLY SIGNAL OUTPUTS...................... 4-75
4.7.6 DIAGNOSTIC LEDS.................................. 4-76
4.7.7 POWER SUPPLY PROTECTION.......................... 4-77

4.7.7.1 Overvoltage Protection........................ 4-77
4.7.7.2 Overcurrent Protection........................ 4-77
4.7.7.3 Overtemperature Protection.................... 4-77
4.8 FLOPPY DISK DRIVES.................................... 4-77
4.8.1 OPERATING MODES.................................. 4-77
4.8.2 PHYSICAL DESCRIPTION............................. 4-78
4.8.3 ELECTRICAL DESCRIPTION........................... 4-78
4.9 COOLING SYSTEM.. 4-78
4.9.1 COOLING SYSTEM OVERVIEW.......................... 4-78
4.9.2 BLOWER SPEED CONTROL............................. 4-80
4.9.3 BLOWER BYPASS SWITCH............................. 4-81
4.9.4 BLOWER POWER REQUIRMENTS......................... 4-81
4.10 UNINTERRUPTIBLE POWER SUPPLY......................... 4-82
4.11 DISTRIBUTED SYSTEM MANAGEMENT (DSM).................. 4-83
4.11.1 ADMINISTRATION AND ACCESS CONTROL................ 4-84
4.11.2 UNSOLICITED MESSAGE HANDLING..................... 4-85
4.11.3 DSM LOGGING...................................... 4-85

CHAPTER 5. PREVENTIVE MAINTENANCE.......................... 5- 1

5.1 REVIEWING SYSTEM HISTORY.............................. 5- 1
5.1.1 CHECKING THE SYSTEM LOGBOOK....................... 5- 1
5.1.2 CHECKING THE HISTORY DISK........................ 5- 2
5.1.3 CHECKING THE EVENT LOGGERS....................... 5- 4
5.1.3.1 System Event Logger, Rev. 20.2.3............. 5- 4
5.1.3.2 Network Event Logger, Rev. 20.2.3............ 5- 9
5.1.3.3 Event Loggers, Rev. 21....................... 5-11
5.1.3.3.1 Enabling and Disabling Event Logging.... 5-12
5.1.3.3.2 Reviewing Log Files..................... 5-12
5.2 PERFORMING PREVENTIVE MAINTENANCE..................... 5-13
5.2.1 SYSTEM SHUTDOWN.................................. 5-13
5.2.2 CLEANING AND INSPECTING MODEL 4050/4150 SYSTEMS...... 5-14
5.2.3 MODEL 4050/4150 SYSTEMS ADJUSTMENTS.............. 5-14
5.2.4 PERIPHERALS MAINTENANCE.......................... 5-14
5.2.5 ENVIRONMENTAL CHECKOUT........................... 5-15
5.2.6 SYSTEM STARTUP................................... 5-15
5.3 COMPLETING A PM SCHEDULE.............................. 5-15

CHAPTER 6. CORRECTIVE MAINTENANCE.......................... 6- 1

6.1 EVALUATING THE PROBLEM................................ 6- 2
6.1.1 CHECKING SYSTEM DIAGNOSTIC MESSAGES AND LEDS......... 6- 2
6.1.2 GATHERING INFORMATION ABOUT THE PROBLEM.............. 6- 2
6.1.3 CATEGORIZING THE PROBLEM......................... 6- 3
6.2 PERFORMING GENERAL TROUBLESHOOTING ROUTINES............ 6- 3
6.3 ISOLATING AND CORRECTING THE PROBLEM.................. 6- 3
6.3.1 TROUBLESHOOTING POWER-UP FAILURES................. 6- 6
6.3.1.1 AC Power Problems............................ 6- 6
6.3.1.2 Power-Up Sequence Problems................... 6- 9
6.3.1.3 Verifying the AC Mains Voltage............... 6-13
6.3.1.3.1 Domestic Installations.................. 6-13
6.3.1.3.2 International Installations............. 6-13

6.3.1.4 Measuring Backplane Voltages................. 6-15
6.3.2 TROUBLESHOOTING SYSTEM VERIFICATION AND
INITIALIZATION FAILURES................................ 6-17
6.3.2.1 CPU Verification Failure..................... 6-17
6.3.2.2 CPU Initialization Failure................... 6-18
6.3.3 TROUBLESHOOTING BOOT AND COLDSTART FAILURES.......... 6-19
6.3.3.1 CPBOOT Failure............................... 6-19
6.3.3.2 System Coldstart Failure..................... 6-21
6.3.3.3 System Messages During Boot Operations....... 6-24
6.3.3.3.1 CPBOOT Error Messages.................. 6-24
6.3.3.3.2 BOOT Halts With Location Code Numbers... 6-29
6.3.3.3.3 BOOT.SAVE Halts with Error Messages..... 6-30
6.3.3.3.4 Halts During PRIMOS.SAVE Execution...... 6-32
6.3.4 TROUBLESHOOTING POWER/ENVIRONMENTAL/VCP-V FAILURES
DURING NORMAL OPERATION................................ 6-38
6.3.4.1 Power/Environmental/VCP Failures Flowchart... 6-38
6.3.4.2 Sensor Check Troubleshooting................. 6-40
6.3.4.3 TLA10113 Power Supply Adjustments............ 6-40
6.3.4.4 Using the STATUS Command to Monitor System
Power.. 6-42
6.3.5 TROUBLESHOOTING SYSTEM HALTS.......................... 6-42
6.3.5.1 Troubleshooting Halts Flowcharts............. 6-42
6.3.5.2 PRIMOS Halts................................. 6-46
6.3.5.3 Hardware Diagnostic Status Registers......... 6-48
6.3.5.4 General Machine Check Handling............... 6-54
6.3.6 TROUBLESHOOTING SYSTEM HANGS.......................... 6-55
6.3.7 TROUBLESHOOTING MEMORY PROBLEMS....................... 6-59
6.3.7.1 Handling System Memory Boards................ 6-61
6.3.7.2 ECCC Error Handling Guide.................... 6-61
6.3.7.2.1 Identifying a Failing RAM............... 6-61
6.3.7.2.2 Sample ECCC Error....................... 6-65
6.3.7.3 ECCU Error Handling Guide.................... 6-67
6.3.7.4 Missing Memory Error Handling Guide.......... 6-68
6.3.7.5 Troubleshooting With MEM.TEST8............... 6-68
6.3.7.6 Using MEM.TOOLBOX............................ 6-69
6.3.8 TROUBLESHOOTING DISK/TAPE SUBSYSTEM FAILURES.......... 6-69
6.3.8.1 Troubleshooting Model 4587 Tape Subsystem
Failures... 6-69
6.3.8.1.1 Troubleshooting MSTC Self-Verification
Failures... 6-70
6.3.8.1.2 Using MSTC Status Indicators............ 6-73
6.3.8.1.3 Decoding Tape Drive Status Words........ 6-73
6.3.8.2 Troubleshooting Disk Subsystem Failures...... 6-76
6.3.8.2.1 IDC1 Controller LEDs.................... 6-76
6.3.8.2.2 Disk Status Words....................... 6-78
6.3.8.2.3 Disk Errors Reported by the Disk Driver
Software... 6-82
6.3.9 TROUBLESHOOTING SYSTEM PERFORMANCE DEGRADATION....... 6-84
6.4 TROUBLESHOOTING WITH DIAGNOSTIC MESSAGES AND LEDS.......... 6-88
6.4.1 VCP-V ERROR AND WARNING MESSAGES..................... 6-88
6.4.1.1 VCP-V Self-Verify Messages................... 6-88
6.4.1.2 System Error and Warning Messages............ 6-89
6.4.2 DIAGNOSTIC LEDS ON TLA10113 POWER SUPPLIES...........6-103
6.4.3 DIAGNOSTIC LEDS ON THE IDC1...........................6-104

6.4.4 DIAGNOSTIC LEDS ON THE MSTC..........................6-104
6.4.5 DIAGNOSTIC LEDS ON THE ICS3 CONTROLLER...............6-104
6.4.6 DIAGNOSTIC LEDS ON THE PNC-II........................6-106
6.5 TROUBLESHOOTING WITH DIAGNOSTICS..........................6-109
6.5.1 TROUBLESHOOTING WITH MICRODIAGNOSTICS................6-109
6.5.2 RUNNING THE DIAGNOSTIC TESTING SYSTEM................6-110
6.5.2.1 Applicable DTS Diagnostics..................6-110
6.5.2.2 DTS Diagnostic Monitors.....................6-111
6.5.2.3 Loading and Running DTS From Disk...........6-112
6.5.2.4 Loading and Running DTS From Tape...........6-113
6.5.3 USING REMOTE DIAGNOSTICS.............................6-113

CHAPTER 7. REMOVAL & REPLACEMENT PROCEDURES...................... 7- 1

7.1 SYSTEM POWER-DOWN... 7- 3
7.2 REMOVING AND REPLACING SYSTEM CABINET COVERS............... 7- 3
7.2.1 REMOVING AND REPLACING THE FRONT PANEL............... 7- 4
7.2.1.1 Removing the Front Panel.................... 7- 4
7.2.1.2 Replacing the Front Panel................... 7- 4
7.2.2 REMOVING AND REPLACING THE FLOPPY DISK DRIVE ACCESS DOOR ASSEMBLY... 7- 6
7.2.2.1 Removing the Floppy Disk Drive Access Door Assembly..................................... 7- 6
7.2.2.2 Replacing the Floppy Disk Drive Access Door Assembly..................................... 7- 6
7.2.3 REMOVING AND REPLACING THE TOP COVER................. 7- 6
7.2.3.1 Top Cover Removal........................... 7- 7
7.2.3.2 Replacing the Top Cover..................... 7- 9
7.2.4 REMOVING AND REPLACING THE SIDE COVER................ 7- 9
7.2.4.1 Removing the Side Cover..................... 7- 9
7.2.4.2 Replacing the Side Cover.................... 7- 9
7.2.5 OPENING THE REAR DOOR ASSEMBLY....................... 7-11
7.3 REMOVING AND REPLACING THE CONTROL PANEL................... 7-11
7.3.1 REMOVING THE CONTROL PANEL........................... 7-13
7.3.2 REPLACING THE CONTROL PANEL.......................... 7-13
7.4 REMOVING AND REPLACING BOARD INTERFACE CABLES.............. 7-15
7.4.1 REMOVING A CABLE..................................... 7-15
7.4.2 REPLACING A CABLE.................................... 7-15
7.5 REMOVING AND REPLACING SYSTEM BOARDS....................... 7-17
7.5.1 HANDLING SYSTEM BOARDS............................... 7-17
7.5.2 REMOVING A BOARD..................................... 7-17
7.5.3 REPLACING A BOARD.................................... 7-18
7.6 REMOVING AND REPLACING BOARD RAMS AND PROMS................ 7-20
7.6.1 REMOVING RAMS AND PROMS.............................. 7-20
7.6.2 REPLACING RAM AND PROM............................... 7-20
7.7 REMOVING AND REPLACING SYSTEM POWER SUPPLY FUSES........... 7-20
7.7.1 REMOVING THE POWER SUPPLY FUSE....................... 7-20
7.7.2 REPLACING THE POWER SUPPLY FUSE...................... 7-21
7.8 REMOVING AND REPLACING MODEL TLA10113 POWER SUPPLIES....... 7-21
7.8.1 REMOVING A POWER SUPPLY.............................. 7-21
7.8.2 REPLACING A POWER SUPPLY............................. 7-23
7.9 REMOVING AND REPLACING THE MEMORY BATTERY BACKUP UNIT (MBBU)... 7-24

7.9.1 REMOVING THE MEMORY BATTERY BACKUP UNIT (MBBU)....... 7-24
7.9.2 REPLACING THE MEMORY BATTERY BACKUP UNIT (MBBU)...... 7-24
7.10 REMOVING AND REPLACING THE BLOWER ASSEMBLY................ 7-26
7.10.1 REMOVING THE BLOWER ASSEMBLY......................... 7-26
7.10.2 REPLACING THE BLOWER ASSEMBLY........................ 7-26
7.11 REMOVING AND REPLACING THE AIR FLOW SENSOR................ 7-28
7.11.1 REMOVING THE AIR FLOW SENSOR......................... 7-28
7.11.2 REPLACING THE AIR FLOW SENSOR........................ 7-28
7.12 REMOVING AND REPLACING THE SYSTEM AIR FILTER.............. 7-29
7.12.1 REMOVING THE AIR FILTER.............................. 7-29
7.12.2 REPLACING THE AIR FILTER............................. 7-31
7.13 REMOVING AND REPLACING THE SYSTEM BACKPLANE............... 7-31
7.13.1 REMOVING THE SYSTEM BACKPLANE........................ 7-31
7.13.2 REPLACING THE SYSTEM BACKPLANE....................... 7-33
7.14 REMOVING AND REPLACING THE SYSTEM AC POWER CABLE.......... 7-33
7.14.1 REMOVING THE SYSTEM AC POWER CABLE.................. 7-33
7.14.2 REPLACING THE SYSTEM AC POWER CABLE................. 7-35
7.15 REMOVING AND REPLACING THE POWER DISTRIBUTION UNIT (PDU).. 7-35
7.15.1 REMOVING THE MAINBAY PDU............................. 7-35
7.15.2 MAINBAY PDU REPLACEMENT.............................. 7-37
7.15.3 REMOVING THE PERIPHERAL CABINET PDU................. 7-37
7.15.4 REPLACING THE PERIPHERAL CABINET PDU................ 7-39
7.16 REMOVING AND REPLACING THE FLOPPY DISK DRIVES............. 7-39
7.16.1 REMOVING A FLOPPY DISK DRIVE......................... 7-39
7.16.2 REPLACING A FLOPPY DISK.............................. 7-41
7.17 REMOVING AND REPLACING THE PRIMENET NODE CONTROLLER AND MJ-BOX.. 7-41
7.17.1 REMOVING THE PNC MJ-BOX.............................. 7-41
7.17.2 REPLACING THE PNC MJ-BOX............................. 7-43
7.18 REMOVING AND REPLACING THE ICS3........................... 7-43
7.18.1 REMOVING AND REPLACING THE ICS3 CONTROLLER BOARD.... 7-43
7.18.2 REMOVING AND REPLACING ICS3 LINE ADAPTER CARDS...... 7-43
7.18.2.1 Removing an ICS3 LAC Card.................. 7-44
7.18.2.2 Replacing an ICS3 LAC Card................. 7-45
7.18.3 REMOVING AND REPLACING THE ICS3 BUFFER CARD......... 7-45
7.18.3.1 Removing the ICS3 Buffer Card.............. 7-45
7.18.3.2 Replacing the ICS3 Buffer Card............. 7-46
7.18.4 REMOVING AND REPLACING THE ICS3 LAC BACKPLANE ASSEMBLY.. 7-46
7.18.4.1 Removing the LAC Backplane Assembly......... 7-48
7.18.4.2 Replacing the LAC Backplane Assembly........ 7-49
7.18.5 REMOVING AND REPLACING THE ICS3 POWER SUPPLY........ 7-49
7.18.5.1 Removing the ICS3 Power Supply............. 7-49
7.18.5.2 Replacing the ICS3 Power Supply............ 7-50
7.18.6 REMOVING AND REPLACING THE ICS3 FUSE................ 7-52
7.18.6.1 Removing the ICS3 Power Supply Fuse......... 7-52
7.18.6.2 Replacing the ICS3 Power Supply Fuse........ 7-52
7.18.7 REMOVING AND REPLACING THE ICS3 FAN TRAY ASSEMBLY... 7-54
7.18.7.1 Removing the ICS3 Fan Tray Assembly......... 7-54
7.18.7.2 Replacing the ICS3 Fan Tray................. 7-54
7.19 REMOVING AND REPLACING THE MODEL 4587 TAPE DRIVE.......... 7-56
7.20 REMOVING AND REPLACING THE MODEL 4735 DISK DRIVE (496 MB). 7-56
7.21 REMOVING AND REPLACING THE MODEL 4835 DISK DRIVE (770 MB). 7-56
7.22 SYSTEM PART NUMBERS.. 7-56

TABLE OF CONTENTS

APPENDIX A..A- 1
  1.1 MEMORY CONFIGURATIONS..A- 1
  1.2 SOFTWARE/HARDWARE DEPENDENCIES.................................A- 2
  1.3 I/O CONFIGURATION..A- 3
  1.4 DEVICE ADDRESSES...A- 3
  1.5 BOARD SWITCH SETTINGS..A- 5
  1.6 VCP-V DIAGNOSTIC PROCESSOR CONNECTORS..........................A- 7
  1.7 SAMPLE MAKE COMMAND..A- 7
  1.8 SAMPLE CONFIG FILE...A- 8
  1.9 SAMPLE PRIMOS.COMI FILE..A- 9
  1.10 SUMMARY OF CONTROL PANEL COMMANDS.............................A-10
  1.11 BOOTING INFORMATION...A-11
      1.11.1 SENSE SWITCH BOOT OPTIONS...............................A-11
      1.11.2 BOOT DEVICES..A-12
      1.11.3 DATA SWITCH BOOT OPTIONS................................A-12
      1.11.4 BOOT OPTION WORDS.......................................A-13
  1.12 HALT LOCATIONS..A-14
  1.13 STATUS WORDS..A-15
  1.14 MEMORY DECODE INFORMATION.....................................A-20

FIGURE 1-1: MODEL 4050/4150 COMPUTER SYSTEM 1- 1
FIGURE 1-2: MAJOR SYSTEM ASSEMBLIES 1- 3
TABLE 1-1: MODEL 4050/4150 SOFTWARE REQUIREMENTS 1- 6
TABLE 1-2: MODEL 4050/4150 HARDWARE REQUIREMENTS 1- 6
TABLE 1-3: MODEL 4050/4150 CONFIGURATION GUIDELINES 1- 7
TABLE 1-4: MODEL 4050/4150 GENERAL SPECIFICATIONS 1- 7
TABLE 1-5: MODEL 4050/4150 ELECTRICAL SPECIFICATIONS 1- 8
TABLE 1-6: MODEL 4050/4150 ENVIRONMENTAL SPECIFICATIONS 1- 8
TABLE 1-7: MODEL 4050/4150 PHYSICAL SPECIFICATIONS 1- 9
TABLE 1-8: MODEL 4050/4150 RELATED DOCUMENTATION 1- 9
FIGURE 1-3: EQUIPMENT IDENTIFICATION PLATE 1-11
TABLE 1-9: MODEL 4050/4150 MARKETING MODEL NUMBERS 1-12
TABLE 1-10: MODEL 4050/4150 OPTION MODEL NUMBERS 1-14

FIGURE 2-1: MAJOR INSTALLATION ACTIVITIES 2- 2
TABLE 2-1: MODEL 4050/4150 MAINBAY CABINET ELECTRICAL SPECIFICAT 2- 3
TABLE 2-2: MODEL 4050/4150 PERIPHERAL BAY ELECTRICAL SPECIFICATI 2- 4
TABLE 2-3: MODEL 4050/4150 ENVIRONMENTAL SPECIFICATIONS 2- 4
TABLE 2-4: OPERATING SPECIFICATIONS: DC DRAW PER I/O CONTROLLER AND MEMORY BOARD 2- 4
FIGURE 2-2: MAINBAY CABINET UNPACKING 2- 7
FIGURE 2-3: PERIPHERAL CABINET UNPACKING 2- 8
TABLE 2-5: MODEL 4050/4150 AC POWER CABLE PART NUMBERS 2- 9
FIGURE 2-4: MODEL PLATE LOCATION 2-10
FIGURE 2-5: AC CONNECTOR VERIFICATION 2-11
FIGURE 2-6: TLA10113 VOLTAGE VERIFICATION 2-13
FIGURE 2-7: BATTERY BACKUP UNIT FRONT PANEL 2-13
TABLE 2-6: KIT10035-001 (120 V TO 240 V) CONTENTS 2-14
TABLE 2-7: KIT10036-001 (240 V TO 120 V) CONTENTS 2-14
FIGURE 2-8: TLA10113 VOLTAGE CONVERSION 2-15
FIGURE 2-9: CARD CAGE CONFIGURATION 2-18
FIGURE 2-10: SYSTEM INTERCONNECTION DIAGRAM 2-20
FIGURE 2-11: PDU FRONT PANEL 2-21
FIGURE 2-12: MAINBAY/PERIPHERAL BAY PDU CABLING 2-22
FIGURE 2-13: PDU INTERCONNECTION DIAGRAM 2-24
FIGURE 2-14: TLA10113 SHIPPING RESTRAINT REMOVAL 2-26
FIGURE 2-15: MBBU INSTALLATION 2-27
FIGURE 2-16: DIAGNOSTIC PROCESSOR (VCP-V) SWITCHES............. 2-30
TABLE 2-8: DIAGNOSTIC PROCESSOR (VCP-V) OPTION SWITCH A SETTINGS 2-31
TABLE 2-9: VCP-V OPTION SWITCH B SETTINGS 2-32
TABLE 2-9A: VCP-V SWITCH 3 SETTINGS 2-32
FIGURE 2-17: VCP-V EDGE CONNECTORS 2-34
TABLE 2-10: VCP-V EDGE CONNECTORS AND CABLES 2-35
FIGURE 2-18: SYSTEM CONSOLE PORT 2-36
TABLE 2-11: I/O CONTROLLER PRIORITY: BASIC ORDER 2-38
FIGURE 2-19: SYSTEM BULKHEADING 2-39
FIGURE 2-20: PERIPHERAL CABINET ZONE DESIGNATIONS 2-40
TABLE 2-12: PERIPHERAL CABINET CONFIGURATION GUIDE 2-41
TABLE 2-13: CONTROLLER DEVICE ADDRESSES 2-42
TABLE 2-13: CONTROLLER DEVICE ADDRESSES (CONT.) 2-43
TABLE 2-14: CONTROLLER ADDRESS/JUMPER CONFIGURATION 2-44
FIGURE 2-21: IDC1 CONFIGURATION 2-45
FIGURE 2-22: IDC1 CABLING 2-47
FIGURE 2-23: MSTC CONFIGURATION 2-49
FIGURE 2-24: MSTC CABLING 2-51

TABLE 2-15: ICS3 DEVICE ADDRESSES (OCTAL) 2-53
FIGURE 2-25: ICS3 CONTROLLER CONFIGURATION 2-54
TABLE 2-16: DEVICE ADDRESS DIP SETTINGS 2-55
TABLE 2-17: ICS3 BUFFER CARD APPLICATIONS 2-55
FIGURE 2-26: ICS3 BUFFER CARD CONFIGURATION 2-56
FIGURE 2-27: ICS3 LAC BACKPLANE CONFIGURATION 2-57
FIGURE 2-28: ICS3 MAINBAY CABLING DIAGRAM 2-59
FIGURE 2-29: ICS3 PERIPHERAL BAY CABLING 2-60
FIGURE 2-30: ICS2 CARD CAGE INSTALLATION (MAINBAY) 2-61
FIGURE 2-31: ICS3 CARD CAGE POWER CABLING 2-63
FIGURE 2-32: PERIPHERAL BAY REAR PANEL REMOVAL 2-64
TABLE 2-18: MOUNTING RAIL HOLE LOCATIONS 2-65
FIGURE 2-33: ICS3 CARD CAGE INSTALLATION (PERIPHERAL BAY) 2-66
FIGURE 2-34: 53-INCH PERIPHERAL BAY COVER PLATE REMOVAL 2-67
FIGURE 2-35: ICS3 CARD CAGE INSTALLATION (53-INCH PERIPHERAL BAY) 2-68
FIGURE 2-36: ICS3 LAC PRIORITY 2-70
FIGURE 2-37: ICS3 LAC INSTALLATION 2-70
TABLE 2-19: ICS3 CARD CAGE TRANSFER KIT KIT10159-001 PARTS 2-71
FIGURE 2-38: ICS3 DEVICE CABLING 2-72
FIGURE 2-39: EXHAUST DUCT COVER INSTALLATION 2-74
TABLE 2-20: ICS3 CARD CAGE TRANSFER KIT KIT10173-001 PARTS 2-75
TABLE 2-21: ICS3 CARD CAGE TRANSFER KIT KIT10217-001 PARTS 2-76
TABLE 2-22: ICS3 CARD CAGE TRANSFER KIT KIT10174-001 PARTS 2-77
FIGURE 2-40: PNC-II CABLING 2-80
FIGURE 2-41: PNC MJ-BOX INSTALLATION 2-81
FIGURE 2-42: 496MB DISK DRIVE POWER VERIFICATION 2-83
FIGURE 2-43: I/O SHIELD REMOVAL 2-84
FIGURE 2-44: 496MB DISK DRIVE CABLING 2-85
TABLE 2-23: 496MB DISK DRIVE MOUNTING HARDWARE 2-87
FIGURE 2-45: T-BAR ASSEMBLY 2-89
FIGURE 2-46: MOUNTING THE T-BAR 2-90
TABLE 2-24: CABINET FRONT/REAR RAIL MEASUREMENTS 2-90
FIGURE 2-47: INSTALLING THE RAILS 2-91
FIGURE 2-48: INSTALLING FILLER PANEL 2-93
FIGURE 2-49: 770MB DISK DRIVE VOLTAGE VERIFICATION 2-97
FIGURE 2-50: 770MB DISK DRIVE CABLING 2-98
TABLE 2-25: 770MB DISK DRIVE MOUNTING HARDWARE PARTS 2-100
FIGURE 2-51: ASSEMBLING THE TRAY 2-102
TABLE 2-26: 7730H CABINET NUT BAR MEASUREMENTS 2-103
FIGURE 2-52: SECURING THE TRAY TO THE CABINET 2-104
TABLE 2-27: 7730H CABINET NUT CLIP MEASUREMENTS 2-105
FIGURE 2-53: INSTALLING TRIM AND FILLER PANELS 2-106
FIGURE 2-54: DISTRIBUTION PANEL CABLING 2-107
FIGURE 2-55: QUAD-DENSITY TAPE DRIVE VOLTAGE VERIFICATION 2-110
FIGURE 2-56: QUAD-DENSITY TAPE DRIVE CABLING 2-111
FIGURE 2-57: ICS1 CABLING 2-112
FIGURE 2-58: AMLC CABLING 2-113
FIGURE 2-59: MDLC CABLING 2-114
FIGURE 2-60: CIPHER STREAMER CABLING (30-INCH PERIPHERAL BAY) ... 2-115
FIGURE 2-61: CIPHER STREAMER CABLING (53-INCH PERIPHERAL BAY) ... 2-116
FIGURE 2-62: GCR CABLING 2-117
FIGURE 2-63: DEI CARTRIDGE TAPE CABLING 2-118
FIGURE 2-64: KENNEDY MTT CABLING 2-119
FIGURE 2-65: REMOTE CARTRIDGE TAPE CABLING 2-120
FIGURE 2-66: 4005 DISK CONTROLLER CABLING 2-121
FIGURE 2-67: URC CABLING 2-122
FIGURE 2-68: LHC CABLING 2-123

FIGURE 2-69: MPC-4 CABLING 2-124
FIGURE 2-70: BULKHEAD PANEL TAPES 2-128

TABLE 3-1: SYSTEM STATUS PANEL CONTROLS 3- 2
FIGURE 3-1: SYSTEM STATUS PANEL 3- 4
TABLE 3-2: STATUS PANEL INDICATORS 3- 5
FIGURE 3-2: MAINBAY POWER DISTRIBUTION UNIT 3- 6
FIGURE 3-3: TLA10113 POWER SUPPLY LEDS 3- 7
TABLE 3-3: TLA10113 POWER SUPPLY LEDs 3- 7
FIGURE 3-4: MODEL 4735 DISK DRIVE CONTROLS AND INDICATORS 3- 9
FIGURE 3-5: MODEL 4835 DISK DRIVE CONTROLS AND INDICATORS 3-10
FIGURE 3-6: MODEL 4587 TAPE DRIVE CONTROLS AND INDICATORS 3-11
FIGURE 3-7: PNC-II BOARD LEDS 3-13
TABLE 3-4: PNC-II BOARD LEDS 3-13
TABLE 3-5: MJ-BOX LEDS 3-14
FIGURE 3-8: PNC MJ-BOX CONTROLS AND INDICATORS 3-15
TABLE 3-6: ICS3 CONTROLLER BOARD LEDS 3-16
FIGURE 3-9: ICS3 CONTROLLER LEDS 3-17
FIGURE 3-10: ICS3 LEDS 3-18
TABLE 3-7: OTHER SYSTEM AND BOARD INDICATORS 3-19
FIGURE 3-11: FLOPPY DISK DRIVES 3-20
FIGURE 3-12: POWER-UP MESSAGE SEQUENCE 3-23
FIGURE 3-13: SAMPLE STATUS DISPLAY 3-36
TABLE 3-8: DIAGNOSTIC PROCESSOR MESSAGE (DPM) SUMMARY 3-43
TABLE 3-9: SENSE SWITCH BOOT DEVICE OPTIONS 3-47
TABLE 3-10: COMMON BOOT OPTION WORDS 3-48
TABLE 3-11: MTRESUME COMMAND LINE OPTIONS 3-52
TABLE 3-12: NEW PRIMOS REVISION 21 COMMANDS 3-61
TABLE 3-13: START_DSM COMMAND OPTIONS 3-63
TABLE 3-14: DSM COMMANDS 3-63
TABLE 3-15: STOP_DSM OPTIONS 3-64

FIGURE 4-1: MODEL 4050/4150 SYSTEM BLOCK DIAGRAM 4- 2
FIGURE 4-2: MODEL 4050/4150 CPU BLOCK DIAGRAM 4- 3
TABLE 4-1: 4050/4150 CPU FUNCTIONAL OVERVIEW 4- 4
FIGURE 4-3: IS BOARD BLOCK DIAGRAM 4- 5
FIGURE 4-4: E BOARD BLOCK DIAGRAM 4-10
TABLE 4-2: ALU DATA SOURCES 4-11
FIGURE 4-5: CMI BOARD BLOCK DIAGRAM 4-13
FIGURE 4-6: MEMORY ARRAY LOCATIONS 4-22
FIGURE 4-7: MEMORY ARRAY BLOCK DIAGRAM 4-23
TABLE 4-3: INPUT CONTROLS 4-24
TABLE 4-4: OUTPUT CONTROL SIGNALS 4-24
FIGURE 4-8: I/O CONTROLLER FUNCTIONAL COMPONENTS 4-27
FIGURE 4-9: PNC-II BOARD LAYOUT 4-32
TABLE 4-5: PNC-II INITIALIZATION EVENTS 4-37
FIGURE 4-10: VCP-V BLOCK DIAGRAM 4-40
TABLE 4-6: REMOTE TERMINAL LED DEFINITIONS 4-44
FIGURE 4-11: MICROCODE DISKETTE DISPLAY 4-47
TABLE 4-7: MICROCODE FILE TYPES 4-47
TABLE 4-8: ENVIRONMENTAL SENSOR SUMMARY 4-49
TABLE 4-9: UPS CONNECTOR PINOUT 4-53
TABLE 4-10: BBU SIGNAL DEFINITIONS 4-54
TABLE 4-11: POWER SUPPLY NUMBERING CONVENTIONS 4-55
TABLE 4-12: MARGIN SIGNALS TRUTH TABLE 4-60
FIGURE 4-12: TLA10113 POWER SUPPLY SCHEMATIC 4-73
FIGURE 4-13: TLA10113 POWER SUPPLY FRONT PANEL 4-74

TABLE 4-13: POWER SUPPLY LED VOLTAGES 4-76
TABLE 4-14: FLOPPY DISK POWER REQUIREMENTS 4-78
FIGURE 4-14: SYSTEM BLOWER 4-79
FIGURE 4-15: COOLING SYSTEM DIAGRAM 4-80
FIGURE 4-16: BLOWER BYPASS SWITCH 4-81
TABLE 4-15: BLOWER POWER CABLE PIN ASSIGNMENTS 4-82
FIGURE 4-17: DSM HIERARCHY 4-84

FIGURE 5-1: CUSTOMER SERVICE HISTORY DISK 5- 3
FIGURE 5-2: REV. 21 AND PRE-REV. 21 EVENT LOGGERS 5- 5
FIGURE 5-3: PRINT_SYSLOG SAMPLE FILE 5- 6
TABLE 5-1: PRINT_SYSLOG AND PRINT_NETLOG OPTIONS 5- 7
TABLE 5-2: SYSTEM EVENT TYPES 5- 8
FIGURE 5-4: PRINT_NETLOG SAMPLE FILE 5-10
TABLE 5-3: NETWORK EVENT TYPES 5-11
FIGURE 5-5: LOGREC FILE SAMPLE 5-12
FIGURE 5-6: NETREC FILE SAMPLE 5-13
TABLE 5-4: INDEX OF MANUALS 5-14
FIGURE 5-7: SAMPLE PM SCHEDULE 5-16

FIGURE 6-1: HOW TO USE THE TROUBLESHOOTING CHAPTER 6- 1
FIGURE 6-2: CATEGORIZING THE PROBLEM (F0) 6- 4
TABLE 6-1: TROUBLESHOOTING FLOWCHART INDEX 6- 6
FIGURE 6-3: AC POWER PROBLEMS FLOWCHART (F1) 6- 7
TABLE 6-2: AC POWER PROBLEMS (F1) 6- 9
FIGURE 6-4: POWER UP PROBLEMS FLOWCHRT (F2) 6-10
TABLE 6-3: POWER-UP SEQUENCE PROBLEMS (F2) 6-12
FIGURE 6-5: VERIFYING AC MAINS VOLTAGE 6-14
FIGURE 6-6: MEASURING BACKPLANE VOLTAGE 6-16
FIGURE 6-7: CPU VERIFICATION FAILURE FLOWCHART (F3) 6-17
TABLE 6-4: CPU VERIFICATION FAILURE (F3) 6-18
FIGURE 6-8: CPU INITIALIZATION FAILURE FLOWCHART (F4) 6-18
TABLE 6-5: CPU INITIALIZATION FAILURE (F4) 6-19
FIGURE 6-9: CPBOOT FAILURE FLOWCHART (F5) 6-20
TABLE 6-6: CPBOOT FAILURES (F5) 6-21
FIGURE 6-10: COLDSTART FAILURE FLOWCHART (F6) 6-22
TABLE 6-7: COLDSTART FAILURES (F6) 6-23
TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS 6-24
TABLE 6-9: BOOT HALT LOCATION CODE NUMBERS 6-29
TABLE 6-10: BOOT.SAVE ERROR MESSAGES 6-31
TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES 6-33
FIGURE 6-11: POWER/ENVIRONMENTAL/VCP FAILURE FLOWCHART (F7) 6-39
TABLE 6-12: POWER/ENVIRONMENTAL/VCP FAILURES DURING OPERATION (F7 6-40
TABLE 6-13: TLA10113 POWER SUPPLY SPECIFICATIONS 6-41
TABLE 6-14: TLA10113 POWER SUPPLY RIPPLE 6-42
FIGURE 6-12: SYSTEM HALTS FLOWCHART (F8) 6-43
FIGURE 6-13: ISOLATING SYSTEM HALTS FLOWCHART (F8-A) 6-44
TABLE 6-15: SYSTEM HALTS (F8) 6-45
TABLE 6-16: ISOLATING SYSTEM HALTS (F8-A) 6-46
TABLE 6-17: PRIMOS SYSTEM HALTS 6-47
TABLE 6-18: FORMAT OF DSWPARITY REGISTER: HIGH SIDE 6-49
TABLE 6-19: FORMAT OF DSWPARITY REGISTER: LOW SIDE 6-50
TABLE 6-20: FORMAT OF DSWPARITY2 REGISTER: HIGH SIDE 6-50
TABLE 6-21: FORMAT OF DSWPARITY2 REGISTER: LOW SIDE 6-51
TABLE 6-22: FORMAT OF DSWSTAT REGISTER: HIGH SIDE 6-52
TABLE 6-23: FORMAT OF DSWSTAT REGISTER: LOW SIDE 6-53
FIGURE 6-14: SYSTEM HANGS FLOWCHART (F9) 6-55

FIGURE 6-15: DETERMINING IF SYSTEM IS REALLY HUNG (F10) 6-56
TABLE 6-24: SYSTEM HANGS (F9) 6-57
TABLE 6-25: DETERMINING IF THE SYSTEM IS REALLY HUNG (F10) 6-58
FIGURE 6-16: MEMORY PROBLEMS FLOWCHART (F11) 6-59
TABLE 6-26: MEMORY PROBLEMS (F11) 6-59
FIGURE 6-17: MMW3-8MB DECODE CHART 6-62
FIGURE 6-18: MMW3-8MB BIT MAP 6-63
FIGURE 6-19: MEMORY ECCC ERROR 6-64
TABLE 6-27: MMW3 BIT IN ERROR DECODE TABLE 6-65
TABLE 6-28: MSTC DIAGNOSTIC LED TRUTH TABLE 6-69
FIGURE 6-20: MSTC CONTROLLER LEDS 6-70
TABLE 6-29: MSTC SELF-VERIFICATION TEST LED DESCRIPTIONS 6-71
TABLE 6-30: MSTC SCSI INTERFACE LED DESCRIPTIONS 6-72
TABLE 6-31: TAPE STATUS WORD I BREAKDOWN 6-73
TABLE 6-32: TAPE STATUS WORD II BREAKDOWN 6-74
FIGURE 6-21: IDC1 CONTROLLER LEDS 6-75
TABLE 6-33: CONTROLLER BOARD STATUS INDICATORS 6-76
TABLE 6-34: POWER-UP SELF-VERIFY FAILURE REPORTS 6-76
TABLE 6-35: OPERATIONAL ERROR CONDITIONS 6-77
TABLE 6-36: DISK STATUS WORDS 6-78
TABLE 6-37: COMMON DISK ERRORS 6-82
FIGURE 6-22: SLOW SYSTEM FLOWCHART A (F12-A) 6-84
FIGURE 6-23: SLOW SYSTEM FLOWCHART B (F12-B) 6-85
FIGURE 6-24: SLOW SYSTEM FLOWCHART C (F12-C) 6-85
TABLE 6-38: SLOW SYSTEM - STEP A (F12-A) 6-86
TABLE 6-39: SLOW SYSTEM - STEP B (F12-B) 6-86
TABLE 6-40: SLOW SYSTEM - STEP C (F12-C) 6-87
TABLE 6-41: VCP-V LED MESSAGES 6-88
TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS 6-89
TABLE 6-43: VCP-V WARNING CODES AND CORRECTIVE ACTIONS 6-100
FIGURE 6-25: TLA10113 POWER SUPPLY LEDS 6-103
TABLE 6-44: SYSTEM POWER SUPPLY LEDs 6-103
FIGURE 6-26: ICS3 CONTROLLER LEDS 6-104
TABLE 6-45: ICS3 COLDSTART LED ERRORS 6-105
TABLE 6-46: ICS3 STATUS LED ERRORS 6-106
TABLE 6-47: PNC-II PCB NETWORK STATUS LEDS 6-106
FIGURE 6-27: PNC-II CONTROLLER AND MJ-BOX LEDS 6-107
TABLE 6-48: PNC-II LED ERROR CODES 6-108
TABLE 6-49: MJ-BOX LED STATES 6-108
TABLE 6-50: SYSTEM DIAGNOSTICS 6-111
TABLE 6-51: DTS MONITORS 6-112

FIGURE 7-1: MODEL 4050/4150 EXPLODED VIEW 7- 2
FIGURE 7-2: FRONT PANEL REMOVAL 7- 5
FIGURE 7-3: FLOPPY DRIVE ACCESS DOOR REMOVAL 7- 7
FIGURE 7-4: TOP COVER REMOVAL 7- 8
FIGURE 7-5: SIDE COVER REMOVAL 7-10
FIGURE 7-6: REAR DOOR ASSEMBLY 7-12
FIGURE 7-7: CONTROL PANEL REMOVAL 7-14
FIGURE 7-8: BOARD INTERFACE CABLE REMOVAL 7-16
FIGURE 7-9: BOARD REMOVAL 7-19
FIGURE 7-10: TLA10113 POWER SUPPLY FUSE REMOVAL 7-21
FIGURE 7-11: POWER SUPPLY LOCATIONS 7-22
FIGURE 7-12: TLA10113 POWER SUPPLY REMOVAL 7-23
FIGURE 7-13: MBBU REMOVAL 7-25
FIGURE 7-14: BLOWER ASSEMBLY REMOVAL 7-27
FIGURE 7-15: AIR FLOW SENSOR REMOVAL 7-29

FIGURE 7-16: AIR FILTER REMOVAL 7-30
FIGURE 7-17: BACKPLANE REMOVAL 7-32
FIGURE 7-18: AC POWER CABLE REMOVAL 7-34
FIGURE 7-19: MAINBAY PDU REMOVAL 7-36
FIGURE 7-20: PERIPHERAL BAY PDU REMOVAL 7-38
FIGURE 7-21: FLOPPY DISK DRIVE REMOVAL 7-40
FIGURE 7-22: MJ BOX REMOVAL 7-42
FIGURE 7-23: ICS3 LAC REMOVAL 7-44
FIGURE 7-24: ICS3 BUFFER CARD/LAC BACKPLANE REMOVAL 7-47
FIGURE 7-25: ICS3 POWER SUPPLY REMOVAL 7-51
FIGURE 7-26: ICS3 POWER SUPPLY FUSE REMOVAL 7-53
FIGURE 7-27: ICS3 FAN TRAY REMOVAL 7-55
TABLE 7-1: MODEL 4050/4150 PART NUMBERS 7-56
TABLE 7-2: MODEL 4050/4150 CABLE PART NUMBERS 7-59

TABLE A-1: MEMORY CONFIGURATIONS FOR MODELS 4050 & 4150 SYSTEMS..A- 1
TABLE A-2: MODEL 4050/4150 SOFTWARE REQUIREMENTS.................A- 2
TABLE A-3: MODEL 4050/4150 HARDWARE REQUIREMENTS.................A- 2
TABLE A-4: MODELS 4050 & 4150 I/O CONTROLLER PRIORITY:
BASIC ORDER.......................................A- 3
TABLE A-5: DEVICE ADDRESSES......................................A- 3
TABLE A-6: DIAGNOSTIC PROCESSOR (VCP-V) OPTION SWITCH SETTINGS...A- 5
TABLE A-7: VCP-V OPTION SWITCH B SETTINGS........................A- 6
TABLE A-7A: VCP-V SWITCH OPTION 3 SETTINGS.......................A- 6
TABLE A-8: VCP-V EDGE CONNECTORS AND CABLES......................A- 7
TABLE A-9: RECOMMENDED MAKE COMMAND OPTIONS......................A- 8
TABLE A-10: MODELS 4735 AND 4784 DISK DRIVES DESCRIPTION.........A- 8
TABLE A-11: SUMMARY OF CONTROL PANEL COMMANDS....................A-10
TABLE A-12: SENSE SWITCH BOOT DEVICE OPTIONS.....................A-12
TABLE A-13: COMMONLY-USED BOOT OPTION WORDS......................A-13
TABLE A-14: PRIMOS SYSTEM HALTS..................................A-14
TABLE A-15: FORMAT OF DSWPARITY REGISTER: HIGH SIDE..............A-15
TABLE A-16: FORMAT OF DSWPARITY REGISTER: LOW SIDE...............A-16
TABLE A-17: FORMAT OF DSWPARITY2 REGISTER: HIGH SIDE.............A-17
TABLE A-18: FORMAT OF DSWPARITY2 REGISTER: LOW SIDE..............A-18
TABLE A-19: FORMAT OF DSWSTAT REGISTER: HIGH SIDE................A-19
TABLE A-20: FORMAT OF DSWSTAT REGISTER: LOW SIDE.................A-19
TABLE A-21: MMW3 BIT IN ERROR DECODE TABLE.......................A-20
FIGURE A-1: MMW3 DECODE CHART....................................A-21
FIGURE A-2: MMW3 BIT MAP..A-22
FIGURE A-3: WIRING DIAGRAM.......................................A-23

CHAPTER 1
GENERAL DESCRIPTION

The Model 4050 and Model 4150 Computer Systems are high-performance, office-installable TTL super-minicomputers with 10-stage synchronous pipeline architecture. The Model 4050/4150 system is shown with a matching option bay in Figure 1-1. Both models are targeted as high-end office products and as entry-level computer room machines. The 4050 offers higher performance than its predecessor in the product line, the 2755. The 4150 replaces the 9755 in the product line, offering the same performance but at lower cost. A three-board central processor with space-saving Very Large Scale Integration (VLSI) components is packaged in a newly-styled 30-inch "lowboy" cabinet. Peripheral devices, including the new quad-density tape drive and 496MB or 770MB fixed disk drives, are housed in a matching option bay.

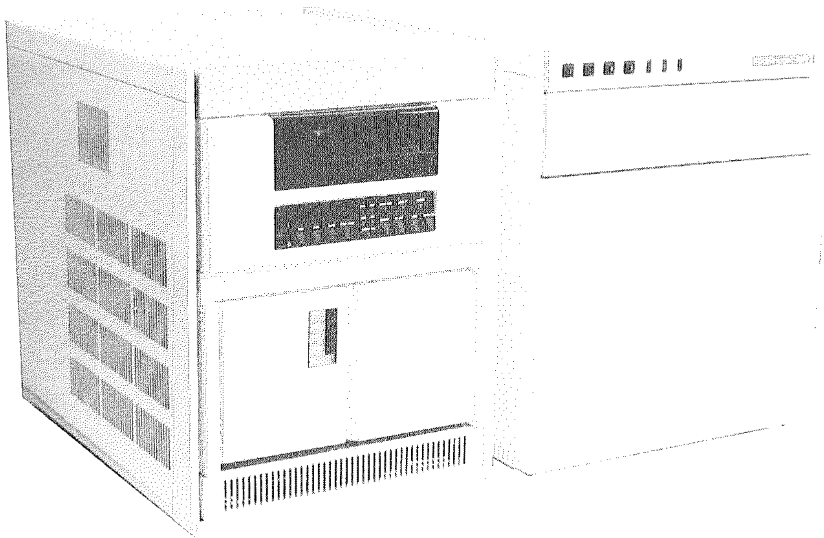


FIGURE 1-1: MODEL 4050/4150 COMPUTER SYSTEM

1.1 MODEL 4050/4150 NEW FEATURES

Model 4050 and 4150 Computer Systems offer the following new features:

- Vertically-mounted circuit boards and power supplies accessible from the front of the system.
- Two-way set associative 128 Kb cache with soft error recovery.
- Dual floppy disk drives for microcode storage and history log file support.
- 8MB (32MB max.) memory array boards.
- A single-board VCP-V Diagnostic Processor.
- Optional Battery Backup Unit for extensive ride-through of main memory.
- Processor Diagnostic Aid (PDA) support.
- High-efficiency, low-noise, speed-controlled cooling system.
- Two ILA10113 power supplies.
- Support for all currently-marketed I/O controllers (maximum of 10 slots).
- Support for ICS3 Sr. subsystem in either mainbay or peripheral cabinet.

1.2 SYSTEM OVERVIEW

This section briefly describes the following hardware components that are standard with the Model 4050/4150 system:

- CPU Board Set
- VCP-V Diagnostic Processor
- Model MMW3-8MB, MMW3-16MB, or MMW3-32MB Memory Array Board
- Status Panel
- Power Supplies
- Blower Assembly
- Tilt Bulkhead
- Power Distribution Unit

Refer to Figure 1-2 for the location of major system assemblies and components.

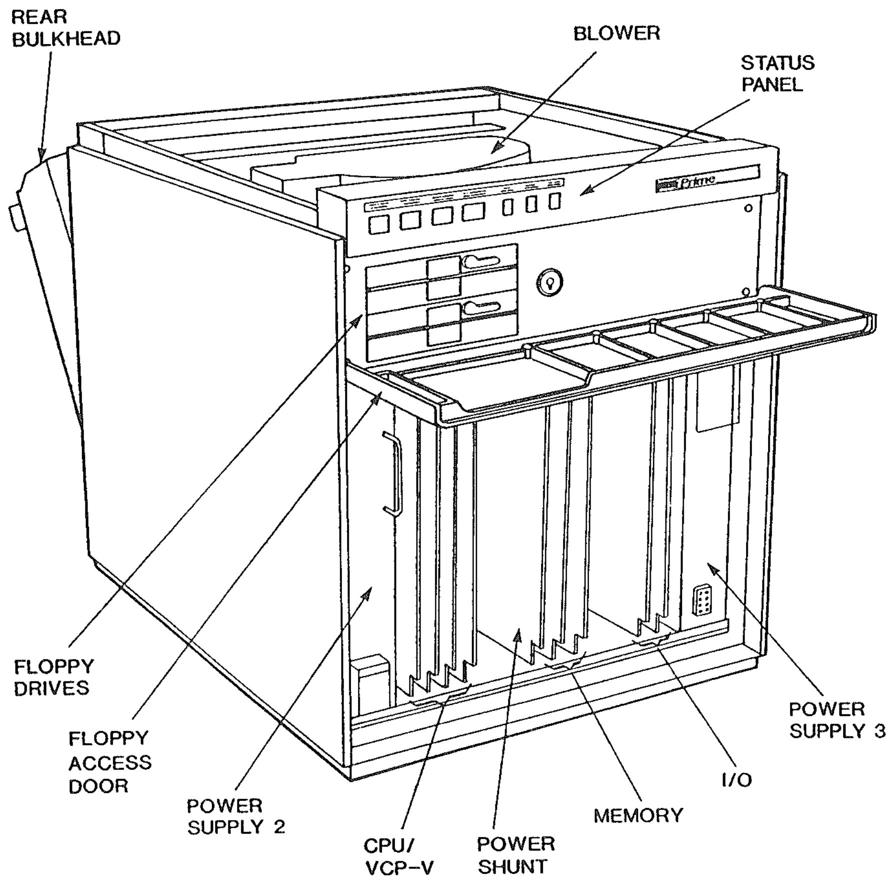


FIGURE 1-2: MAJOR SYSTEM ASSEMBLIES

1.2.1 CPU BOARD SET

Each Central Processor consists of three boards based on the pipeline architecture of earlier Prime ECL-based systems. VLSI components provide faster and more reliable performance with the use of less board space.

New features of each processor include two-way set associative cache, two-way set associative 1K entry Segment Table Lookaside Buffer (STLB), an associative write buffer, improved floating point hardware and algorithms, and soft and hard error recovery in cache and STLB.

A summary of the board functions are as follows:

- E-Unit - Execution Unit, I/O Address Interface

- CMI-Unit - Control Store, Memory Interface, and I/O Data Interface

- IS Unit - Prefetch, Cache/STLB, PCU

Part numbers for each three-board CPU board set are as follows:

- Model 4050: TLA10290-001

- Model 4150: TLA10104-001

1.2.2 VCP-V DIAGNOSTIC PROCESSOR

The VCP-V Diagnostic Processor is a 15-inch board housed in the CPU card cage. The hardware and software functionality of the VCP-V is very similar to its predecessors, the VCP-III and VCP-IV. This includes support for a system console, user mode terminal, remote system terminal, an interface to the CPU, loadable control store support, system ID PROM, time of day clock, microdiagnostics, status panel interface, environmental sensing, and VCP functions.

1.2.3 MODEL MMW3-8MB, MMW3-16MB, and MMW3-32MB MEMORY ARRAY BOARDS

The maximum memory allowed in the 4050 and 4150 is 32MB regardless of the PRIMOS revision.

Error checking and correction on all memory transfers are performed by the CPU MC board and CMI board, rather than the memory array boards.

1.2.4 STATUS PANEL

The Model 4050/4150 features a status panel that provides operating mode information and control via momentary and toggle switches and LEDs. Refer to Status Panel Controls and Indicators in Chapter 3 of this manual for operating information.

1.2.5 POWER SUPPLIES

Model 4050/4150 power is controlled by two TLA10113 power supplies and an optional Model 7300HG memory battery backup unit (MBBU).

PS1, the MBBU, provides memory ridethrough and power for the VCP-V and the CMI board during brief power failures or glitches. If a MBBU is not present, a power shunt board replaces this power supply to divert power from PS2.

PS2, the CPU power supply, provides power to the central processor, and the processor diagnostic aid (PDA), if present.

PS3, the I/O power supply, provides power to four memory slots and 10 I/O slots.

1.2.6 BLOWER ASSEMBLY

The Model 4050/4150 is cooled by a 24 Vdc, 340 cubic feet per minute variable speed blower. The blower features temperature-dependent speed control that automatically senses changes in cabinet temperature and increases or decreases blower speed accordingly.

1.2.7 TILT BULKHEAD

The Model 4050/4150 is equipped with a rear tilt bulkhead, which provides easy access to Power Distribution Unit connectors and the system backplane. By unlocking two quarter-turn screws, the bulkhead tilts 45 degrees. The bulkhead tilts a full 90 degrees by also disconnecting two support wires.

1.2.8 POWER DISTRIBUTION UNIT

The Power Distribution Unit (PDU) features two-phase sequencing that that is controlled by the VCP-V. Power supply and peripheral device connections are accessible through the tilt bulkhead without removing the PDU. A lamp indicates that power is present at the mainbay cabinet.

1.3 OPTIONAL COMPONENTS

The Model 4050/4150 can be ordered standard with the following optional disk, tape, and communications devices:

- Model 4735 Disk Drive - A 496 megabyte high-speed, random-access, digital data Fixed Module Disk controlled by the Model 6850 Intelligent Disk Controller.

- Model 4835 Disk Drive - A 770 megabyte high-speed, random-access, digital data Fixed Module Disk controlled by the Model 6850 Intelligent Disk Controller.

- Model 4587 Tape Drive - A rack-mounted automatic-load tape drive that can operate at four recording densities: 800, 1600, 3200, and 6250 CPI. The device is controlled by a Model 2382-003 SCSI Tape Controller. This device must be ordered separately.

- Intelligent Communications Subsystem Model 3 - The system supports the ICS3 controller and 16-slot cardcage in either the mainbay or peripheral cabinet.

1.4 SOFTWARE/HARDWARE DEPENDENCIES

Model 4050 and 4150 software dependencies are listed in Table 1-1. Hardware requirements are listed in Table 1-2.

TABLE 1-1: MODEL 4050/4150 SOFTWARE REQUIREMENTS

MODEL	MINIMUM PRIMOS REV.
4050	20.2.6 21.0.2S
4150	20.2.5 21.0.1

NOTE

Both the Model 4050 and Model 4150 support all currently-marketed 50 Series controllers and peripheral devices. All system boards must be at their latest revision level. Minimum board revision requirements are listed in Table 1-2.

TABLE 1-2: MODEL 4050/4150 HARDWARE REQUIREMENTS

BOARD NAME	MODEL NUMBER	PART NUMBER	MINIMUM REVISION
IDC1	6580	TLA10019-001	R
MSTC	2382-003	TLA10234-001	B
MPC4	7010T	SPL91521-91	H
8MB MEMORY	MMW3-8MB	TLA10088-001	C
STSC		2301-901	AA
ASYNC LAC	CLAC304	ESA10063-001	C
BMTC		2023-901	N

1.5 CONFIGURATION GUIDELINES

Model 4050/4150 configuration guidelines are listed in Table 1-3.

TABLE 1-3: MODEL 4050/4150 CONFIGURATION GUIDELINES

DESCRIPTION	VALUE 4050	4150
Memory (MAX.)	32 Mb	32 Mb
Asynchronous Lines	128	254
ICS3s	2	4
AMLCs	2	2
Synchronous Lines	8	8
Disk Drives	8*	16*
Disk Controllers	2	4
Tape Drives	8	8
Tape Controllers	2	2
4592 Tri-Density Tape	NO	YES
Line Printers	4 (2 URCs)	4 (2 URCs)
LAN300 Controllers	6	6

* Due to acoustic noise emission, the maximum number of disk drives in an office environment should not exceed four.

1.6 SPECIFICATIONS

Table 1-4 lists Model 4050/4150 general specifications.

TABLE 1-4: MODEL 4050/4150 GENERAL SPECIFICATIONS

DESCRIPTION	VALUE 4050	4150
Processor (number of boards)	3	3
CPU Clock Speed	34.5 nsec 30 MHz	31.25 nsec 32 MHz
Memory Type	MMW3-8MB	MMW3-8MB
Memory Cycle Time	1550 nsec	1460 nsec
Memory Access Time	84 nsec	77 nsec

*Performance is application dependent.

TABLE 1-4: MODEL 4050/4150 GENERAL SPECIFICATIONS (CONT.)

DESCRIPTION	VALUE 4050	4150
Cache Memory	128 Kb	128 Kb
Cache Cycle Time	69 nsec	62.5 nsec
Virtual Address Space	512 mb	512 mb
Performance*	2.8 MIPs	4.1 MIPs

* Performance is application dependent.

Table 1-5 lists Model 4050/4150 electrical specficiations

TABLE 1-5: MODEL 4050/4150 ELECTRICAL SPECIFICATIONS

DESCRIPTION	DOMESTIC	INTERNATIONAL
Voltage (ac)	120 V, (90-132)	240 V (180-264)
Frequency (Hz)	60 (59-61)	50 (49-51)
Phase	4-wire	3-wire
AC Plug	NEMA L14-20	Unterminated
Consumption	.918 kVA	1.96 kVA
Start-up Current (AMP Peak, 3 ac cycles)	170	170

Table 1-6 lists Model 4050/4150 environmental specifications.

TABLE 1-6: MODEL 4050/4150 ENVIRONMENTAL SPECIFICATIONS

DESCRIPTION	DOMESTIC	INTERNATIONAL
Temperature (Computer Room)	59-86 F	15-30 C
Temperature (Office)	50-95 F	10-40 C
Humidity (Computer Room)	20-80%*	20-80%*
Humidity (Office)	10-90%*	10-90%*
Altitude	8000 feet	2440 meters
Heat Dissipation	4880 Btu/hr	4880 Btu/hr
Noise Output	46 dBA**	46 dBA**

* Non-condensing
** At 25 degrees C

Table 1-7 lists Model 4050/4150 physical specifications.

TABLE 1-7: MODEL 4050/4150 PHYSICAL SPECIFICATIONS

DESCRIPTION	VALUE
Height	30.0 in. (76 cm)
Width	25 in. (63 cm)
Depth	31.0 in. (79 cm)
Weight (fully loaded)	280 lbs (127 kg)

1.7 RELATED DOCUMENTATION

A variety of Customer Service and Technical Publications hardware and software manuals containing useful reference material and procedures are available to help you install, maintain and service the Model 4050/4150 system and its subsystems. Table 1-8 lists the most pertinent material.

TABLE 1-8: MODEL 4050/4150 RELATED DOCUMENTATION

DOCUMENT NAME	PART NUMBER
Prime Model 4050/4150 Handbook	DOC10162-1LA
Using Your 4050/4150	DOC10163-1LA
Site Preparation Guide	DOC5029-3LA
Update to Site Prep. Guide	UPD5029-32A
Prime User's Guide	DOC4130-190
4000 Series Technical Manual	TIM710
4000 Series Pocket Guide	PCG710
PRIMOS and Utilities Software Service Guide	SSG080
System Administrators Guide (Rev.20.2)	DOC5037-3LA
System's Operator's Guide Vol. (20.2.)	DOC5037-4LA
System Administrators Guide (Rev. 21)	
Volume I: System Configuration	DOC10131-1LA
Volume II: Communications Lines	DOC10132-1LA
Volume III: System Access & Security	DOC10133-1LA
Operator's Guide to System Commands (Rev. 21)	DOC9304-3LA
Operator's Guide to File System Maintenance	DOC9300-3LA
Operator's Guide to System Commands	DOC9304-3LA
Diagnostic Testing System (DTS) User's Guide	SMN400
DSM User's Guide	DOC10061-1LA
Model 6580 Intelligent Disk Controller Service Manual	SMN501
Model 4735 Disk Drive Service Procedures Manual	SPM470
Model 4835 Disk Drive Service Procedures Manual	SPM390
Model 4587 Tape Drive Service Procedures Manual	SPM920

1.8 FCO LOG

Prime Field Change Orders (FCOs) are generated whenever a condition exists which requires that equipment in the field be changed. It is important that FCOs be installed in the units in a timely manner and that the FCO log for the equipment be kept current. An accurate record of the changes that have been installed in the unit is necessary to relate the machine configuration to the manual.

1.9 EQUIPMENT IDENTIFICATION

The equipment identification (ID) and model number plates, are located at the lower left rear corner of the system (see Figure 1-3). The system ID plate provides the identification number for the type of system. The model number plate provides the following information:

- Model number
- Serial number
- Voltage and current specifications

1.10 MARKETING MODEL NUMBERS

Model 4050/4150 marketing model numbers are listed in Table 1-9. Table 1-10 lists model numbers of Model 4050/4150 options.

A standard system includes the 4050 or 4150 central processor, the diagnostic processor (VCP-V), cabinet, chassis, power supplies, and PRIMOS operating system (execute-only). All 60Hz versions include a built-in modem for remote diagnostics and a U.S keyboard. All 50Hz versions require a locally-specified modem for remote diagnostics and include a U.K. keyboard. Add -A to all model numbers for the 50Hz version.

NOTE

The marketing model numbers that follow represent a sample of the Model 4050 and 4150 configurations currently available. These model numbers may change and additional model numbers may be added in the future.

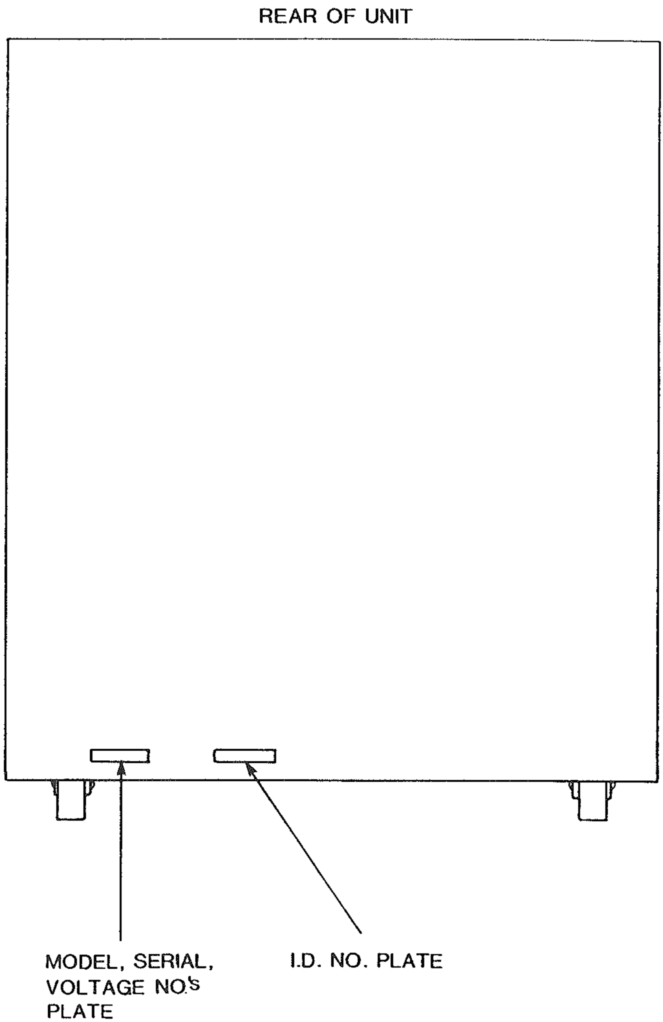


FIGURE 1-3: EQUIPMENT IDENTIFICATION PLATE

TABLE 1-9: MODEL 4050/4150 MARKETING MODEL NUMBERS

MODEL NUMBER	DESCRIPTION
4050-11C	Standard 4050 system with: 2 8MB ECC MOS memory boards 1 496MB Fixed Media Disk Drive 1 Model 6580 Intelligent Disk Controller 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4050-11A	Same as 4050-11C without system console. This model is not available in the U.S.
4050-12C	Standard 4050 system with: 2 8MB ECC MOS memory boards 1 770MB Fixed Media Disk Drive 1 Model 6580 Intelligent Disk Controller 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4050-12A	Same as 4050-12C without system console. This model is not available in the U.S.
4050-23C	Standard 4050 system with: 3 8MB ECC MOS memory boards 2 770MB Fixed Media Disk Drives 1 Model 6580 Intelligent Disk Controller 1 ICS3 (mainbay) with 32 Asynchronous Lines 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4050-23A	Same as 4050-23C without system console. This model is not available in the U.S.
4050-24C	Standard 4050 system with: 3 8MB ECC MOS memory boards 2 496MB Fixed Media Disk Drives 1 Model 6580 Intelligent Disk Controller 1 ICS3 (mainbay) with 32 Asynchronous Lines 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4050-24A	Same as 4050-24C without system console. This model is not available in the U.S.

TABLE 1-9: MODEL 4050/4150 MARKETING MODEL NUMBERS (CONT.)

MODEL NUMBER	DESCRIPTION
4050-25C	Standard 4050 system with: 3 8MB ECC MOS memory boards 2 496MB Fixed Media Disk Drives 1 Model 6580 Intelligent Disk Controller 1 LHC300 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 NTS License 1 PRIMOS User License
4050-25A	Same as 4050-25C without system console. This model is not available in the U.S.
4150-11C	Standard 4150 system with: 3 8MB ECC MOS memory boards 1 496MB Fixed Media Disk Drive 1 Model 6580 Intelligent Disk Controller 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4150-11A	Same as 4150-11C without system console. This model is not available in the U.S.
4150-22C	Standard 4150 system with: 3 8MB ECC MOS memory boards 1 770MB Fixed Media Disk Drive 1 Model 6580 Intelligent Disk Controller 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4150-22A	Same as 4150-22C without system console. This model is not available in the U.S.
4150-23C	Standard 4150 system with: 3 8MB ECC MOS memory boards 2 770MB Fixed Media Disk Drives 1 Model 6580 Intelligent Disk Controller 1 ICS3 (mainbay) with 32 Asynchronous Lines 1 Model 7730H 30-Inch Peripheral Cabinet 1 PT250 System Console 1 PRIMOS User License
4150-23A	Same as 4150-23C without system console. This model is not available in the U.S.

TABLE 1-9: MODEL 4050/4150 MARKETING MODEL NUMBERS (CONT.)

MODEL NUMBER	DESCRIPTION
4150-24C	Standard 4150 system with: 3 8MB ECC MOS memory boards 3 496MB Fixed Media Disk Drives 2 Model 6580 Intelligent Disk Controller 1 ICS3 (mainbay) with 32 Asynchronous Lines 2 Model 7730H 30-Inch Peripheral Cabinets 1 PT250 System Console 1 PRIMOS User License
4150-24A	Same as 4150-24C without system console. This model is not available in the U.S.
4150-25C	Standard 4150 system with: 3 8MB ECC MOS memory boards 3 496MB Fixed Media Disk Drives 2 Model 6580 Intelligent Disk Controller 1 LHC300 2 Model 7730H 30-Inch Peripheral Cabinets 1 PT250 System Console 1 NTS License 1 PRIMOS User License
4150-25A	Same as 4150-25C without system console. This model is not available in the U.S.

TABLE 1-10: MODEL 4050/4150 OPTION MODEL NUMBERS

MODEL NUMBER	DESCRIPTION
4735HG	Left 496MB disk drive, controller, full rack mounting hardware, and cable.
4736HG	Right 496MB disk drive, controller, and cable.
4737HG	Left 496MB disk drive, full rack mounting hardware, and cable.
4738HG	Right 496MB disk drive and cable.
4835HG	Left 770MB disk drive, controller, full rack mounting hardware, and cable.
4836HG	Right 770MB disk drive, controller, and cable.

TABLE 1-10: MODEL 4050/4150 OPTION MODEL NUMBERS (CONT.)

4837HG	Left 770MB disk drive, full rack mounting hardware, and cable.
4838HG	Right 770MB disk drive and cable.
7300HG	Battery Back-up unit (MBBU) for both 60Hz and 50Hz systems.
4587HG	Quad-Density magnetic tape subsystem with controller, cables and peripheral cabinet.
4588	Same as 4587HG but without cabinet.
4560HG	Streaming tape drive with controller and cables.
4561HG	Streaming tape drive with cables.
5735HG	ICS3 subsystem for 7730H peripheral cabinet. Includes one synchronous capable controller, 16-slot card cage, internal cables
5733	ICS3 subsystem for mainbay system.

CHAPTER 2
INSTALLATION

This chapter contains instructions to install, configure, and verify the operation Prime Model 4050/4150 systems. To install the system, complete the installation instructions in the following order:

- Inventory and Inspection
- Handling Precautions
- Site Survey
- System Unpacking/Repacking
- Verifying and Converting Voltages
- Installing the System
- Installing the I/O Subsystem
- Checking Out the Hardware
- Installing the Software
- Final Checkout
- Damaged/Missing Equipment Corrective Procedures

Figure 2-1 illustrates the major activities involved in system installation. Refer to each subsection for details.

2.1 INVENTORY AND INSPECTION

Prior to and during unpacking, inspect the outer carton and packaged components for signs of possible shipping damage or missing equipment. If any of these conditions exist, refer to the Damaged/Missing Equipment Corrective Procedures at the end of this chapter.

2.2 HANDLING PRECAUTIONS

Before handling any system boards, install the Field Service Grounding Kit (TEATTFSKIT). The kit consists of a 10-foot (3-meter) ground cord, a work surface, and a 12-foot (3.6-meter) wrist strap.

CAUTION

MOS IC components can be easily damaged by a discharge of static electricity. When handling system boards, use the following rules:

- DO NOT handle boards when out of their protective shipping bags without using the Field Service Grounding Kit.
- DO NOT walk across carpeted floors (especially in low humidity areas) when handling the board out of its shipping bag.

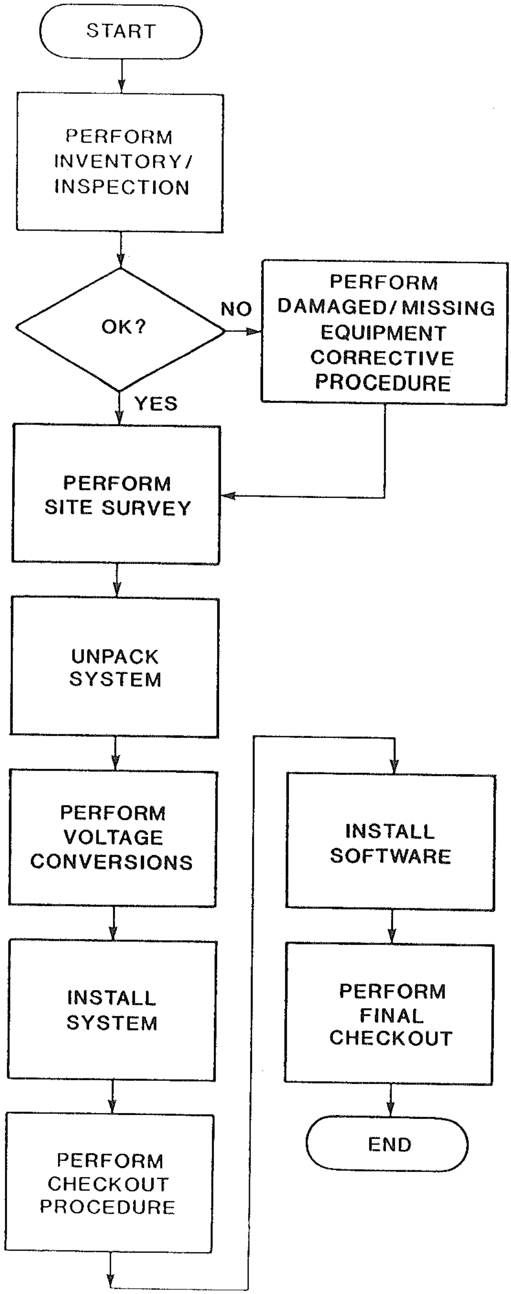


FIGURE 2-1: MAJOR INSTALLATION ACTIVITIES

To use the Field Service Grounding Kit, follow these steps:

1. Place the shielded work surface on a flat area near the system you are installing.

2. Attach the work surface to system ground via the 10-foot ground cord.

3. Attach the wrist strap to ground via the 12-foot ground cord.

4. Slip on the wrist strap.

5. After removing a board from the system chassis, be sure to place the board on the grounded work surface. If further handling is required, insert the board in its static-shielding shipping bag or in the pocket of the work surface, which is designed for this purpose. Always place the board in a static shielding bag if shipping is required.

2.3 SITE SURVEY

Before installing a system, survey the site for the specific electrical and environmental conditions required by the system's components. Refer to the following subsections for system power requirements and electrical and environmental specifications.

NOTE

> Refer to the Prime Office Systems Site Preparation Guide (DOC10058-1LA) for additional site preparation and system environment information.

Using the tables provides below, verify that the site meets the system's electrical and environmental requirements. Tables 2-1 and 2-2 provide mainbay and peripheral cabinet electrical requirements. Table 2-3 provides system environmental requirements. Table 2-4 provides +5V current draw specifications for system PCBs and assemblies.

TABLE 2-1: MODEL 4050/4150 MAINBAY CABINET ELECTRICAL SPECIFICATIONS

DESCRIPTION	DOMESTIC	INTERNATIONAL
Voltage (AC)	120/208 V(156-228)	240 V(180-254)
Frequency (Hz)	57/63	47/53
Phase	4-wire Single	Single
AC Plug	NEMA L14-20P	Unterminated
Consumption	2.00 kVA	2.14 kVA
Start-up Current (AMP Peak, 3 ac cycles)	170	170

TABLE 2-2: MODEL 4050/4150 PERIPHERAL BAY ELECTRICAL SPECIFICATIONS

DESCRIPTION	DOMESTIC	INTERNATIONAL
Voltage (AC)	120 V(90-132)	240 V(180-254)
Frequency (Hz)	57/63	47/53
Phase	Single	Single
AC Plug	NEMA 5-20P	Unterminated
Consumption	.78 kVA	.79 kVA

TABLE 2-3: MODEL 4050/4150 ENVIRONMENTAL SPECIFICATIONS

DESCRIPTION	DOMESTIC	INTERNATIONAL
Temperature (Computer Room)	59-86 F	15-30 C
Temperature (Office)	50-95 F	10-40 C
Humidity (Computer Room)	20-80%*	20-80%*
Humidity (Office)	10-90%*	10-90%*
Altitude	8000 feet	2440 meters
Heat Dissipation	4880 Btu/hr**	4880 Btu/hr**
Noise Output	46 dBA	46 dBA

* Non-Condensing
** At 25-degrees C

TABLE 2-4: OPERATING SPECIFICATIONS: DC DRAW PER I/O CONTROLLER AND MEMORY BOARD

MNEMONIC	BOARD NAME	PART NUMBER	AMPS (+5 V, CC1)
I/O CONTROLLERS:			
QAMLC	Asynchronous Multi-Line Controller (16-line)	5154-901	8.60
BMSMC	Burst Mode Storage Module Controller	4005-901	10.80
BMTC	Burst Mode Tape Controller	2023-901	13.50
DDF-MPC	Dual Density Formatter Micro-Programmed Controller	2270-901	12.30
FMTR	Formatter	2269-901	7.00
ICS1	Intelligent Communications Subsystem 1 Controller	2036-901	6.70
ICS2	Intelligent Communications Subsystem 2 Controller	2034-901	12.80
ICS3	Intelligent Communications Subsystem 3 Controller	TLA10021-001	13.79

TABLE 2-4: OPERATING SPECIFICATIONS: DC DRAW PER I/O CONTROLLER AND MEMORY BOARD (CONT.)

MNEMONIC	BOARD NAME	PART NUMBER	AMPS (+5 V, CC1)
I/O CONTROLLERS:			
MDLC	Multiple Data Link Controller (2 line)	5602-903	11.50
MDLC	Multiple Data Link Controller (4 line)	5602-913	12.0
MTC	Magnetic Tape Controller (9-track)	2081-902	10.20
MTC	Magnetic Tape Controller (NRZ1)	4020-902/ 2295-901	10.20
OPT-A	Option-A	3003-901	6.10
PNC	PRIMENET Node Controller	2257-902	12.70
PNC-II	PRIMENET Node Controller	2384-001	14.00
STS	Streaming Tape Subsystem Controller	2301-901	6.90
MSTC	Minnow SCSI Tape Controller	2382-003	TBS
URC	Unit Record Controller	3156-90X/ 2294-90X	11.4
IDC1	Model 6580 Intelligent Disk Controller	TLA10019-001	13.0
MEMORY BOARD:			
MA	Memory Array (8 Mb)	TLA10088-001	7.0

2.4 SYSTEM UNPACKING

Unpacking instructions are provided in the next subsections for the following:

- Model 4050/4150 Mainbay and Peripheral Cabinets
- Cabinet-mounted and Free-standing Peripherals
- Miscellaneous Items and Software Boxes

2.4.1 SYSTEM CABINETS

The Model 4050/4150 mainbay and peripheral cabinets are packed separately. Each cabinet is bolted to a shipping pallet with an anti-static plastic bag over the cabinet. Systems shipped by ground are packaged with right-angle corrugated cardboard on each corner. The entire shipment is then wrapped in anti-static wrap. Systems shipped by air are further protected by an exterior cardboard carton over the plastic-wrapped cabinet. Store all packing material in a dry place in case repacking and return shipment is required.

Use the procedures in the next two subsections to unpack:

- Air Shipments
- Ground Shipments

2.4.1.1 Unpacking Air Shipments

To unpack a system shipped by air:

1. Cut the banding straps and remove the shipping carton. A typically packaged mainbay cabinet appears in Figure 2-2. A typically packaged peripheral cabinet appears in Figure 2-3.

2. Proceed to the instructions for unpacking ground shipments.

2.4.1.2 Unpacking Ground Shipments

To unpack a system that has been shipped by ground transport see Figure 2-2 or Figure 2-3 and the following procedure.

1. Slide a knife up the plastic shroud to cut it free of the cabinet.

2. Remove the corrugated edge protectors.

3. Remove the pallet ramp, which is vertically stretch-wrapped in place against the side of the cabinet.

4. Install the ramp on the pallet's ramp nails.

5. If you are unpacking a mainbay cabinet, use an adjustable wrench to remove the two shipping brackets that secure the cabinet to the pallet as shown in Figure 2-2. If you are unpacking a peripheral cabinet, use a 3/16 right-angle Allen wrench to remove the four bolts that secure the cabinet to the pallet as shown in Figure 2-3.

6. Roll the cabinet down the ramp and off the pallet. Remove any additional packing material from the cabinet and check for any signs of damage.

7. Position the cabinet in its approximate installation location.

2.4.2 CABINET-MOUNTED AND FREE-STANDING PERIPHERALS

Unpack all cabinet-mounted and free-standing peripherals according to the instructions in the appropriate Service Manual. Move all free-standing peripherals into their permanent positions and level them as required.

2.4.3 MISCELLANEOUS ITEMS AND SOFTWARE BOXES

Unpack miscellaneous items such as I/O cables and software boxes. Boards shipped with the system should remain in their protective packaging until you are ready to install them. When you do unpack the boards, use the ESD kit.

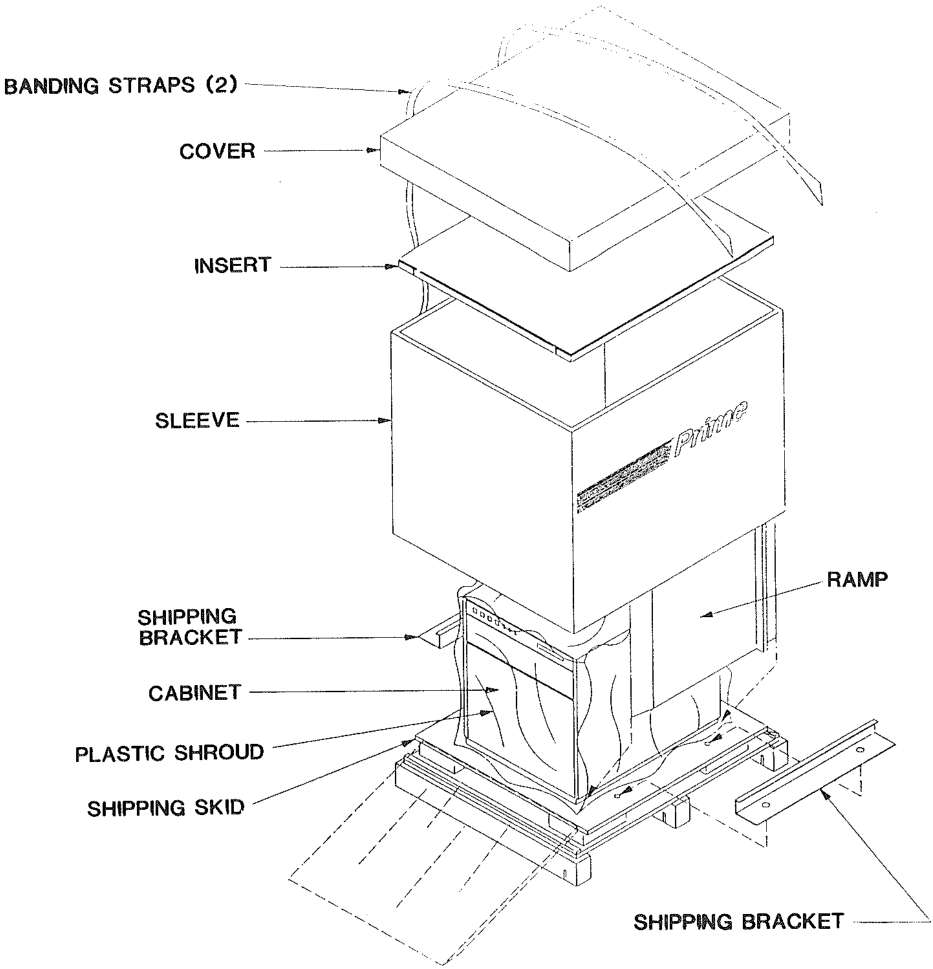


FIGURE 2-2: MAINBAY CABINET UNPACKING

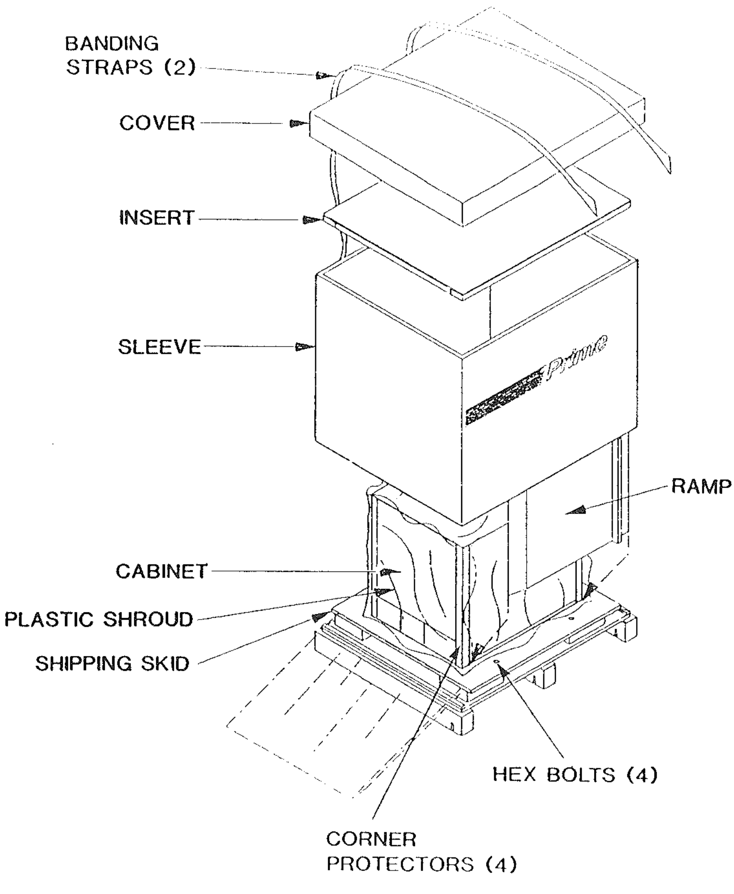


FIGURE 2-3: PERIPHERAL CABINET UNPACKING

2.5 REPACKING

If any problems are found with the Model 4050/4150 cabinet or system components, re-secure the cabinet to the shipping pallet and repack the cabinet and accessories in their original cartons. Refer to Damaged/Missing Equipment Corrective Procedures at the end of this chapter to return defective equipment and order replacement parts.

2.6 VERIFYING AND CONVERTING VOLTAGES

The Model 4050/4150 computer must be properly configured to operate at the customer's available ac voltage. Domestic (U.S.) systems require 208 Vac input power, from which the Power Distribution Unit (PDU) derives 120 Vac to drive the system's internal power supplies and peripheral devices. International systems require 240 Vac input power.

Information is provided in the subsections that follow to verify that your system is properly configured to the customer's voltage. Although conversion should not be necessary, a procedure is also provided to convert a Model 7778 power supply from 120 Vac to 240 Vac and from 240 Vac to 120 Vac.

2.6.1 VERIFYING VOLTAGE CONFIGURATION

To determine if the system and its sub-assemblies are configured for the available ac voltage, complete the following procedure:

1. Locate the system model number plate on the lower right rear corner of the Model 4050/4150 cabinet (see Figure 2-4). If the suffix is <u>not</u> followed by an -A, the system is configured for 208 V (domestic). If the suffix is followed by an -A, the system is configured for 240 V (international).

2. Inspect the PDU's ac power cord. Using Table 2-5, verify that the ac power cord part number is correct for the customer's electrical requirements.

TABLE 2-5: MODEL 4050/4150 AC POWER CABLE PART NUMBERS

PART NUMBER	DESCRIPTION
CBL10898-001	Mainbay Domestic
CBL10598-001	Mainbay International
CBL10864-001	Peripheral Bay Domestic
CBL10600-001	Peripheral Bay International

3. Inspect the mainbay and peripheral cabinet PDU ac connector, then refer to the ac power cable wiring diagrams in Figure 2-5 to verify that the PDU connector is correct for the available voltage.

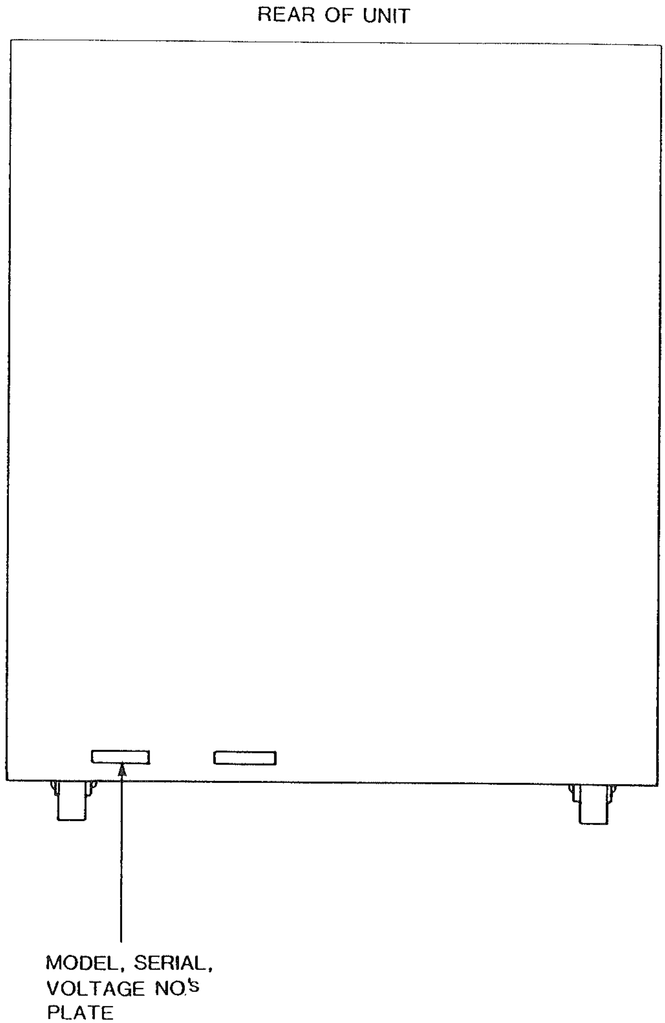
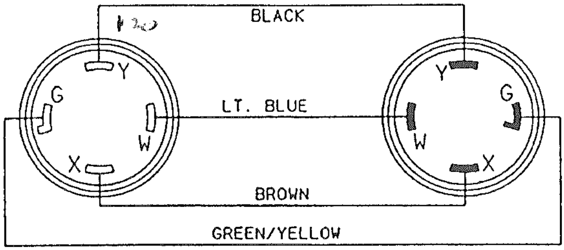
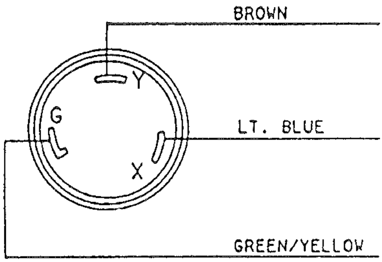


FIGURE 2-4: MODEL PLATE LOCATION

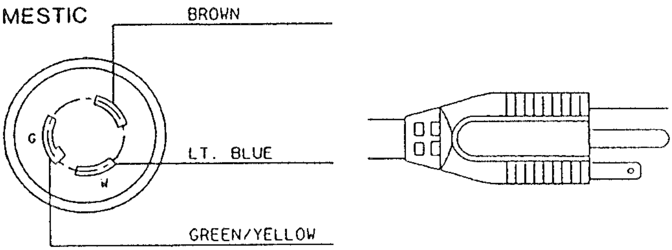
MAINBAY DOMESTIC
CBL10599-001



MAINBAY INTERNATIONAL
CBL10598



PERIPHERAL DOMESTIC
CBL10864



PERIPHERAL INTERNATIONAL
CBL10600

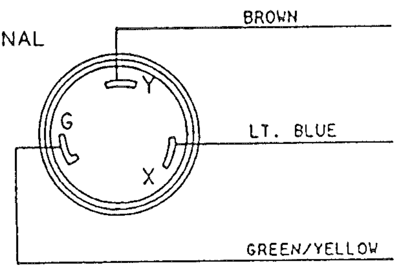


FIGURE 2-5: AC CONNECTOR VERIFICATION

4. Remove the front panel by opening the floppy disk drive access door and unlocking the two quarter-turn captive fasteners.

5. Inspect the system power supply voltage labels (see Figure 2-6). The label located above the ac power connector indicates 120 V or 240 V. The other label indicates the power supply model number as follows:

   - If a -005 suffix follows the model number, the power supply is configured for 120 V (domestic) operation.

   - If a -006 suffix follows the model number, the power supply is configured for 240 V (international) operation.

   NOTE

   If it is necessary to convert the operating voltage of your power supplies, refer to Converting the TLA10113 Power Supplies in this chapter.

   Refer to Installing the TLA10113 Power Supplies in this chapter for shipping restraint removal and power supply installation information.

6. If a Memory Battery Backup Unit (MBBU) is to be installed, inspect the MBBU front panel (see Figure 2-7). Verify that the voltage slide switch is set to the customer's available voltage.

7. Refer to the following subsections in this chapter for procedures to verify the operating voltage of peripheral devices:

   - Model 4735 Disk Drive (496Mb) Installation
   - Model 4835 Disk Drive (770Mb) Installation
   - Model 4587 Tape Drive (Quad-Density) Installation

2.6.2 CONVERTING THE TLA10113 POWER SUPPLIES

If it is necessary to field-convert a TLA10113 power supply, use one of the following voltage conversion kits:

- KIT10035-001 for Conversion from 120 V to 240 V

- KIT10036-001 for Conversion from 240 V to 120 V

All parts necessary to make a conversion are included in the kits, as described in Tables 2-6 and 2-7.

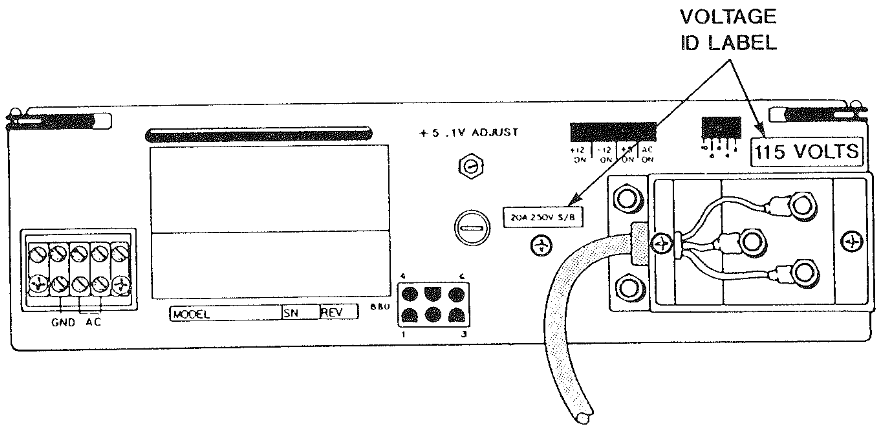


FIGURE 2-6: 7778 VOLTAGE VERIFICATION

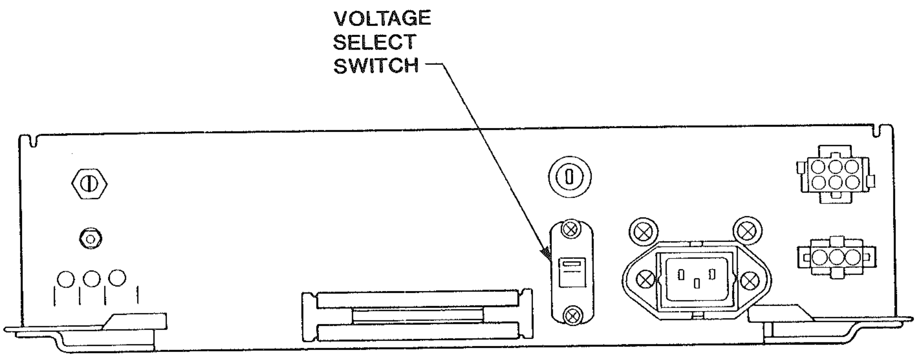


FIGURE 2-7: BATTERY BACKUP UNIT FRONT PANEL

TABLE 2-6: KIT10035-001 (120 V TO 240 V) CONTENTS

PART	DESCRIPTION
CBL8562-001	Cable, Conn., Shorting 50 Hz
CBL10198-002	Cable, ac power, 50 Hz
FUS6094-001	Carrier, Fuse, UL/CSA Style, Gray, .25 mm x 1.25 mm
FUS0224-034	Fuse, 5 mm x 20 mm, 50 Hz 10 A slow blow
MEC1590-006	Label, Model/SN/Rev
MEC1853-002	Label, 230 Volts (Black on Orange)
MEC3259-001	Label, Power Supply Fuse Designation 10 A, 240 V Slow Blow

TABLE 2-7: KIT10036-001 (240 V TO 120 V) CONTENTS

PART	DESCRIPTION
CBL8515-001	Cable, Conn., shorting 60 Hz
CBL10198-001	Cable, ac power, 60 Hz
FUS0224-036	Fuse, 60 Hz 20 A, Slow Blow
FUS6093-003	Fuse, Holder SP HPRO NACAR
MEC1590-006	Label, Model/SN/Rev
MEC1853-001	Label, 115 Volts (Black on White)
MEC3259-005	Label, Power Supply Fuse Designation 20A, 240 V Slow Blow

Complete one of the following conversion procedures if applicable:

- Converting 120 Vac Power Supply to 240 Vac
- Converting 240 Vac Power Supply to 120 Vac

2.6.2.1 Converting 120 Vac Power Supply To 240 Vac

If the power supply is configured for 120 Vac (7778-005) and the available ac voltage is 240 Vac, complete the following procedure:

1. Remove the system power supply (refer to Removing and Replacing the Power Supplies in Chapter 7 of this manual).

2. Locate and remove Jumper Plug CBL8515-001 from connector P3 inside the power supply (see Figure 2-8). Replace Jumper Plug CBL8515-001 with Jumper Plug CBL8562-001.

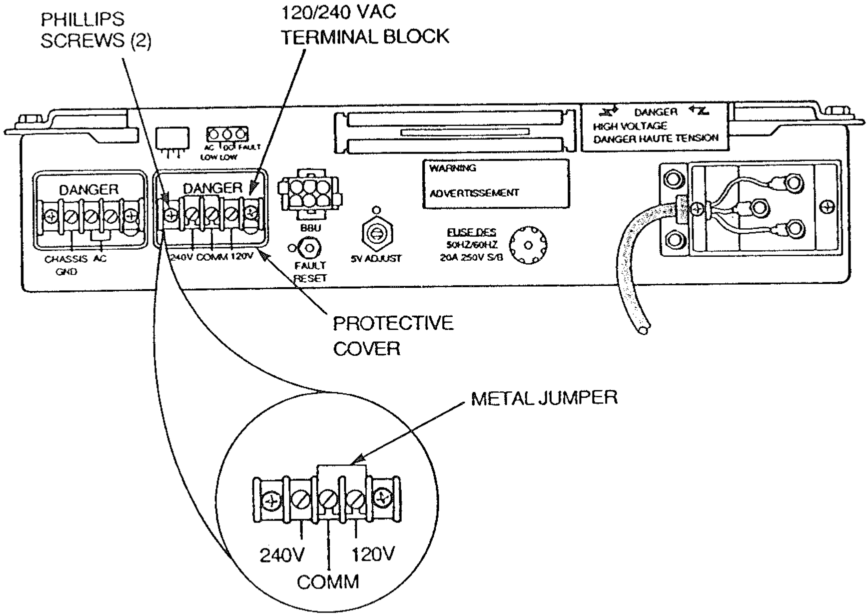


FIGURE 2-8: TLA10113 VOLTAGE CONVERSION

3. Move Jumper WIR1580-006 from connector J4 on the power supply filter PCB to connector J3 (see Figure 2-8).

4. Remove the power supply fuse and fuse carrier, FUS0224-036 (see Figure 2-8). Replace with FUS6215-007 and fuse carrier FUS6094-002.

5. Exchange the two labels on the power supply (see Figure 2-6) as follows:

   - Replace label MEC1853-001 with label MEC1853-002

   - Replace label MEC1590-006 with label MEC1590-007

6. Re-install the system power supply (refer to Removing and Replacing the Power Supplies in Chapter 7 of this manual).

2.6.2.2 Converting 240 Vac Power Supply To 120 Vac

If the power supply is configured for 240 Vac (7778-006) and the available ac voltage is 120 Vac, complete the following procedure:

1. Remove the system power supply (refer to Removing and Replacing the Power Supplies in Chapter 7 of this manual).

2. Locate and remove Jumper Plug CBL8562-001 from connector P3 inside the power supply (see Figure 2-8). Replace with Jumper Plug CBL8515-001.

3. Move Jumper WIR1580-006 from connector J3 on the power supply filter PCB to connector J4 (see Figure 2-8).

4. Remove the power supply fuse FUS6215-007 and carrier (see Figure 2-8). Replace with fuse, FUS0224-036 and fuse carrier FUS6093-003.

5. Exchange the two labels on the power supply (see Figure 2-6) as follows:

   - Replace label MEC1853-002 with label MEC1853-001

   - Replace label MEC1590-007 with label MEC1590-006

6. Re-install the system power supply (refer to Removing and Replacing the Power Supplies in Chapter 7 of this manual).

2.7 SYSTEM INSTALLATION

System installation procedures are presented in the following sequence:

- System Configuration Overview

- Cabling and Verifying the Power Distribution Unit

- Installing the Model TLA10113 Power Supplies

- Installing and Verifying the Power Shunt Board
- Installing the Memory Battery Backup Unit (optional)
- Installing the Uninterruptible Power Supply (UPS) (optional)
- Installing the Memory Boards
- Configuration and Cabling the VCP-V
- Installing and Verifying the CPU
- Installing the System Console

2.7.1 SYSTEM CONFIGURATION OVERVIEW

The following subsections provide a system configuration overview, general configuration guidelines, and a system interconnection diagram.

2.7.1.1 Minimum Configuration Requirements

The minimum configuration for multi-user PRIMOS operation is as follows:

- System Console
- VCP-V Diagnostic Processor
- 8 Mb MMW3-8MB Memory Board
- Model 4050/4150 CPU
- Two Model 7778 Power Supplies
- MBBU or shunt board
- Disk or tape subsystem

2.7.1.2 System Configuration Guidelines

Use the following guidelines when configuring a Model 4050/4150 system (refer to Figure 2-9):

1. The Model 4050/4150 supports up to 32 Mb of main memory (up to four 8 Mb MMW3-8MB memory array boards) in slots M1 through M4.

2. The system supports up to ten I/O controllers in slots I/O1 through I/O10.

3. An optional Memory Battery Backup Unit (MBBU), if installed, requires four I/O slots and one memory slot. Slot I/O4 requires a noise and safety shield (MEC10495-001). The MBBU option reduces the maximum main memory to 24 Mb and the maximum number of I/O controllers to six.

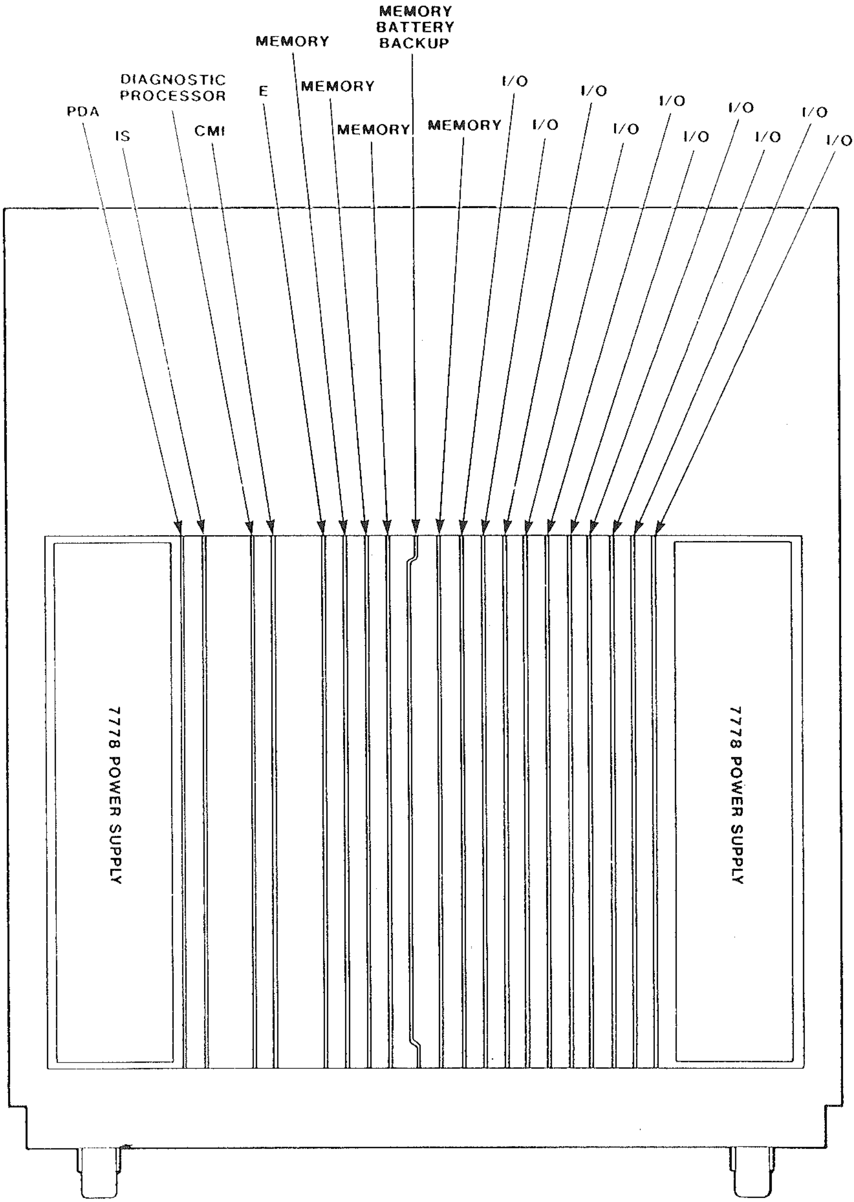


FIGURE 2-9: CARD CAGE CONFIGURATION

4. Install a power shunt board (ESA10252-001) in slot PS1 if a Memory Battery Backup Unit is not installed.

5. ICS3 subsystem can be installed in either the mainbay or peripheral cabinet. Refer to Installing the ICS3 in this chapter to install an ICS3 or to transfer an ICS3 from the mainbay to a peripheral cabinet.

2.7.1.3 System Interconnection Diagram

Figure 2-10 is a cabling diagram for the Model 4050/4150 domestic (208 Vac) and international (240 Vac) systems.

2.7.2 CABLING AND VERIFYING THE POWER DISTRIBUTION UNIT

The power distribution unit (ESA10233 mainbay and ESA10293 peripheral bay) is pre-installed and partially cabled. PDU cabling consists of three major tasks:

- Installing the main ac power cable
- Verifying installation of PDU interface cables
- Daisy-Chaining Mainbay and Peripheral Cabinets

The subsections that follow describe these tasks.

2.7.2.1 Installing the Main AC Power Cable

To install the main ac power cable, follow these steps:

1. Locate the female Hubbell connector on the ac power cable.

2. Align and mate the male pins on the PDU power port with the female connector on the power cable (see Figure 2-11).

3. Twist the connector clockwise until it locks in place.

CAUTION

Do not plug the main power cable into the wall outlet until the system is ready to power up.

2.7.2.2 Verifying the PDU Cabling

All Standard Factory Build systems are shipped with the mainbay and peripheral cabinet PDUs pre-installed and cabled. Refer to Figure 2-12 and the following procedures to verify cabling to the mainbay and peripheral cabinet PDUs.

2.7.2.2.1 Verifying Mainbay PDU Cabling

To verify mainbay PDU cabling, follow these steps:

1. From the rear of the cabinet, remove the two trim panels from either side of the door, unlock the two quarter-turn captive fasteners, and tilt open the rear door.

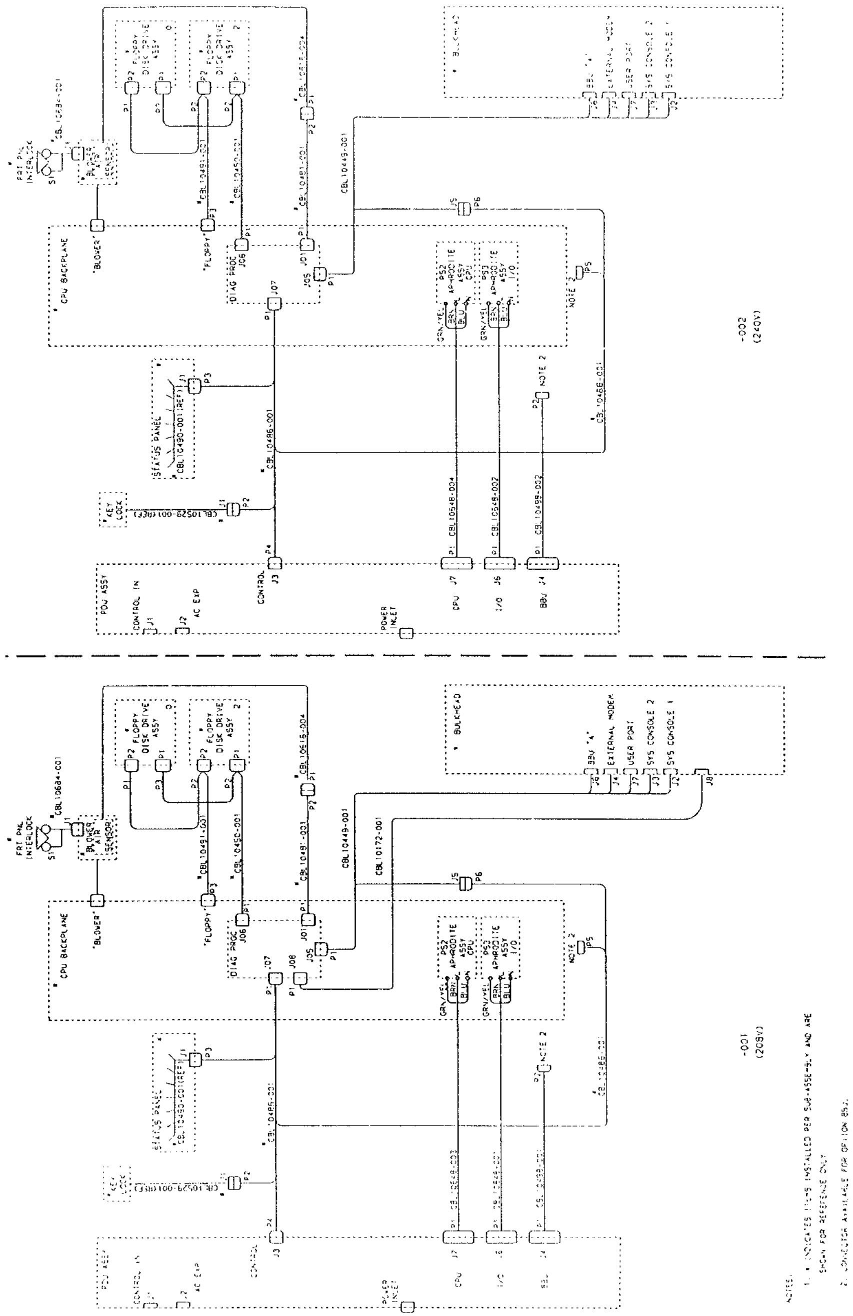


FIGURE 2-10: SYSTEM INTERCONNECTION DIAGRAM

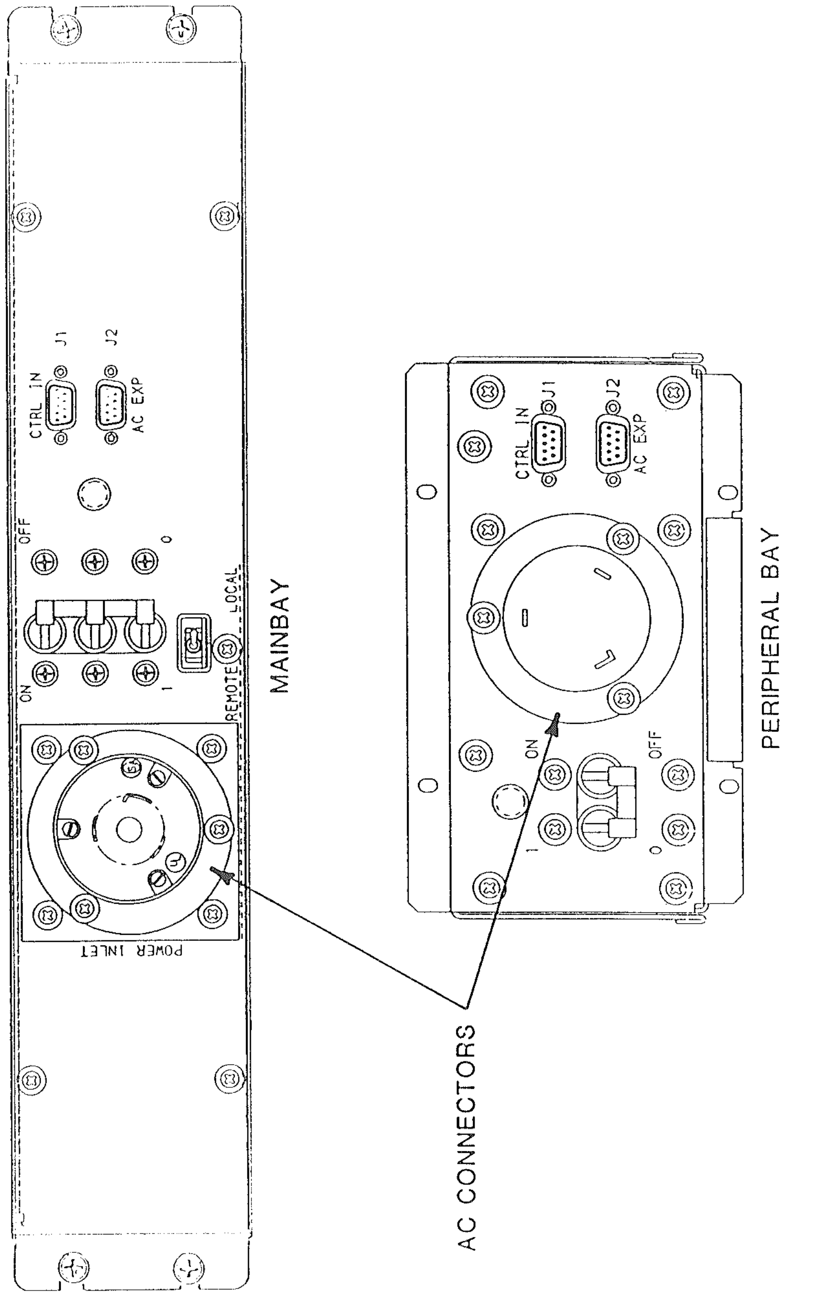
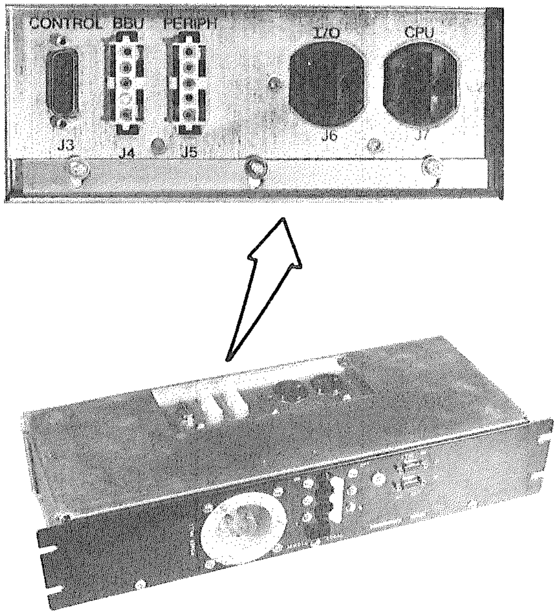
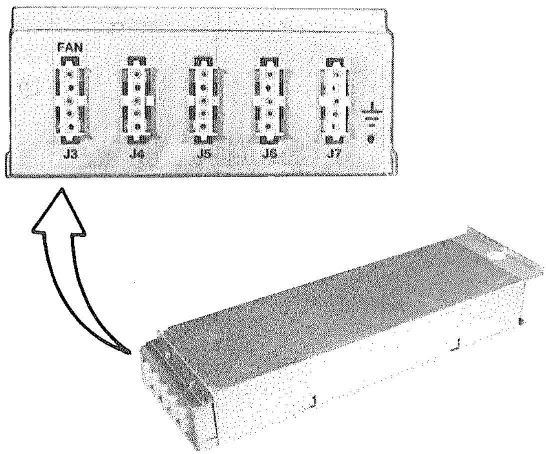


FIGURE 2-11: PDU FRONT PANEL



MAINBAY PDU



PERIPHERAL BAY PDU

FIGURE 2-12: MAINBAY/PERIPHERAL BAY PDU CABLING

2. Verify that the cables are connected to the correct mainbay PDU receptacle as follows (see Figure 2-12):

• VCP/Status Panel Control	to	J3 CONTROL
• Optional MBBU	to	J4 BBU
• Optional ICS3	to	J5 PERIPH
• I/O Power Supply (PS3)	to	J6 I/O
• CPU Power Supply (PS2)	to	J7 CPU

NOTE

Be sure to connect PS3 to J6 and PS2 to J7. If these power supply cables are reversed, the VCP-V will not receive power to sequence the PDUs.

If a Memory Battery Backup Unit (MBBU) is not installed, remove the cable connector from J4 and tie it out of the way. At the front of the cabinet, make sure that the MBBU cables are clear of the card cage.

2.7.2.2.2 Verifying Peripheral Cabinet PDU Cabling

To verify proper peripheral cabinet PDU cabling, follow these steps:

1. From the front of the cabinet, remove the lower cover panel from its ball stud fasteners, then remove the two screws that secure the cover plate to the cabinet chassis to access the peripheral device power cables.

2. Verify that the following cables are firmly connected to a peripheral bay PDU receptacle (see Figure 2-12):

   - Tape drive power
   - Disk drive power
   - ICS3 power (optional)

2.7.2.3 Daisy-Chaining Mainbay and Peripheral Cabinets

The mainbay PDU, under command of the VCP-V, controls the power-up sequence of the peripheral cabinet PDU.

To daisy-chain the mainbay and one or more peripheral cabinets, follow these steps (refer to Figure 2-13):

1. Connect one end of CBL7033-001 to the nine-pin connector on the mainbay PDU labelled AC EXP CONTROL OUT.

2. Connect the free end of CBL7033-001 to the nine-pin connector on the first peripheral cabinet PDU labelled CTRL (J1).

3. Connect the one end of a second CBL7033-001 to the nine-pin connector on the first peripheral cabinet PDU labelled AC EXP (J2).

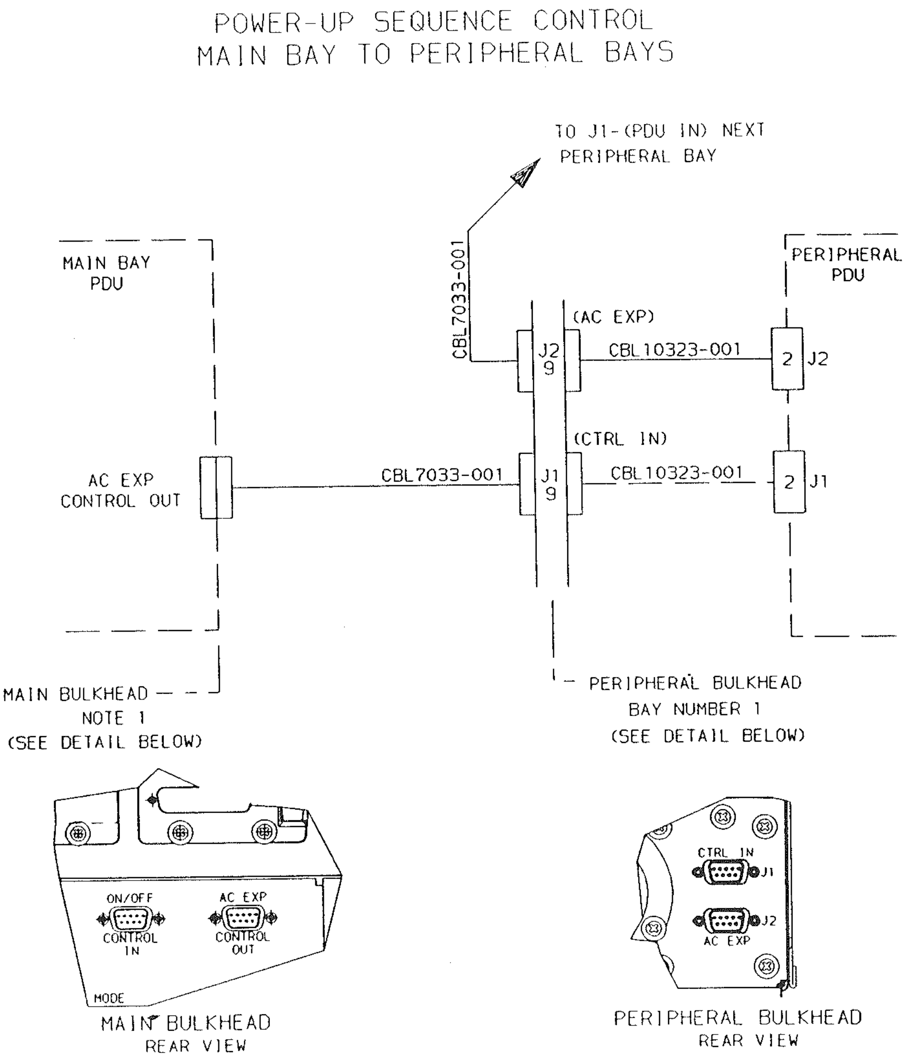


FIGURE 2-13: PDU INTERCONNECTION DIAGRAM

4. Connect the free end of the second CBL7033-001 to the nine-pin connector on the second peripheral cabinet PDU labelled CTRL (J1).

5. Repeat steps 3 and 4 for all subsequent peripheral cabinets in the daisy-chain.

2.7.3 INSTALLING MODEL 7778 POWER SUPPLIES

To install Model 7778 power supplies, follow these steps:

1. Remove the two shipping restraints from the bottom of the 7778 power supplies (see Figure 2-14).

2. Using the ejector arms, seat both power supplies. If you need more information, refer to Removing and Replacing the Power Supply in Chapter 7 of this manual.

CAUTION

Failure to verify installation of the power supplies could seriously damage the system.

3. Verify that PS3 is cabled to PDU connector J6 and that PS2 is cabled to PDU connector J7. If these connections are reversed, the system will not power up.

2.7.4 VERIFYING POWER SHUNT BOARD INSTALLATION

The Model 4050/4150 system cannot operate without a power shunt board (ESA10252-001) or Memory Battery Backup Unit (MBBU). Systems ship with the shunt board pre-installed in slot PS1. Verify that the board is correctly installed by making sure the board is firmly seated in slot PS1 and that the board stiffener is pointing in the direction of the arrow silkscreened on the cardcage (right). Some boards have an arrow on the stiffener. Make sure the arrow is pointing up (towards the system status panel).

CAUTION

The shunt board must be installed correctly to avoid damage to the system.

If you remove the shunt board to install a MBBU (described in the subsection that follows), be sure to save the board at the customer's site.

2.7.5 INSTALLING THE MEMORY BATTERY BACKUP UNIT (MBBU)

All Standard Factory Build systems are shipped with a special power shunt board installed in slot PS1 of the card cage. If an optional MBBU is purchased, the unit must be site-installed in place of the shunt board.

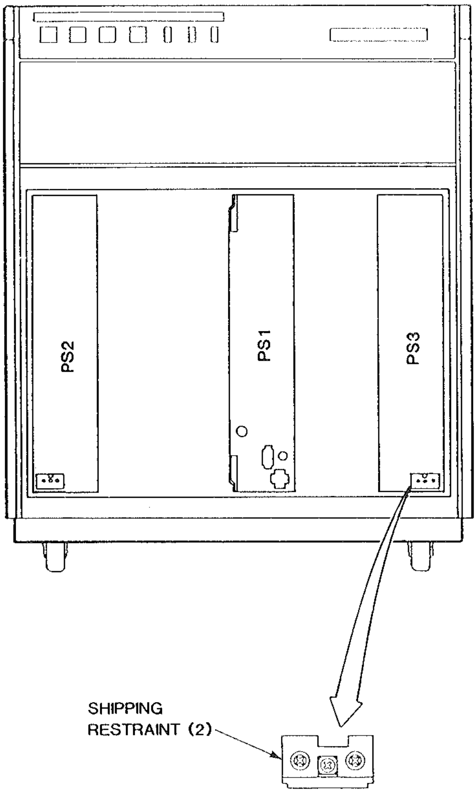


FIGURE 2-14: 7778 SHIPPING RESTRAINT REMOVAL

To remove the shunt board and install an MBBU, follow these steps:

1. Remove the floppy disk drive access door and the front panel (refer to Removing and Replacing System Cabinet Covers in Chapter 7 of this manual).

2. Remove the shunt board from slot PS1 (refer to Removing and Replacing System Boards in Chapter 7 of this manual). Store the shunt board on site in a protective covering.

3. Inspect the MBBU's voltage select switch (see Figure 2-15). Verify that the switch is set to 115V for domestic installations, and to 220V for international installations.

4. Align the MBBU in slot PS1 of the card cage. Push the MBBU into the slot until it rests against the backplane connectors.

5. Push the ejector tabs until the MBBU is firmly seated in the backplane.

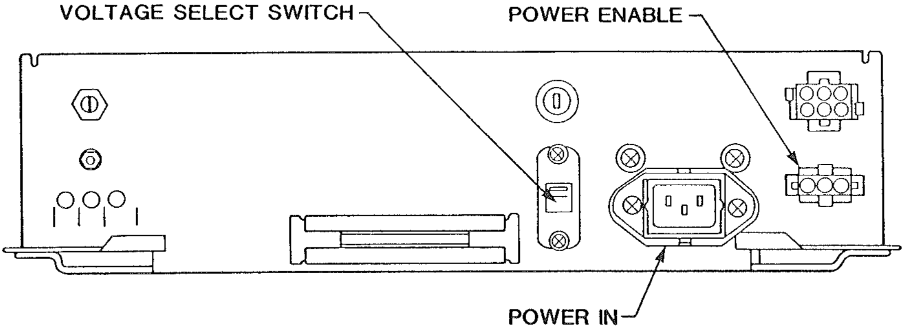


FIGURE 2-15: MBBU INSTALLATION

6. Install the MBBU protective shield (MEC10495-001) in slot I/O4. The shield is secured to the card cage by two captive screws.

7. MBBU cables are already supplied in the system cabinet. Feed the MBBU cables through a slot in the cable comb, then cable the MBBU as follows:

   A) Connect P2 of CBL10498-001 to the connector labelled POWER IN on the MBBU (see Figure 2-15). Connect P1 of CBL10498-001 to J4 on the PDU (see Figure 2-12).

   B) Connect P5 of CBL10486-001 to the connector labelled POWER ENABLE on the MBBU (see Figure 2-15). The free ends of this cable are already connected to the VCP-V, the status panel, the keylock switch, and the PDU control port.

8. Replace the floppy disk drive access door and the front panel.

2.7.6 INSTALLING THE UNINTERRUPTIBLE POWER SUPPLY

The Uninterruptible Power Supply (UPS) maintains ac power if main power is shut off. Normally, the supply only maintains power to the mainbay.

Prime does not currently install or support the UPS. However, Prime recommends the UPS as an alternative to poor electrical power. Prime's hardware and software are configured to support the UPS.

The customer must arrange for purchase, installation and maintenance support of a UPS. The VCP-V receives the following UPS signals:

- ACFAIL-C- : Pin 1
- GND : Pin 2
- LOWBATA-C- : Pin 3

- FAULTA-C : Pin 6

2.7.7 INSTALLING MEMORY BOARDS

Memory boards are packaged and shipped separately. Configuration and installation information is provided in the following sections:

- Memory Board Handling Precautions
- Memory Board Configuration

2.7.7.1 Memory Board Handling Precautions

MOS IC components in memory boards can be easily damaged by a discharge of static electricity. When handling memory boards, be sure to use the Field Service Grounding Kit (TEATTFSKIT) as described in Handling Precautions in this chapter.

CAUTION

> Due to a board warping problem, some memory boards may not align properly with the backplane connector. When installing a memory board, do not use the ejector keys to force the board into the backplane. This could damage the board and/or the backplane. Instead, place your hand against the soldered side of the board and apply gentle pressure to correct the warping, then use your other hand to seat the board into the backplane.

2.7.7.2 Memory Board Configuration

Use the following guidelines to configure MMW3-8MB, MMW3-16MB, and MMW3-32MB memory boards.

1. Only MMW3-8MB, MMW3-16MB, and MMW3-32MB boards may be used.

2. Always begin in slot 1.

3. Only one 32MB memory board may be used in a 4050 or 4150 system. This board must be placed in slot 1. If a 32MB board is used, no other memory boards are allowed in the memory backplane.

4. Due to the memory restriction of the 4150 and 4050 systems (1 - 32MB board), slots should not be skipped when configuring the memory chassis.

5. When using combinations of 8MB and 16MB memory boards in 4150 or 4050 systems, always install the 16MB boards before the 8MB memory boards.

For more specific information on memory board configurations, refer to the Configuring the Memory Subsystem section of the Controller/Memory Boards Service Manual - Service Module MAN552.

2.7.8 CONFIGURING AND CABLING THE VCP-V

The Diagnostic Processor (VCP-V) is a standard 15-inch PCB installed in slot DP of the card cage.

NOTE

The VCP-V used in domestic systems (TLA10132-001) cannot be used in systems outside the United States. International systems use a version of the VCP-V (TLA10132-002) that does not contain the integral modem. To use the REMOTE system terminal function on international systems, attach an external modem to the modem connector on the system bulkhead.

Using the configuration and cabling information for the VCP-V processor in the following subsections, verify that the processor is correctly installed. This step consists of four major tasks:

- Discarding foam shipping material and removing board from cardcage.
- Verifying that VCP-V configuration switches are set correctly.
- Verifying the system identification board.
- Installing and cabling the board.

These tasks are described in the subsections that follow.

2.7.8.1 Removing the Shipping Material

Before the system is shipped from the factory, the diagnostic procesor is protected with shipping foam. Remove the shipping material, eject the board from the cardcage, then proceed to Configuring the Diagnostic Processor.

2.7.8.2 Configuring the Diagnostic Processor

The Diagnostic processor (VCP-V) contains three eight- position DIP switches (see Figure 2-16). The switches configure the floppy media and modem, and set baud rates for VCP-V ports. The switches are accessible only when the board is removed.

After removing the board, use Tables 2-8 and 2-9 to verify that the switches are correctly configured for the local terminal baud rate, self-verification execution, and internal/external modem enabling.

NOTE: DOWN = OFF UP = ON

NOTE

The switch numbers listed in Tables 2-8, 2-9, and 2-9A are correct when used with Figure 2-16. Be aware that the numbers silkscreened on the board do not match the tables. They correspond as follows:

SWITCH NUMBER IN TABLE	SWITCH NUMBER SILKSCREENED ON BOARD
1 - 8	SW2 (1 - 8)
9 - 16	SW1 (1 - 8)
17 - 24	UNLABELED (1 - 8)

The Diagnostic Processor (VCP-V) contains three eight- position DIP switches (see Figure 2-16). The switches configure the floppy media and modem, and set baud rates for VCP-V ports. The switches are accessible only when the board is removed.

Using Tables 2-8, 2-9, and 2-9A, verify that the switches are correctly configured for the local terminal baud rate, self-verification execution, and internal/external modem enabling.

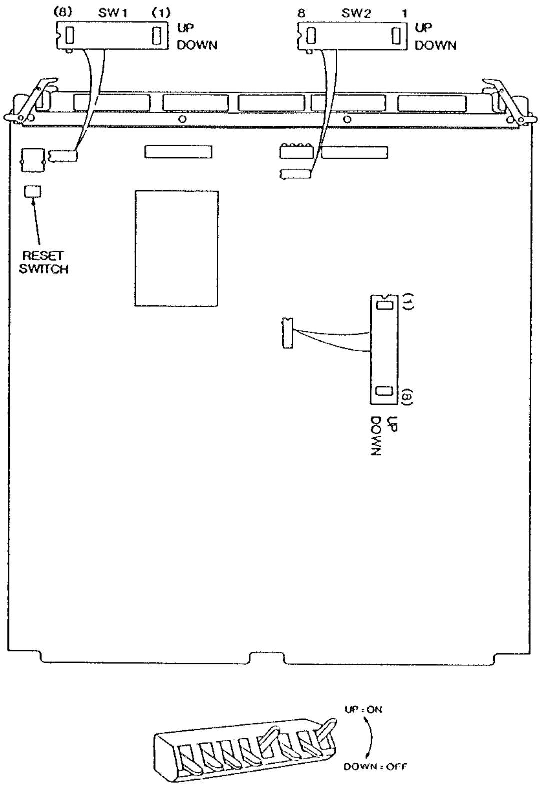


FIGURE 2-16: DIAGNOSTIC PROCESSOR (VCP-V) SWITCHES

TABLE 2-8: DIAGNOSTIC PROCESSOR (VCP-V) OPTION SWITCH A SETTINGS

NOTE: DOWN = OFF UP = ON

SWITCH SETTINGS	FUNCTION
S1 S2 S3	LOCALL SYSTEM CONSOLE BAUD RATE
OFF OFF OFF ON OFF OFF OFF ON OFF ON ON OFF OFF OFF ON ON OFF ON OFF ON ON ON ON ON	300 BAUD 600 BAUD 1200 BAUD 2400 BAUD 4800 BAUD 9600 BAUD 19200 BAUD (Not Supported) 38400 BAUD
S4 S5	REMOTE SYSTEM CONSOLE BAUD RATE
OFF OFF ON OFF OFF ON ON ON	300 BAUD 1200 BAUD 4800 BAUD (Not Supported) 9600 BAUD (Not Supported)
S6	BOOT DEVICE
ON OFF OFF	Attempt to use next logical device if current device fails during power up. Use only the current device
S7	SELF-VERIFICATION EXECUTION
OFF ON	Run self-verification once Loop on failing test
S8	VCP-V CODE BOOT DEVICE
ON OFF	Enable Diagnostic Tools Mode (In-house only) Boot VCP-V code from Floppy Drive

TABLE 2-9: VCP-V OPTION SWITCH B SETTINGS

SWITCH SETTINGS			FUNCTION
S9	S10	S11	LOCAL2 SYSTEM CONSOLE BAUD RATE
OFF	OFF	OFF	300 BAUD
ON	OFF	OFF	600 BAUD
OFF	ON	OFF	1200 BAUD
ON	ON	OFF	2400 BAUD
OFF	OFF	ON	4800 BAUD
ON	OFF	ON	9600 BAUD
OFF	ON	ON	19200 BAUD (Not Supported)
ON	ON	ON	38400 BAUD
S12			
OFF			Normal Operation
ON			If S8 is on, Virtual Floppy Automatically used.
S13			INTERNAL/EXTERNAL MODEM
OFF			External modem enabled
ON			Internal modem enabled
S14	S15	S16	USER MODE PORT BAUD RATE
OFF	OFF	OFF	300 BAUD
ON	OFF	OFF	600 BAUD
OFF	ON	OFF	1200 BAUD
ON	ON	OFF	2400 BAUD
OFF	OFF	ON	4800 BAUD
ON	OFF	ON	9600 BAUD
OFF	ON	ON	19200 BAUD (Not Supported)
ON	ON	ON	38400 BAUD

TABLE 2-9A: VCP-V SWITCH 3 SETTINGS*

SWITCH SETTINGS		FUNCTION
S17		
ON		Battery is Disconnected from Real Time Clock Circuit
OFF		Battery is connected to Real Time Clock Circuit
S18	S19	
ON		Disconnects 2nd PDA port from the Backplane
OFF		Connects 2nd PDA Port to the Backplane

*Switch 3 is unlabeled on the board.

TABLE 2-9A: VCP-V OPTION SWITCH 3 SETTINGS (CONT.)

SWITCH SETTINGS	FUNCTION
S20 S21	
ON ON	Disconnects 1st PDA Port from the Backplane Connects 1st PDA Port to the Backplane
S22	
ON OFF	Does not Supply Modem with -5 volts (used with a 1760) Supplies Modem with -5 volts (used with a 1770)
S23	
Not Used	
S24	
Not Used	

*Switch 3 is unlabeled on the board.

NOTE

The VCP-V ships to the customer site with the LOCAL1 and LOCAL2 ports set at 300 baud. Reset these baud rates to 9600 during system installation.

2.7.8.3 Verifying the System Identification Board

The system is shipped with the system ID board already installed. The system identification (ID) board has a PROM that contains configuration and revision information for the particular system being installed. This board must be installed into connector J03 for the Model 4050/4150 system to operate.

NOTE

If the incorrect ID PROM is installed in a Model 4050/4150 system, a halt occurs and an error message is issued.

Part numbers for the ID board/PROM assemblies are as follows:

- Model 4050 CPU: ESA6481-916
- Model 4150 CPU: ESA6481-913

2.7.8.4 Cabling the Diagnostic Processor

Figure 2-17 illustrates the locations of the VCP-V edge connectors. Table 2-10 lists the VCP-V edge connectors, their functions, and the part number for each connectors mating cable.

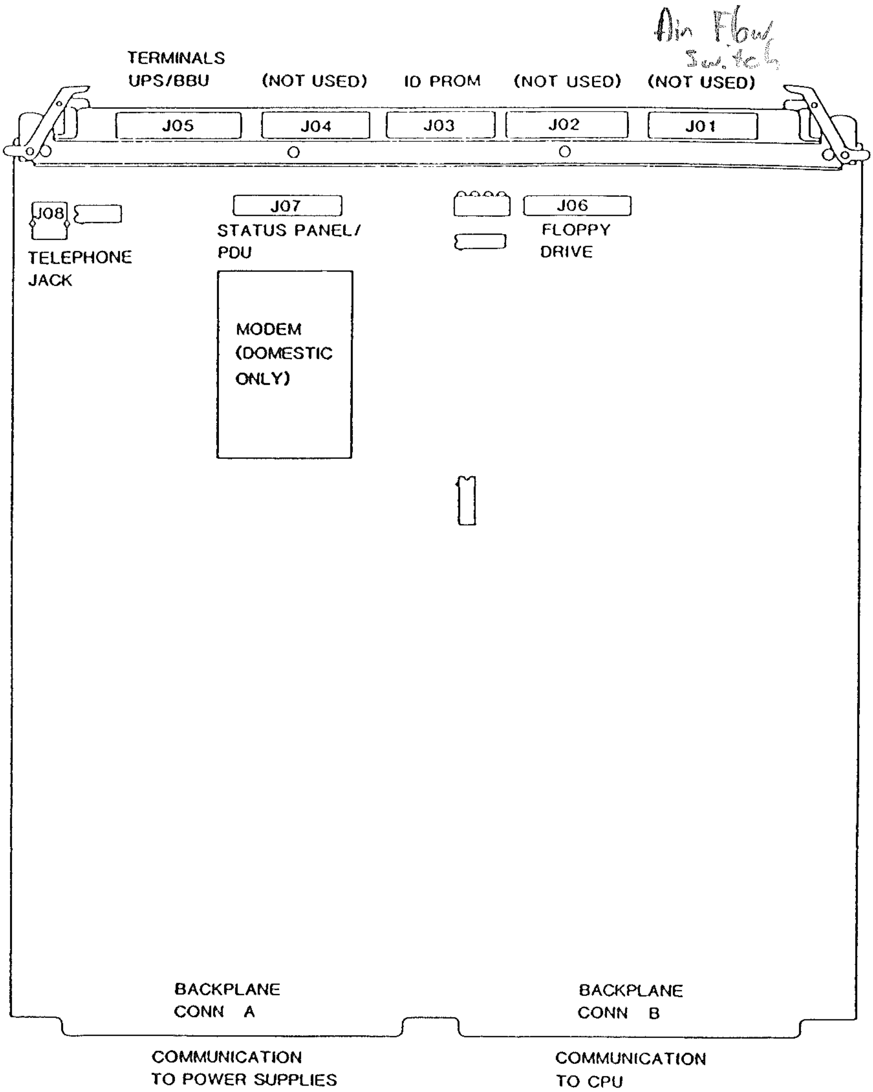


FIGURE 2-17: VCP-V EDGE CONNECTORS

To cable to VCP-V, follow these steps:

1. Install the board in slot DP. Be sure the board components are facing the same direction as the arrow silkscreened on the chassis.

2. Use Figure 2-17 and Table 2-10 to verify that the VCP-V is cabled correctly.

TABLE 2-10: VCP-V EDGE CONNECTORS AND CABLES

CONNECTOR	CONNECTS VCP-V TO:	CABLE NUMBER
J01	Air Flow Switch	CBL10481-001
J03	ID Board/PROM	N/A
J05	Terminals/UPS/MBBU	CBL10449-001
J06	Floppy Disk Assembly	CBL10450-001
J07	Status Panel/PDU	CBL10486-001
J08	Modem Phone Jack	CBL10172-001

2.7.9 VERIFYING CPU BOARD INSTALLATION

Verify that the CPU boards are properly installed by ejecting and reseating all three boards.

The CPU boards have unusually tall VLSI components, with heat sinks about one inch high. Two protective measures help prevent damage to the heat sinks and other components:

- The CPU boards are arranged in pairs of facing boards. Although each board in the pair can be installed in any sequence, you must install each board with its mate so that VLSI components pass each other safely.

- Each CPU board is keyed and labeled for a specific slot.

- The proper orientation is indicated by arrow on the chassis. The arrows point in the direction of the board components.

NOTE

Use ESD procedures and general board-handling procedures when reseating CPU boards. The boards do not "snap" in, as previous boards did. If a board will not seat properly, verify that it is in the correct slot. The front edge of all boards should be even in the card cage if they are properly seated.

2.7.10 INSTALLING THE SYSTEM CONSOLE

Use the following procedure to install the system console:

1. Position the system terminal and connect the terminal power cable to the external ac power source.

2. Install the terminal interface cable between the system terminal and connector J2 of the system bulkhead (see Figure 2-18).

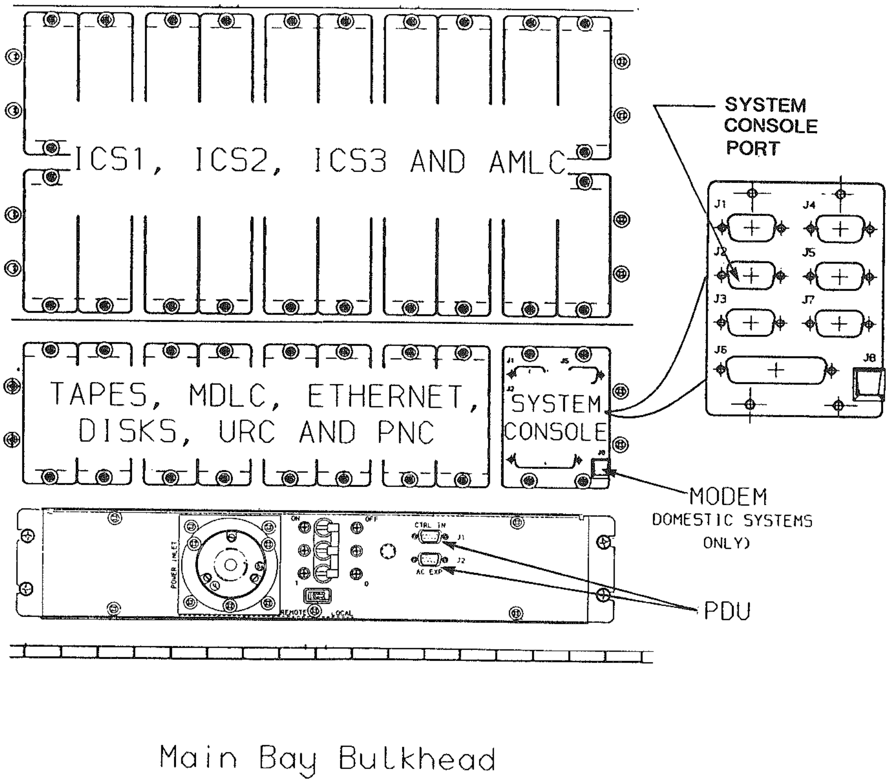


FIGURE 2-18: SYSTEM CONSOLE PORT

3. Apply power to the system terminal.

4. Set the main baud rate setting of the device to match that of the LOCAL1 terminal baud rate on option switch A of the VPC-V diagnostic processor (refer to Configuring the VCP-V in this chapter).

5. Refer to the appropriate service manual for additional terminal installation instructions.

2.8 INSTALLING THE I/O SUBSYSTEM

The Model 4050/4150 system supports a maximum of ten I/O slots. A memory Battery Backup Unit, if installed, requires four I/O slots (I/01 through I/04). Prime's 50 Series controller boards are shipped separately and must be configured and installed at the customer's site. I/O installation information is provided in the following subsections:

- I/O Configuration Guidelines
- Peripheral Cabinet Configuration Guidelines
- Controller Device Address Summary
- Installing Intelligent Disk Controller Model 1 (IDC1)
- Installing SCSI Tape Controller (MSTC)
- Installing the Intelligent Communications Controller (ICS3)
- Installing PRIMENET Node Controller (PNC)
- Installing the LHC300 Controller
- Installing the Model 4735 Disk Drive (496 Mb)
- Installing the Model 4835 Disk Drive (770 Mb)
- Installing the Model 4587 Tape Drive (quad-density)
- Controller Board Cabling Diagrams

2.8.1 I/O CONFIGURATION GUIDELINES

Use the following general configuration guidelines when installing the I/O subsystem:

1. Slot priority for the Model 4050/4150 is the same as for other 50 Series systems, except that it is no longer necessary to be concerned about the number of slots between controllers. However, cleaner control signals result if spacing between boards is minimized and controllers are clustered near the I/O power supply (PS3).

2. Among communications devices, all asynchronous devices have priority over synchronous devices.

3. Place the highest priority I/O controller in the highest numbered I/O slot. That is, slot I/O10, the rightmost slot, has the highest priority and slot I/O1 has the lowest. Priority for I/O controllers in Model 4050/4150 systems is presented in Table 2-11. If you have further questions concerning priority, contact the Support Center.

TABLE 2-11: I/O CONTROLLER PRIORITY: BASIC ORDER

PRIORITY	I/O CONTROLLER
Lowest	Synchronous
●	Asynchronous
●	Disk
Highest (Rightmost slot)	Tape (see Note)

NOTE

Install the magnetic tape controller (MSTC) to the right of disk controllers.

4. Reseat all circuit boards in the backplane before connecting any cables.

5. Connect cables to the rightmost board in the cabinet, then work toward your left using a vacant slot in the cable dress comb nearest the board you are installing. The comb guides the cable into the wireform cable trough on the top right side of the chassis.

6. Mark the line number connections on all cables not marked by color code. For example, AMLC cable 6126 may be connected to any one of the four AMLC edge connectors. Each connector runs 4 of the possible 16 lines on an AMLC. The cable receptacle-connector ends must be marked with the 4-line numbers (0-3, 4-7, 8-11, or 12-15) connected to the cable.

7. When bulkheading peripheral devices, refer to the recommended bulkheading scheme shown in Figure 2-19.

8. Tighten all connector screws.

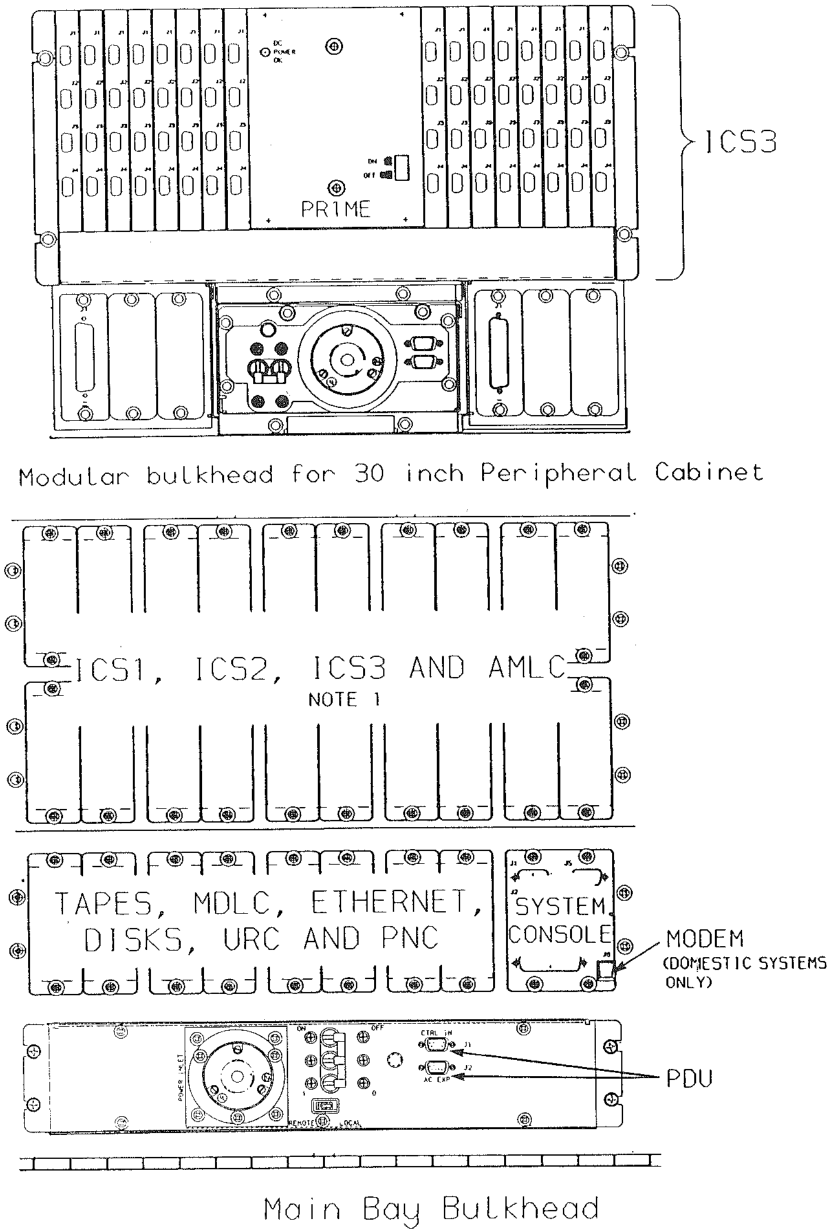


FIGURE 2-19: SYSTEM BULKHEADING

2.8.2 PERIPHERAL CABINET CONFIGURATION GUIDELINES

The 30-inch peripheral cabinet provides rack mounting space in four zones for disk drives, tape drives, and Intelligent Communications Subsystem Model 3 card cages. The following unit combinations are allowed in the 30-inch peripheral bay:

A) Tape Drive 1

B) Tape Drive 1 and Tape Drive 2

C) Tape Drive 1 with Disk Drive 1 and/or Disk Drive 2

D) Tape Drive 1 with ICS3

E) Disk Drive 1 and/or Disk Drive 2

F) Disk Drive 1 and/or 2 with Disk Drive 3 and/or 4

G) Disk Drive 1 and/or 2 with ICS3

H) ICS3 1

I) ICS3 1 and ICS3 2

To select the appropriate zone for a peripheral device, match your unit combination above against the zones described in Figure 2-20 and Table 2-12.

NOTE

Cover all unused rail space with decorative 10.5 inch front filler panels as described in Table 2-12.

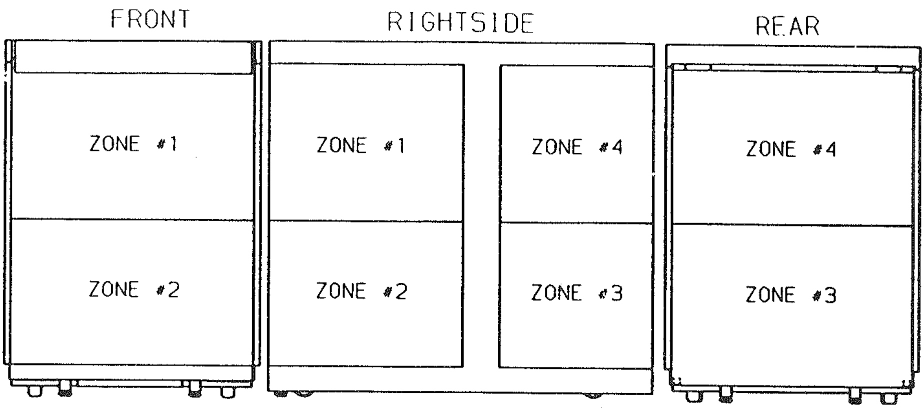


FIGURE 2-20: PERIPHERAL CABINET ZONE DESIGNATIONS

TABLE 2-12: PERIPHERAL CABINET CONFIGURATION GUIDE

UNIT	TAPE DRIVE	496/770MB DISK DRIVE	ICS3	10.5-INCH FILLER
A	Tape 1/Zone 1			Zone 2
B	Tape 1/Zone 1 Tape 2/Zone 2			
C	Tape 1/Zone 1	Disk 1,2/Zone 2		
D	Tape 1/Zone 1		Unit 1/Zone 3	Zone 2
E		Disk 1,2/Zone 2		Zone 1
F		Disk 1,2/Zone 2 Disk 3,4/Zone 1		
G		Disk 1,2/Zone 1	Unit 1/Zone 3	Zone 2
H			Unit 1/Zone 3	Zone 1&2
I			Unit 1/Zone 3 Unit 2/Zone 4	Zone 1&2

To cable the mainbay PDU to the first peripheral cabinet PDU and daisy-chain subsequent PDUs, refer to Daisy Chaining Mainbay and Peripheral Cabinet PDUs in this chapter.

2.8.3 CONTROLLER DEVICE ADDRESS SUMMARY

Table 2-13 provides a quick summary of Prime controller device addresses. To facilitate servicing, mark boards with their respective address. For additional information, refer to the installation section for that specific device in this chapter, or to the appropriate controller board service manual.

TABLE 2-13: CONTROLLER DEVICE ADDRESSES

DEVICE ADDRESS (OCTAL)	CONTROLLER MODEL	DESCRIPTION
00	----	-----
01	3000	Paper Tape Reader
02	3000	Paper Tape Punch
03	31XX/2294	URC #1 (Line Printer, Card Reader)
04	*	System Terminal
05	31XX/2294	URC #2 (Line Printer, Card Reader)
06	7000	IPC (Interprocessor Communications Board)
07	7040	PRIMENET Node Controller #1
10	2034/2036	ICS2 #1 or ICS1 (Intelligent Communication Subsystem) #3

TABLE 2-13: CONTROLLER DEVICE ADDRESSES (CONT.)

DEVICE ADDRESS (OCTAL)	CONTROLLER MODEL	DESCRIPTION
11	2034/2036	ICS2 #2 or ICS1 #4
12	4300	Floppy Disk
14	2382-003	Magnetic Tape Controller #1
15	5XXX/2036	AMLC/QAMLC #5 or ICS1 #8
16	5XXX/2036	AMLC/QAMLC #6 or ICS1 #7
17	5XXX/2036	AMLC/QAMLC #7 or ICS1 #6
20	*	Processor I/O Select (PIOS) Board SOC (System Option Controller)
21	4002	Disk Option B'
22	4005/6580/6590	Disk Controller #3
23	4005/6580/6590	Disk Controller #4
24	6590	Disk Controller #5
25	6590	Disk Controller #6
26	4005/6580/6590	Disk Controller #1
27	4005/6580/6590	Disk Controller #2
30	3007	Buffered Parallel I/O Channel #1
31	3025	Buffered Parallel I/O Channel #2
32	5XXX/2036	AMLC/QAMLC #8 or ICS1 #5
33	3009/3008	VERSATEC/GOULD Printer Plotter
34	3009/3008	VERSATEC/GOULD Printer Plotter
35	5XXX/2036	AMLC/QAMLC #4 or ICS1
36	2034/2036	ICS1 #1 or ICS2 #3
37	2034/2036	ICS1 #2 or ICS2 #4
40	6000/6005	PRIMAD (AIS, Analog Input System)
41	6020	Digital Input #1 (DIS)
42	6020	Digital Input #2
43	6040	Digital Output #1 (DOS)
44	6040	Digital Output #2
45	6590	Disk Controller # 7
46	6590	Disk Controller # 8
47	7040	PRIMENET Node Controller #2
50	5300	HSSMLC #1 (High Speed Synchronous Multiline Controller) or MDLC (Multiple Data Link Controller)
51	5300	HSSMLC #2 or MDLC
52	5XXX/2036	AMLC/QAMLC #3 or ICS1
53	5XXX	AMLC/QAMLC #2
54	5XXX	AMLC/QAMLC #1
55	5400	Multiple Autocall
56	5200	SMLC (Synchronous Multiline Controller)
	LHC300	LAN Controller
57	____	____________
60	7000	General Purpose Interface Board
61	7000	General Purpose Interface Board
62	7000	General Purpose Interface Board
63	7000	General Purpose Interface Board
64	7000	General Purpose Interface Board
65	7000	General Purpose Interface Board
66	7000	General Purpose Interface Board
67	7000	General Purpose Interface Board

TABLE 2-13: CONTROLLER DEVICE ADDRESSES (CONT.)

DEVICE ADDRESS (OCTAL)	CONTROLLER MODEL	DESCRIPTION
70	----	Reserved for Specials
71	----	Reserved for Specials
72	----	Reserved for Specials
73	----	Reserved for Specials
74	----	Reserved for Specials
75	----	Reserved for Controllers Using T$GPPI
76	----	Reserved for Controllers Using T$GPPI
77	----	I/O Bus Tester

*Used by the VCP-V Diagnostic Processor

2.8.4 INSTALLING THE INTELLIGENT DISK CONTROLLER (IDC1)

This subsection provides information to install the 6580 Intelligent Disk Controller (TLA10019-001). The IDC1 can control up to four Model 4735 fixed module disk drives (496 Mb) or Model 4835 fixed module disk drives (770 Mb) in any combination.

NOTE

> If you are installing the IDC1 and a Model 4735 or Model 4835 disk drive as an add-on to an existing system, install the disk drive first, then the IDC1 controller. This minimizes system down-time and avoids powering down the mainbay cabinet more than once to complete the controller to disk drive connections. Refer to Installing the Model 4735 Disk Drive or to Installing the Model 4835 Disk Drive in this chapter for more information.

Refer to the following subsections for controller configuration and cabling information:

- Configuration Rules
- Controller Settings
- IDC1 Insertion and Cabling

For more detailed information on the Model 6580 Intelligent Disk Controller (IDC1), refer to SMN501.

2.8.4.1 Configuration Rules

This subsection provides the configuration parameters that define minimum revision levels and permissable IDC1 controller mixes within a system.

The IDC1 must be at revision R or greater for use in the Model 4050/4150 system.

The 6580 controllers can be included with 4005 channel command protocol controllers in a system. Four unique addresses permit a total of four controllers of any mix.

2.8.4.2 Controller Settings

This subsection describes the device address header and jumpers on the 6580 controller.

ADDRESS HEADER

The header dip at address 43C configures the controller's address. Figure 2-21 illustrates the possible addresses, and Table 2-14 describes the pins jumpered in each case.

TABLE 2-14: CONTROLLER ADDRESS/JUMPER CONFIGURATION

CONTROLLER NUMBER	HEADER SITE 43C ADDRESS (OCTAL)	JUMPER FROM PIN	JUMPER TO PIN
1st	26	3	10
2nd	27	3	9
3rd	22	3	14
4th	23	3	13

JUMPERS

The controller has seven pairs of jumpers that encode the operation mode and hardware revision level of the board. The operation mode test points set the controller in 4005 mode when jumpers are on test points 1 and 9. In this mode the controller reports a 4005 controller ID, and accepts only 4005 channel commands. Figure 2-21 illustrates the jumper test points. If the jumper is not present, the board asks PRIMOS for the downline load file. If the file exists, the IDC1 operates in Intelligent Channel Order Protocol (ICOP) mode.

Certain revisions of the board PROM code verify that the hardware is at the revision level required by the code. If the hardware does not meet the rev. level requirement, the board fails its self-verify test and reports the error through LEDs at the right front edge of the board.

2.8.4.3 IDC1 Insertion and Cabling

To install the Model 6580 Disk Controller, follow these steps:

1. Verify that the test point and address header configurations are correct.

2. Slide the controller into the appropriate I/O slot in the system chassis. Refer to I/O Configuration Guidelines in this chapter for slot selection rules.

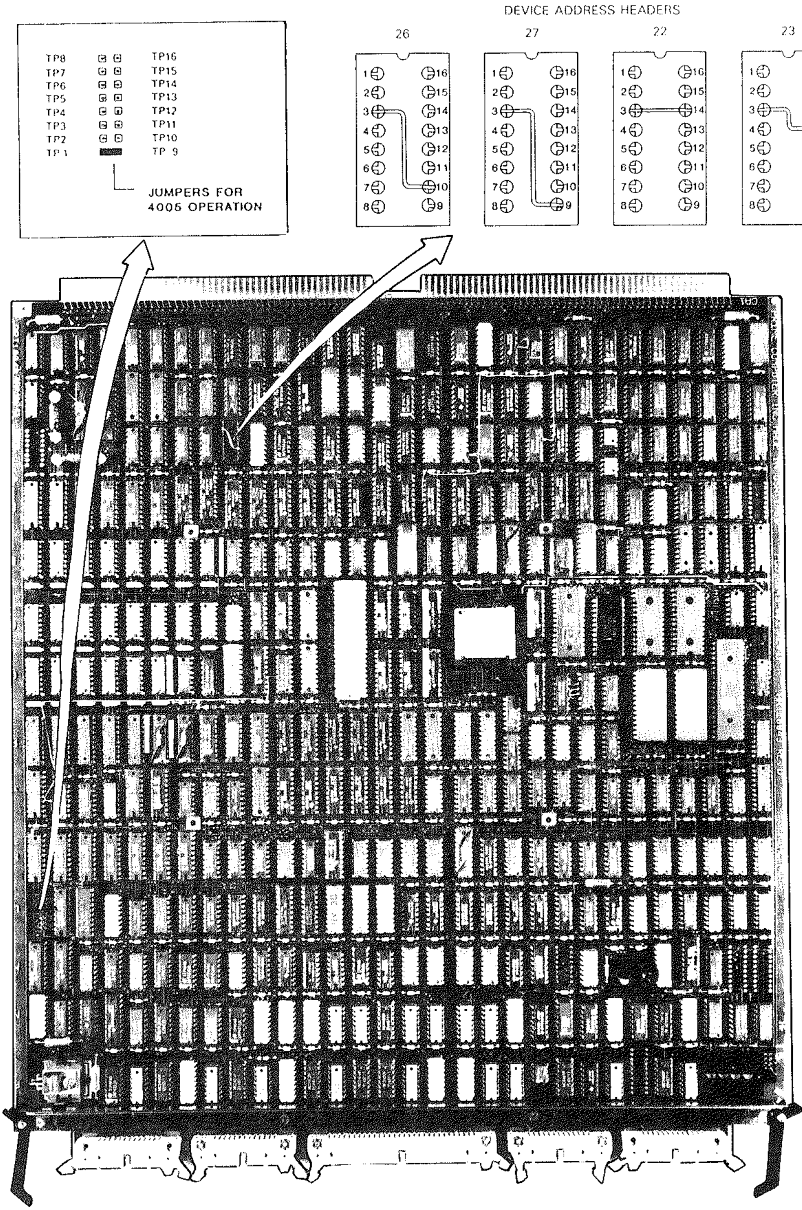


FIGURE 2-21: IDC1 CONFIGURATION

3. Using the board ejector keys, seat the board firmly in the backplane.

4. Connect one end of control cable CBL10702-002 to connector J03 (60 pin) on the controller board (see Figure 2-22).

5. Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough. Then connect the free end to a 62 pin disk connector panel on the system bulkhead (refer to Figure 2-19 for a recommended bulkheading scheme).

6. For each disk drive you are installing, connect one end of data cable CBL10701-004 to a data connector on the controller board (refer to Figure 2-22).

7. Feed the cable through the cable dress comb and into the wireform cable trough. Then connect the free end to a 25 pin disk connector panel on the system bulkhead (refer to Figure 2-19 for a recommended bulkheading scheme).

8. Refer to Installing the Model 4735 Disk Drive or Installing the Model 4835 Disk Drive in this chapter for disk drive installation and cabling information.

2.8.5 INSTALLING THE SCSI TAPE CONTROLLER (MSTC)

The SCSI Tape Controller (2382-003) is a modified Disk/Tape Controller (2382-XXX). The controller supports one Model 4587 quad-density tape drive in a peripheral cabinet.

Controller installation is divided into the following subsections:

- Converting the 2382 Controller
- Verifying MSTC Device Address and Revision Jumpers
- Installing and Cabling the MSTC

All 2382 controllers shipped as part of a standard factory build are pre-converted at the factory and require only verification/modification of the device address and hardware revision jumpers, installation, and cabling. If you are configuring a factory-installed tape drive, proceed directly to Verifying the MSTC Device Address and Revision Jumpers, and to Installing and Cabling the MSTC.

Controller boards shipped by Logistics require field modification. If you are installing a 2382 controller as a replacement board, refer to Converting the 2382 Controller before configuring and installing the controller.

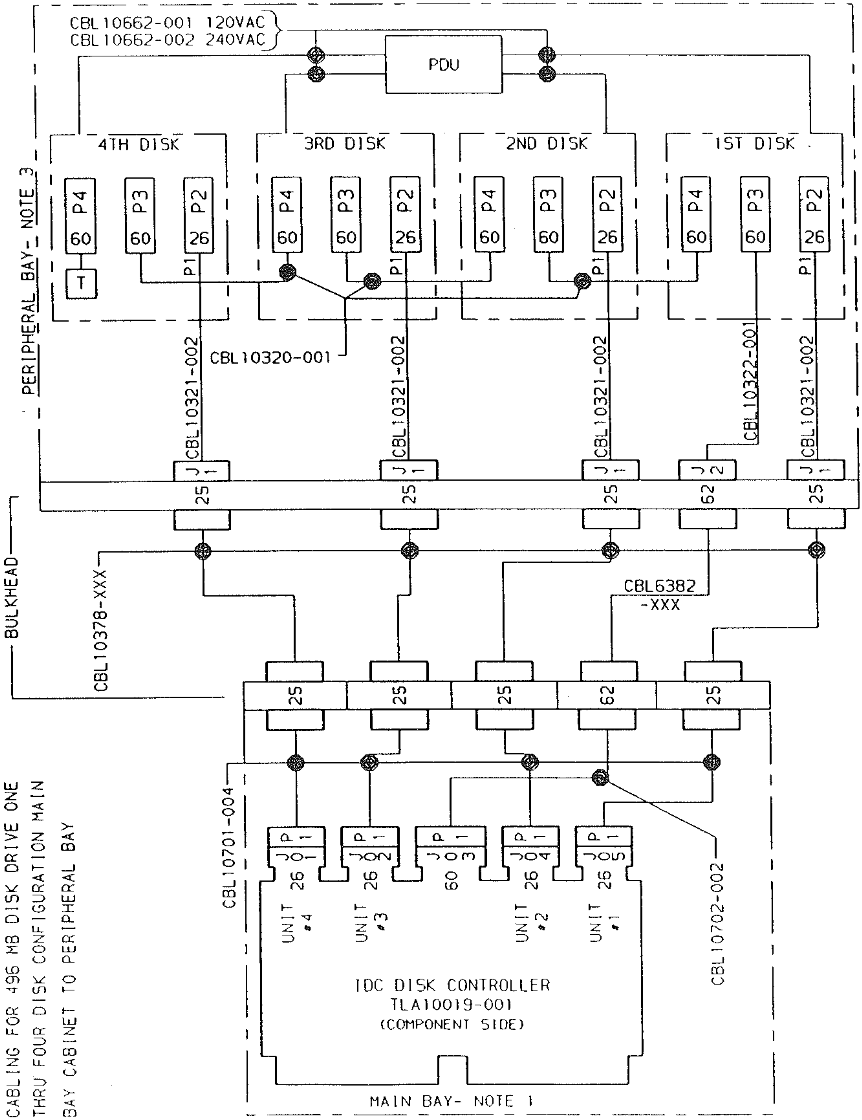


FIGURE 2-22: IDC1 CABLING

2.8.5.1 Converting the 2382 Controller

Conversion of a 2382-001 to a 2382-003 requires KIT10204-001, which is shipped with the 2382-001 controller board. The kit contains the following items:

- INS10075 Conversion Instructions
- PRM10257-001 AJU Microcode PROM (Rev. 1)

To convert a 2382-001 (MDTC) to a 2382-003 (MSTC), follow these steps:

NOTE

The 2382-001 (MDTC) must be at Revision R or greater to be converted into a 2382-003 (MSTC).

1. Remove the disk header from location 25E (see Figure 2-23).
2. Replace the SQ PROM set with the AJU PROM set supplied in KIT10204-001 (see Figure 2-23).
3. Verify that hardware revision jumpers are set to 8 (see Figure 2-23).
4. Using a pen, change the controller board model number on the board stiffener to 2382-003.

2.8.5.2 Verifying MSTC Device Address and Revision Jumpers

The MSTC contains an option block header at location 25C (see Figure 2-23) that controls the device address of the tape segment of the controller as follows:

FIRST CONTROLLER:

If the MSTC is the first tape controller in the system, verify that the board address is '14 (pin 7 jumpered to pin 13).

SECOND CONTROLLER:

If the MSTC is the second tape controller in the system, verify that the board address is '13 (pin 7 jumpered to pin 12).

NOTE

Model 2382 controllers shipped from the factory as expansions, upgrades, or spares are pre-addressed as the first controller ('14).

The board also contains a series of jumpers that identify the board's hardware revision. The jumpers should be set to 8, as shown in Figure 2-23.

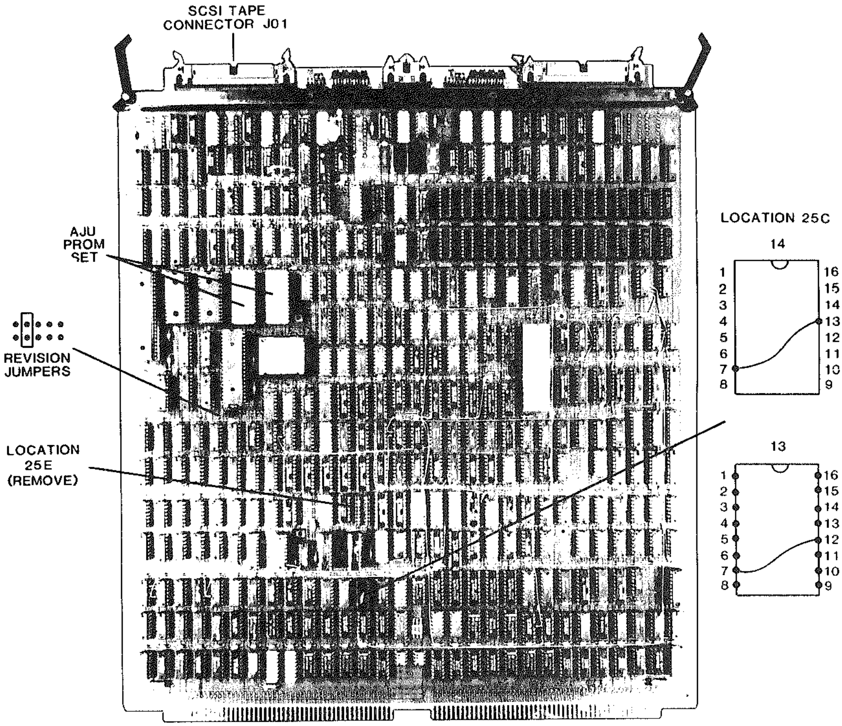


FIGURE 2-23: MSTC CONFIGURATION

2.8.5.3 Installing and Cabling the MSTC

To install the MSTC, follow these steps:

1. Verify that the microcode PROM and tape address header are correct, that the disk address header is removed, and that hardware revision jumpers are in their correct locations, as described in the previous sections.

2. Slide the controller into the appropriate I/O slot in the system chassis. Refer to I/O Configuration Guidelines in this chapter for slot selection rules.

3. Using the board ejector keys, seat the board firmly in the backplane.

4. Connect one end of cable CBL10394-002 to SCSI connector J01 (50 pin) on the controller board (see Figure 2-24). The SCSI connector is the rightmost connector on the board if you hold the board component side up with the stiffener pointing toward you. The other side is unused.

NOTE

The board will not verify if the control cable is inserted in the wrong connector.

5. Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough. Then connect the free end to a 50 pin tape connector panel on the system bulkhead (refer to Figure 2-19 for a recommended bulkheading scheme).

6. Refer to Installing the Model 4587 Tape Drive in this chapter for tape drive installation and cabling information.

2.8.6 INSTALLING THE INTELLIGENT COMMUNICATIONS CONTROLLER (ICS3)

The ICS3 consists of a printed circuit board controller assembly and a 16-slot card cage. The 16-slot card cage is designed to fit the Model 4050/4150 mainbay and the 30-inch or 53-inch peripheral cabinets.

The following subsections provide ICS3 installation procedures for Model 4050/4150 mainbay and peripheral cabinet configurations:

- Using This Installation Guide
- Verifying ICS3 Configuration
- Installing the ICS3 Controller
- Installing the ICS3 Card Cage
- Transferring the ICS3 Card Cage
- Installing ICS3 Line Adapter Cards (LACs)
- Cabling Devices to the ICS3

2.8.6.1 Using This Installation Guide

This section contains several procedures to help you install the ICS3 controller and card cage. To help make the installation proceed more smoothly, complete the procedures in the following order:

1. Make sure your ICS3 controller board, buffer card, and LAC backplane are properly configured. Refer to Verifying ICS3 Configuration.

2. Install and cable the controller board. Refer to Installing the ICS3 Controller.

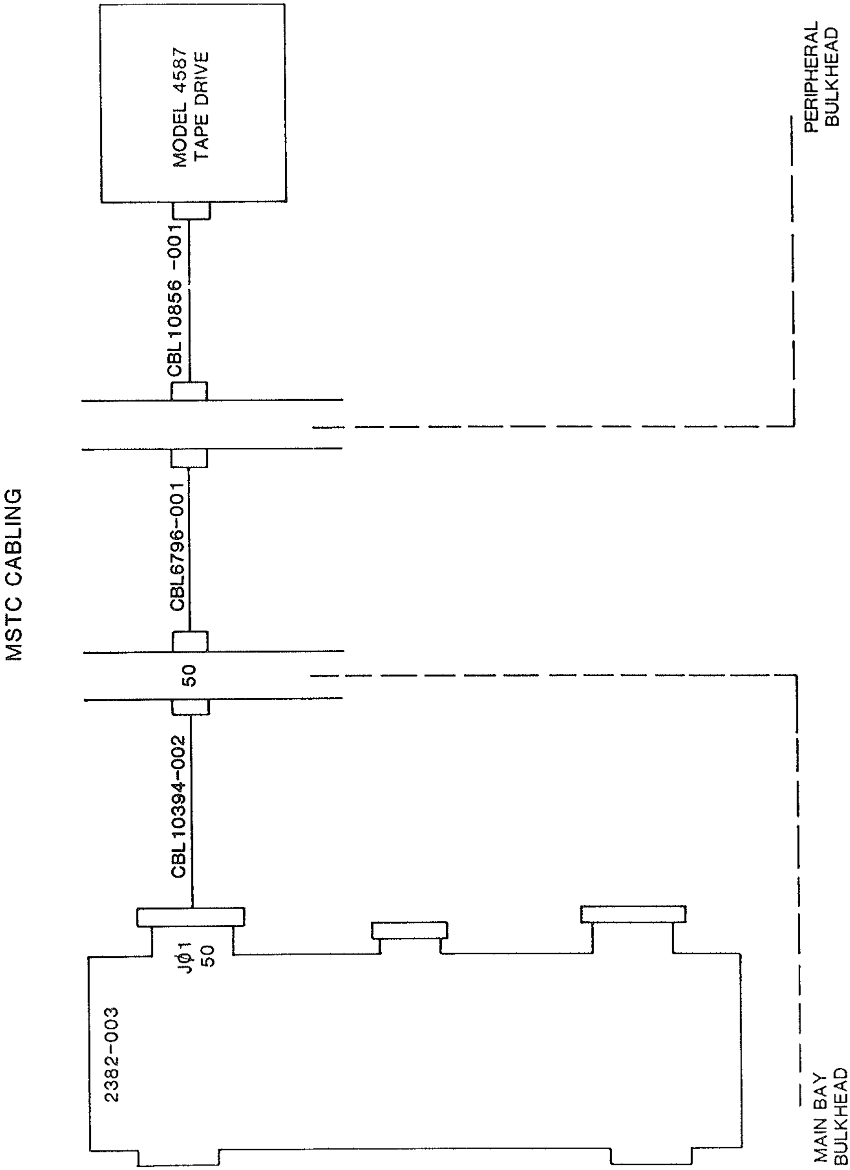


FIGURE 2-24: MSTC CABLING

3. Install the ICS3 card cage. Refer to Installing the ICS3 Card Cage. Some standard factory builds are shipped with the ICS3 card cage pre-installed in the mainbay or peripheral cabinet. If your ICS3 card cage is pre-installed, use this section to verify proper installation and cabling before powering up the system.

4. Transfer the ICS3 card cage, if necesssary. In some instances, the customer may choose to transfer an ICS3 card cage from the mainbay to a 30-inch or 53-inch peripheral cabinet, from a 30-inch peripheral cabinet to a mainbay, or from a 30-inch peripheral cabinet to a 53-inch peripheral cabinet. Special kits are available to help you complete the task. Refer to Transferring the ICS3 Card Cage. This section contains the following transfer procedures:

   - Mainbay to 30-Inch Peripheral Cabinet
   - Mainbay to 53-Inch Peripheral Cabinet
   - 30-Inch Peripheral Cabinet to Mainbay
   - 30-Inch to 53-Inch Peripheral Cabinet

   CAUTION

   ICS3 card cages installed in a mainbay cabinet are cooled differently than card cages installed in a peripheral cabinet. Failure to follow the installation procedures and cautions in this section could lead to thermal shutdown of the ISC3 subsystem or overheating of the system cabinet.

5. Install Line Adapter Cards (LACs). Refer to Installing Line Adapter Cards. This section also contains card cage priority information that you will need to know.

6. Install peripheral devices. Refer to Cabling Devices to the ICS3 for peripheral device installation information.

7. Perform final checkout. Refer to Intelligent Communications Subsystems Service Manual (SMN250-B) for a detailed ICS3 checkout procedure.

2.8.6.2 Verifying ICS3 Configuration

Verify configuration of the following ICS3 components:

- Controller Board
- Buffer Card
- LAC Bus Backplane

2.8.6.2.1 Controller Board (ICS3)

Use the following ICS3 controller board items to verify controller configuration:

- Memory Header DIP
- Device Address DIP Switch

The memory header DIP, located at 23L on the ICS3 controller board (TLA10021-002), encodes the board revision level and the memory size. The ICS3 controller board's memory consists of two banks of on-board 256K Dynamic Random Access Memory (DRAM).

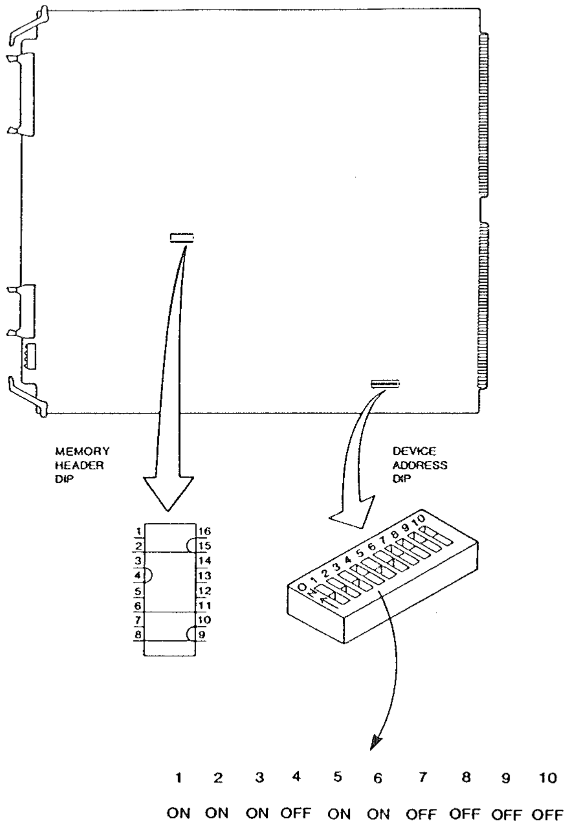
Using Figure 2-25, verify that the memory header DIP on the ICS3 controller board, is properly wired (jumpered) to reflect the memory size of the board.

The device address DIP switch, located at 03D on the ICS3 controller board, identifies the Programmable Input/Out (PIO) device address of the ICS3. PRIMOS recognizes a maximum of four ICS controller addresses.

Verify the ICS3 controller board device address using Tables 2-15 and 2-16. Refer to Figure 2-25 and Table 2-16 to ensure that the device address DIP switch settings reflect the device address determined from Table 2-15.

TABLE 2-15: ICS3 DEVICE ADDRESSES (OCTAL)

NO. OF ICS3s	ADDRESSES
1	'10
2	'10,'11
3	'10, '11, '36
4	'10,'11, '36, '37



ICS3 CONTROLLER BOARD DIPS

FIGURE 2-25: ICS3 CONTROLLER CONFIGURATION

TABLE 2-16: DEVICE ADDRESS DIP SETTINGS

SWITCH NUMBER	SWITCH POSITION			
	ADDRESS 10	ADDRESS 11	ADDRRESS 36	ADDRESS 37
1	ON	OFF	ON	OFF
2	ON	ON	OFF	OFF
3	ON	ON	OFF	OFF
4	OFF	OFF	OFF	OFF
5	ON	ON	OFF	OFF
6	ON	ON	ON	ON
7	OFF	OFF	OFF	OFF
8	OFF	OFF	OFF	OFF
9	OFF	OFF	OFF	OFF
10	OFF	OFF	OFF	OFF

OFF = Contact open (binary 1)
ON = Contact closed (binary 0)

2.8.6.2.2 Buffer Card (ICS3)

Resistor packages and jumpers at buffer card locations J03 and J04 determine the card's application in the card cage.

Table 2-17 lists the buffer card types and their card cage position. Refer to Figure 2-26 and Table 2-17 to verify that the preinstalled buffer card(s) matches the type needed for the ICS3 installation.

TABLE 2-17: ICS3 BUFFER CARD APPLICATIONS

CARD TYPE	CARD CAGE POSITION
ESA10031-002	1st Buffer Card
ESA10031-003	2nd Buffer Card

2.8.6.2.3 LAC Bus Backplane (ICS3)

A shorting plug at LAC bus backplane location J11 determines the upper LAC slot addresses. The ICS3 card cage's 16 LAC slots are physically contained on two separate backplanes.

Using Figure 2-27, verify that the preinstalled LAC bus backplane(s) matches the type needed for the ICS3 installation.

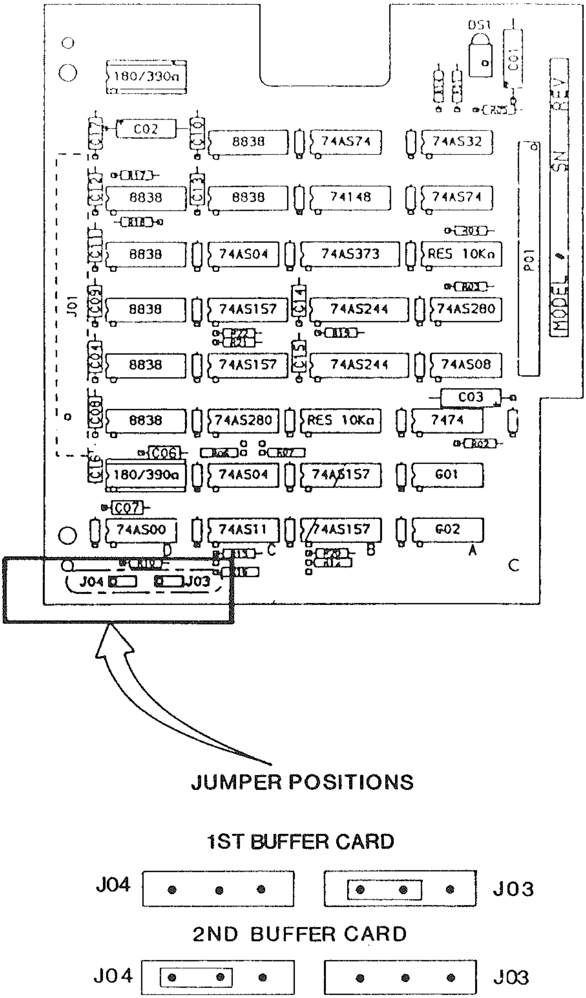


FIGURE 2-26: ICS3 BUFFER CARD CONFIGURATION

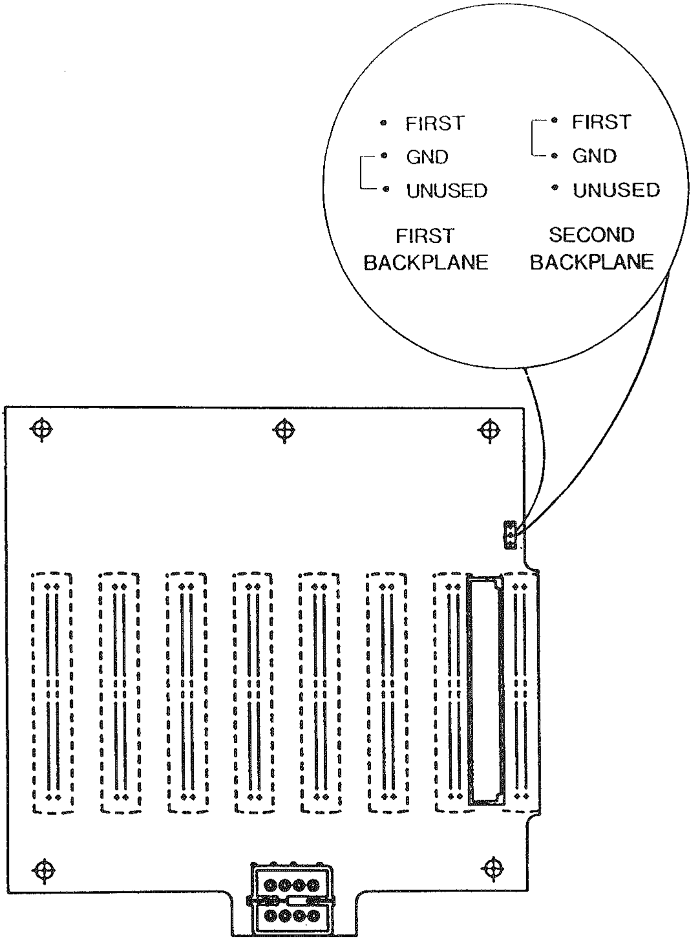


FIGURE 2-27: ICS3 LAC BACKPLANE CONFIGURATION

2.8.6.3 Installing the ICS3 Controller Board

To install the ICS3 controller board in the mainbay card cage, follow these steps:

1. Perform the ESD Procedure outlined previously in this chapter.

2. Remove the front panel, the floppy disk drive access door, and the top cover, then tilt open the rear door assembly (refer to Removing and Replacing System Cabinet Covers in Chapter 7 of this manual).

3. Holding the ICS3 board vertically with the component side facing left, install the board into the system chassis. Refer to I/O Configuration Guidelines in this chapter for controller board priority rules.

4. Select the step that applies to your installation:

   A) If you are installing the ICS3 card cage in the mainbay, connect P3 of CBL10136-002 to connector J02 on the ICS3 controller board (refer to Figure 2-28). Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough. Proceed to Installing the ICS3 Card Cage.

   B. If you are installing the ICS3 card cage in the peripheral cabinet, connect P1 of CBL10394-002 to connector J02 on the ICS3 controller board (refer to Figure 2-29). Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough. Then connect the free end to a 50 pin connector panel on the system bulkhead (refer to Figure 2-19 for a recommended bulkheading scheme). Proceed to Installing the ICS3 Card Cage.

2.8.6.4 Installing the ICS3 Card Cage

The following subsections provide procedures for installing the ICS3 card cage in the following:

- Model 4050/4150 Mainbay
- 30-Inch Peripheral Cabinet
- 53-Inch "S" Series Peripheral Cabinet

2.8.6.4.1 Installing an ICS3 in the Mainbay

To install the ICS3 16-slot card cage in the mainbay, follow these steps:

CAUTION

In mainbay installations, the ICS3 card cage is cooled by the Model 4050/4150's blower assembly. An exhaust tray (MEC10505-001) takes the place of the ICS3 fan tray (MSA10037-001) (see Figure 2-30).

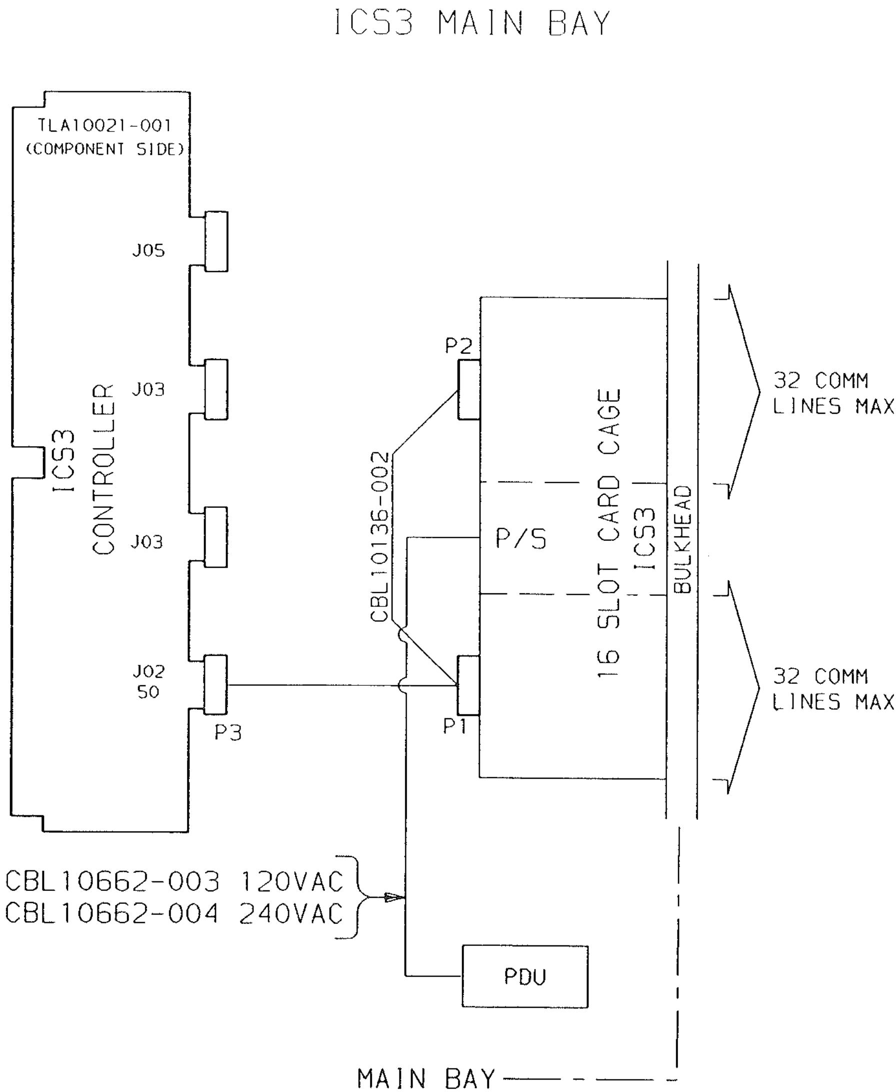


FIGURE 2-28: ICS3 MAINBAY CABLING DIAGRAM

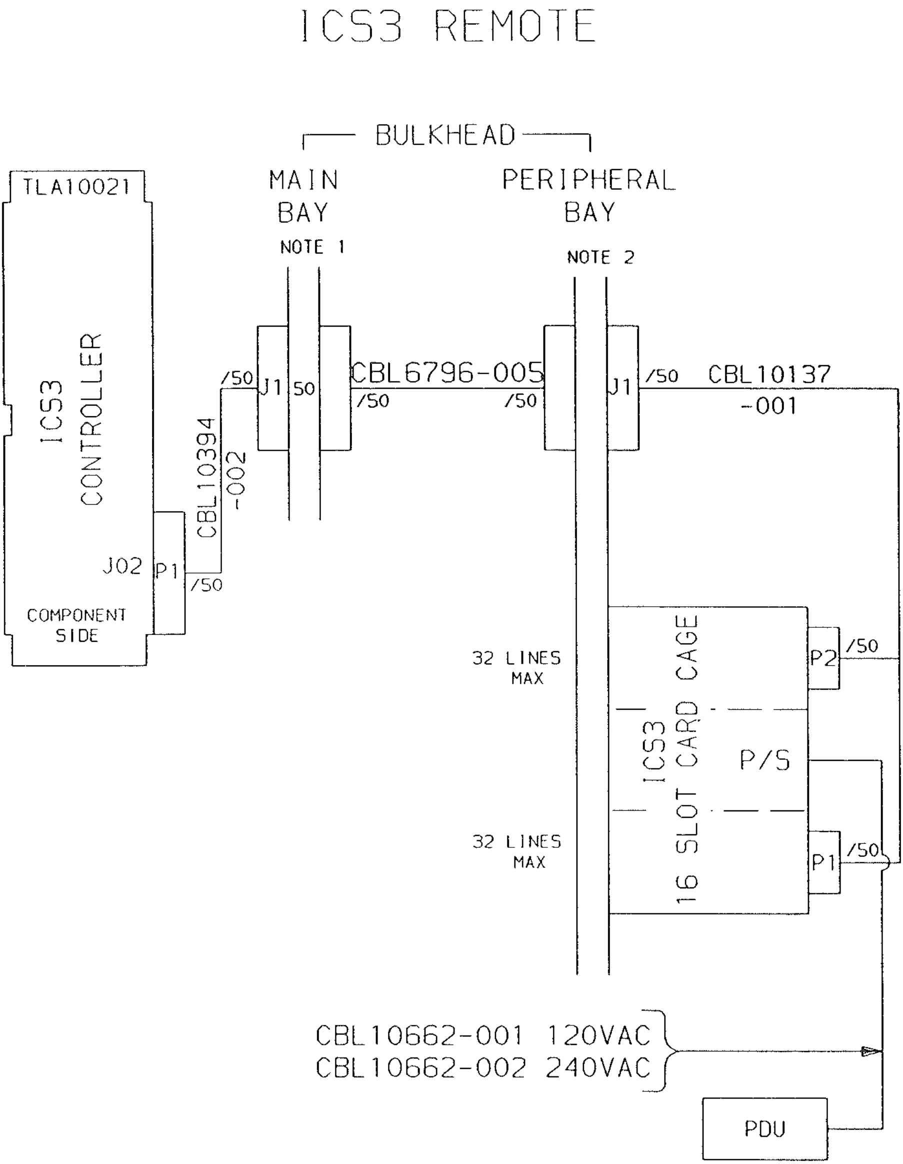


FIGURE 2-29: ICS3 PERIPHERAL BAY CABLING

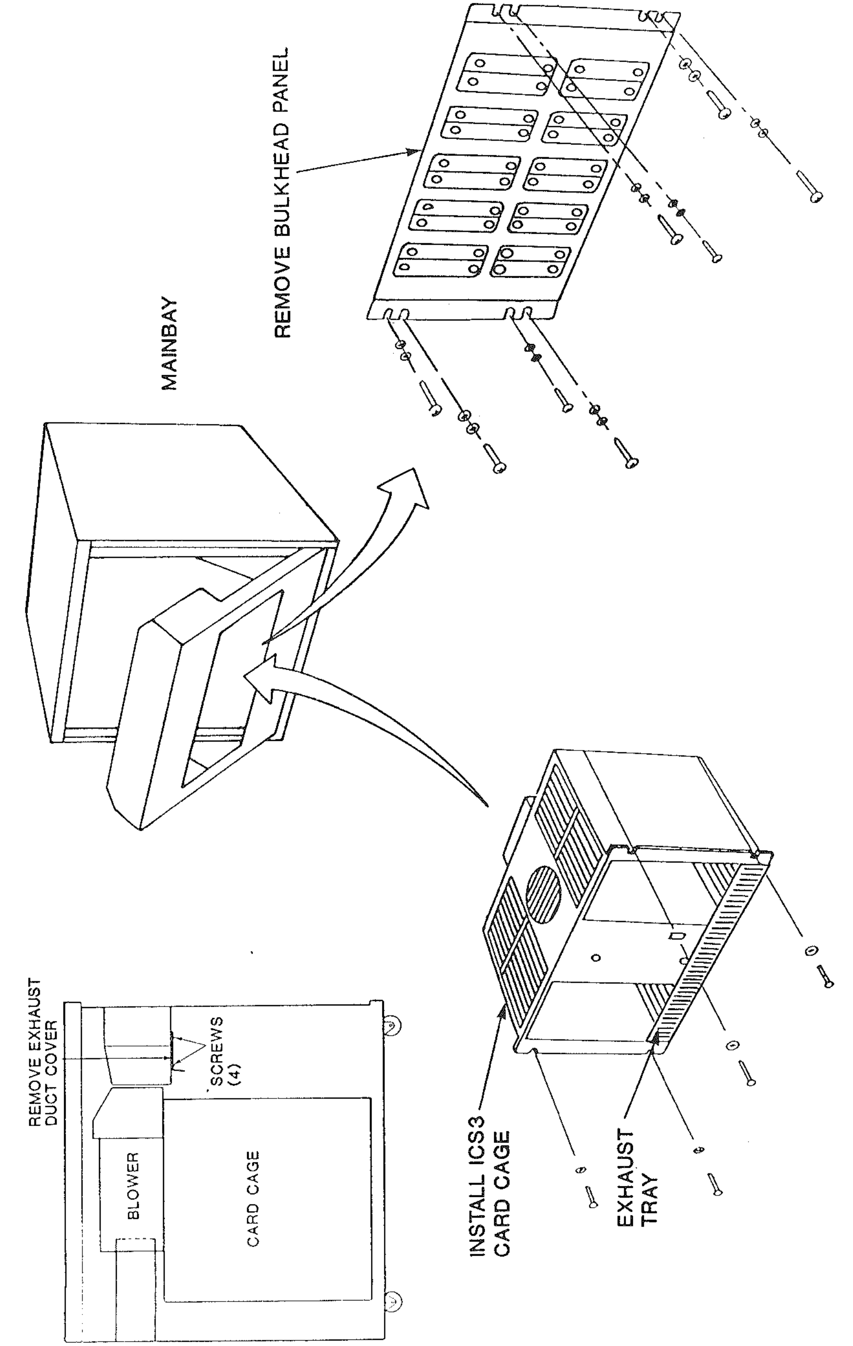


FIGURE 2-30: ICS3 CARD CAGE INSTALLATION (MAINBAY)

1. Loosen and remove the four screws securing the two-row bulkhead panel to the rear door assembly. Remove the bulkhead panel (see Figure 2-30).

2. Remove the four screws that secure the exhaust duct cover (MEC10476) to the exhaust duct (see Figure 2-30).

3. Verify that exhaust tray MEC10505-001 is secured in place at the bottom of the ICS3 card cage assembly. Refer to ICS3 Fan Tray Removal/Replacement in Chapter 7 of this manual for fan tray removal procedures, if necessary.

4. Guide the 16-slot card cage through the bulkhead opening (see Figure 2-30).

5. Insert and tighten the four screws securing the card cage to the cabinet (see Figure 2-30).

6. Unlock the two quarter-turn fasterners securing the rear door assembly and tilt open the rear door.

7. Ensure that the ac push button on the ICS3 card cage (see Figure 2-30) is in the OFF position (button fully extended).

8. Connect P1 and P2 of CBL10136-002 to ICS3 buffer cards (refer to Figure 2-31). The other end is already connected to J02 of the ICS3 controller board.

9. Locate the PDU adapter cable CBL10662. The -003 suffix denotes 120 Vac for domestic installations. The -004 suffix denotes 240 Vac for international installations.

10. Plug one end of CBL10662 securely into the card cage power supply (see Figure 2-31).

11. Connect the free end into connector J5 (PERIPH) of the PDU (see Figure 2-12).

12. Return the rear door assembly to its full upright position.

13. Proceed to the Line Adapter Card (LAC) Installation.

2.8.6.4.2 Installing an ICS3 in a 30-Inch Peripheral Cabinet

Before installing an ICS3 in a peripheral cabinet, refer to Peripheral Cabinet Configuration Guidelines to determine the zone required for installation.

To install the ICS3 16-slot card cage in a 30-inch peripheral cabinet, follow these steps:

1. Power down the peripheral cabinet.

2. From the rear of the cabinet, remove the rear panel by removing the top two Phillips screws and loosening the bottom two screws (see Figure 2-32).

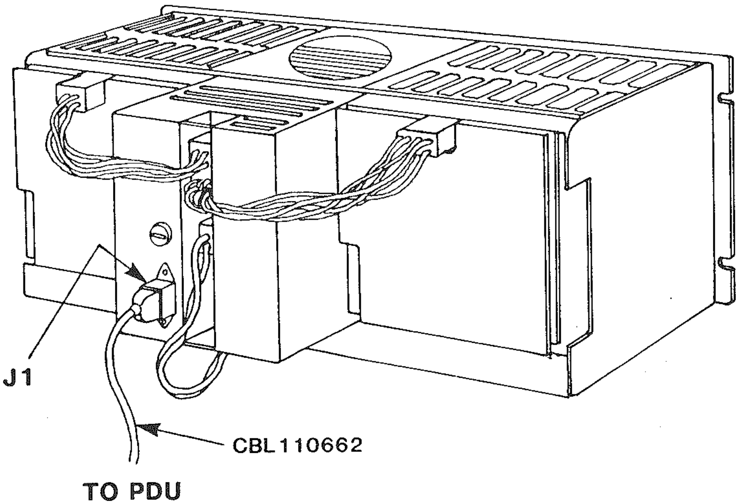


FIGURE 2-31: ICS3 CARD CAGE POWER CABLING

NOTE

If you are installing the card cage in Zone 3, remove the lower cover plate in the next step. If you are installing the card cage in Zone 4, remove the upper cover plate.

3. Remove the four Phillips screws that secures the appropriate rear panel cover plate to the rear panel (see Figure 2-32). This step creates an opening to access the ICS3 LAC cards once the unit and rear panel are installed.

4. Verify that the card cage fan tray assembly (MSA10037-001) is secured to the bottom of the card cage assembly.

5. Place the card cage on the floor directly in front of the peripheral bulkhead. Ensure that the ac push button on the card cage is in the OFF position (button fully extended).

6. Connect P1 and P2 of controller board interface cable CBL10137-001 to the ICS3 buffer cards (see Figure 2-29). Feed the free end (J1) into the cabinet into the narrow space between the cabinet chassis and the left or right side panel. Connect J1 to a 50 pin panel inside the peripheral cabinet bulkhead (see Figure 2-19 for a recommended bulkheading scheme).

7. Locate the PDU adapter cable CBL10662. The -001 suffix denotes 120 Vac for domestic installations. The -002 suffix denotes 240 Vac for international installations.

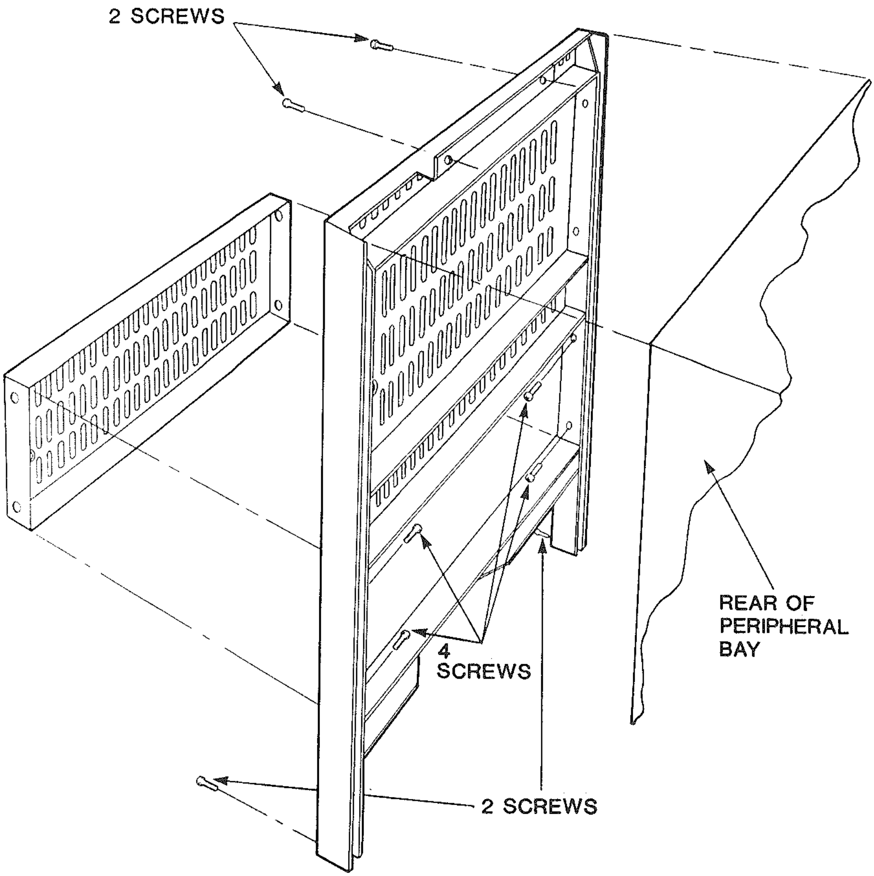


FIGURE 2-32: PERIPHERAL BAY REAR PANEL REMOVAL

8. Plug one end of CBL10662 securely into the card cage power supply (see Figure 2-31). Feed the free end into the narrow space between the cabinet chassis and the left or right side panel.

9. Refer to Table 2-18 to identify the correct position of the top two card cage holes on the mounting rail. Datum 0 is the topmost hole on the mounting rail. Be sure to mark the location on the rail before proceeding to the next step.

TABLE 2-18: MOUNTING RAIL HOLE LOCATIONS

	ZONE 3	ZONE 4
Inches From Datum 0	12.88	2.38
Holes From Datum 0	22	4

10. Guide the 16-slot card cage into the rear of the cabinet until the card cage rests against the mounting rail (see Figure 2-33).

11. Insert and tighten the screws securing the card cage to the cabinet (see Figure 2-33).

12. Replace the peripheral cabinet rear panel, and secure it in place with four Phillips screws.

13. Connect one end of cabinet interface cable CBL6796-005 to the peripheral cabinet bulkhead panel. Connect the free end to the mainbay bulkhead panel (see Figure 2-29).

14. From the front of the cabinet, remove the lower cover panel from its ball stud fasteners, then remove the two screws that secure the cover plate to the cabinet chassis to access the peripheral device power cables.

15. Reach into the opening and locate the free end of power cable CBL10662. Connect the cable to peripheral cabinet PDU (see Figure 2-12).

16. Proceed to Line Adapter Card (LAC) Installation.

2.8.6.4.3 Installing an ICS3 in a 53-Inch Peripheral Cabinet

To install the ICS3 16-slot card cage in a 53-inch "S" series (tilt-bulkhead) peripheral cabinet, follow these steps:

1. Power down the 53-inch peripheral cabinet.

2. Using a Phillips screwdriver, loosen and remove the four screws securing the bulkhead cover plate at the rear of the cabinet. Remove the cover plate.

3. Using a Phillips screwdriver, insert and tighten the screws securing the narrow filler cover plate to the cabinet rails (see Figure 2-34).

4. Verify that the card cage fan tray assembly (MSA10037-001) is secured to the bottom of the card cage assembly, then guide the 16-slot card cage through the bulkhead opening (see Figure 2-35).

5. Using a Phillips screwdriver, insert and tighten the screws securing the card cage to the cabinet (see Figure 2-35).

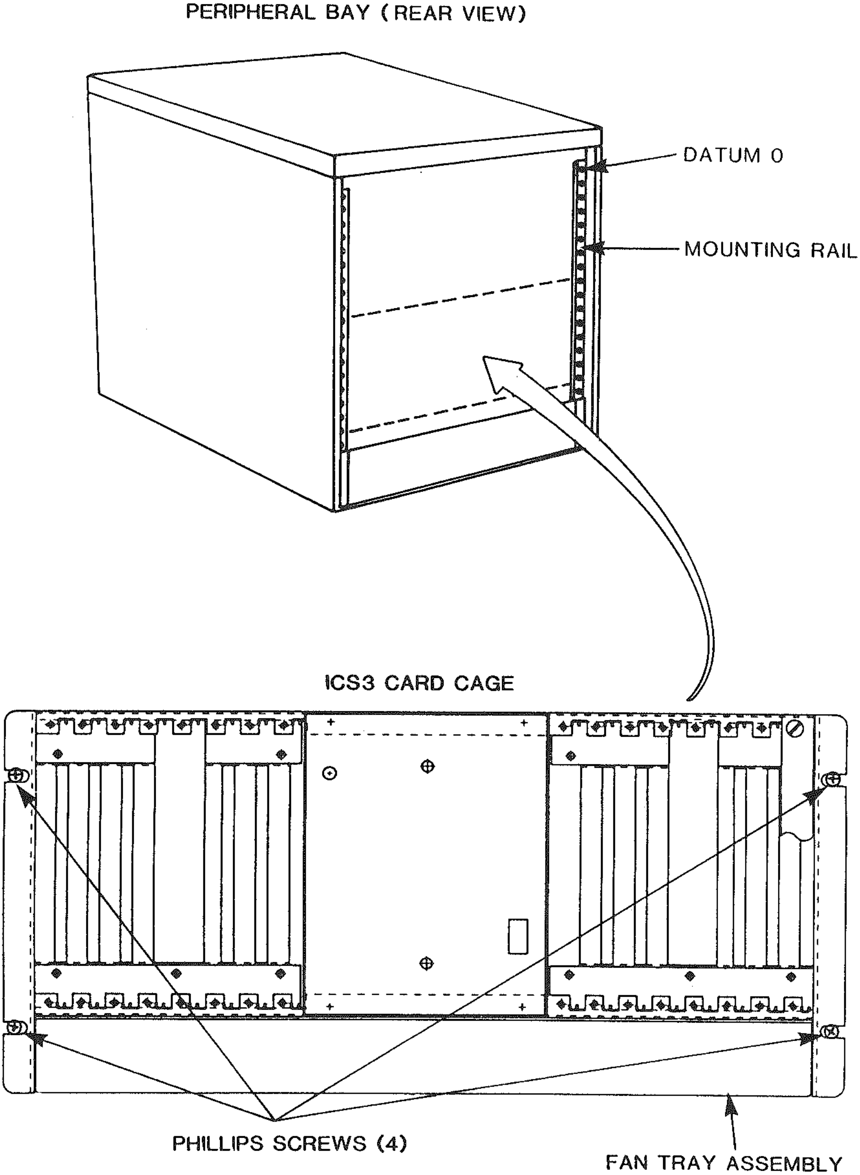


FIGURE 2-33: ICS3 CARD CAGE INSTALLATION (PERIPHERAL BAY)

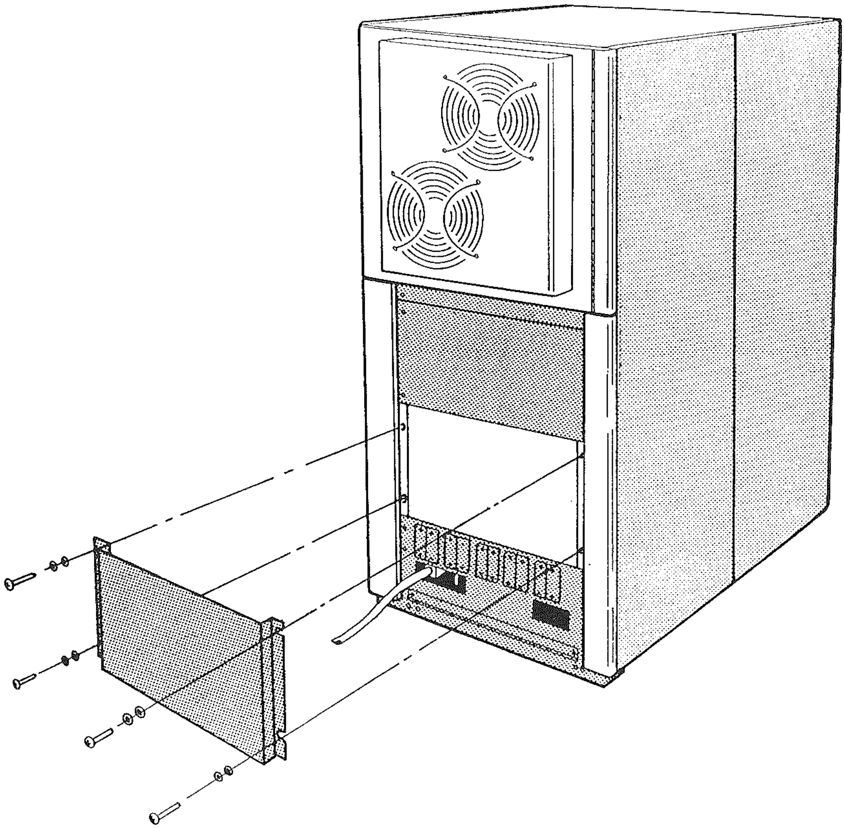


FIGURE 2-34: 53-INCH PERIPHERAL BAY COVER PLATE REMOVAL

6. Open the top rear door panel of the 53-inch peripheral cabinet.

7. Pull the spring-loaded pins located on both sides of the "tilt-bulkhead panel" inward, and tilt the bulkhead.

8. Connect P1 and P2 of controller board interface cable CBL10137-001 to the ICS3 buffer cards. Connect the free end (J1) to a 50 pin panel inside the peripheral cabinet bulkhead.

9. Locate the PDU adapter cable (CBL10368-001).

10. Plug cable end J1 securely into the power supply of the card cage.

11. Connect the adapter cable's 5-pin connector into one of the unused power supply cards (PCB10106-001) located in the peripheral cabinet's PDU (ESA10175-001) (see Figure 2-29).

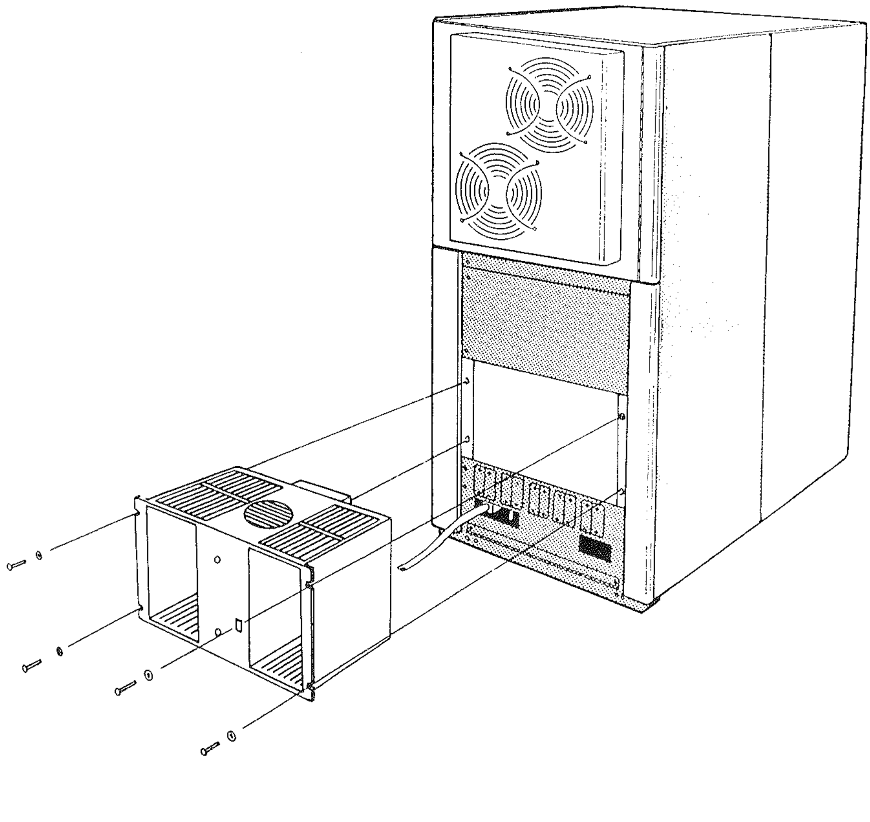


FIGURE 2-35: ICS3 CARD CAGE INSTALLATION (53-INCH PERIPHERAL BAY)

12. Return the "tilt-bulkhead" to its full upright position, and ensure that the spring-loaded pins lock.

13. Close the top rear door panel of the 53-inch peripheral cabinet.

14. Connect the ICS3 bulkhead-to-bulkhead cable CBL6796-005 to J1 on the 53-inch cabinet (see Figure 2-29)

15. Proceed to Line Adapter Card (LAC) Installation.

2.8.6.5 Installing ICS3 Line Adapter Cards (LACs)

To install the first 8 LACs (6.5 by 5-inches) into the ICS3 card cage, proceed as follows:

NOTE

> Asynchronous LAC CLAC304 (ESA10063-001) of Rev. C or greater is required in the Model 4050/4150 to provide proper EMI shielding.

1. Separate the synchronous LACs from the asynchronous LACs. The synchronous LACs have two 25-pin D-type connectors mounted onto the card. The asynchronous LACs have four 9-pin D-type connectors.

2. Select a card cage chassis slot for each line adapter card. LAC slot positions are based on service priority and are generally assigned according to the list of communication types that follows (see Figure 2-36). The communication types are listed from highest to lowest priority:

   - Block mode asynchronous

   - Bisynchronous-framed X.25 or Remote Job Entry (RJE)

   - Synchronous Data Link Controller (SDLC)

     PRIME/SNA and High-level Data Link Controller (HDLC)

   - Asynchronous

   Place higher speed lines of each group into higher priority slots.

3. Hold the LAC card vertically, component-side facing left (see Figure 2-37).

4. Align the card with the upper and lower card guides of the chosen card cage chassis slot and insert the card until the rear edge connector contacts the LAC backplane.

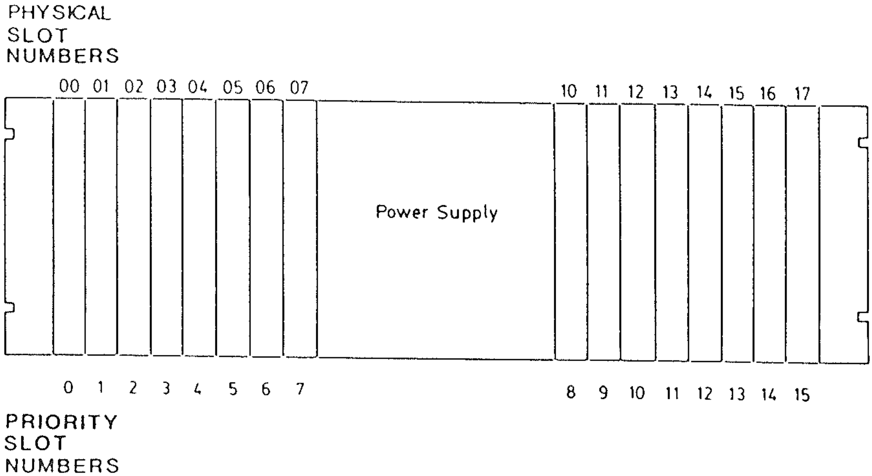


FIGURE 2-36: ICS3 LAC PRIORITY

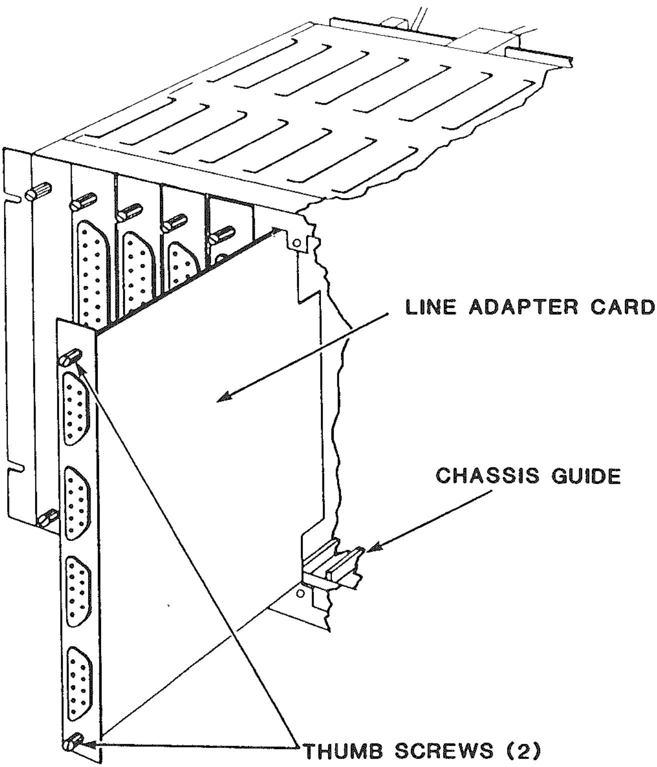


FIGURE 2-37: ICS3 LAC INSTALLATION

5. Seat the LAC and hand tighten the top and bottom thumb screws. DO NOT overtighten (see Figure 2-37).

6. Perform steps 3 through 5 on all LACs.

7. Proceed to Cabling Devices to the ICS3.

2.8.6.6 Cabling Devices to the ICS3

LACs provide direct connection to peripheral devices (terminals, printers, or modems) by means of device cables.

To cable I/O devices to ICS3 LACs, refer to Figure 2-38.

2.8.6.7 Transferring ICS3 Card Cage

This section provides procedures for transferring an ICS3 card cage from one cabinet to another. The following transfer procedures are described:

- From the 4050/4150 mainbay to a 30-inch peripheral cabinet
- From the 4050/4150 mainbay to a 53-inch "S" series peripheral cabinet
- From a 30-inch peripheral cabinet to the mainbay.
- From a 30-inch peripheral cabinet to a 53-inch "S" series peripheral cabinet

Refer to the subsections that follow for transfer kit numbers and procedures.

2.8.6.7.1 Card Cage Transfer From Mainbay to 30-Inch Peripheral Bay

Transferring an ICS3 card cage from the 4050/4150 mainbay to a 30-inch peripheral cabinet requires conversion kit KIT10159-001.

Table 2-19 lists kit components:

TABLE 2-19: ICS3 CARD CAGE TRANSFER KIT KIT10159-001 PARTS

COMPONENT	PART NUMBER
Exhaust Duct Cover	MEC10476-001
Fan Tray	MSA10037-001
Bulkhead-to-Bulkhead Cable	CBL6796-005
Controller-to-Bulkhead Cable	CBL10394-002
Bulkhead to Card Cage Cable	CBL10137-001
Two-Row Bulkhead Panel	MEC10474
Assorted Bulkhead Panels	
Mounting Hardware	

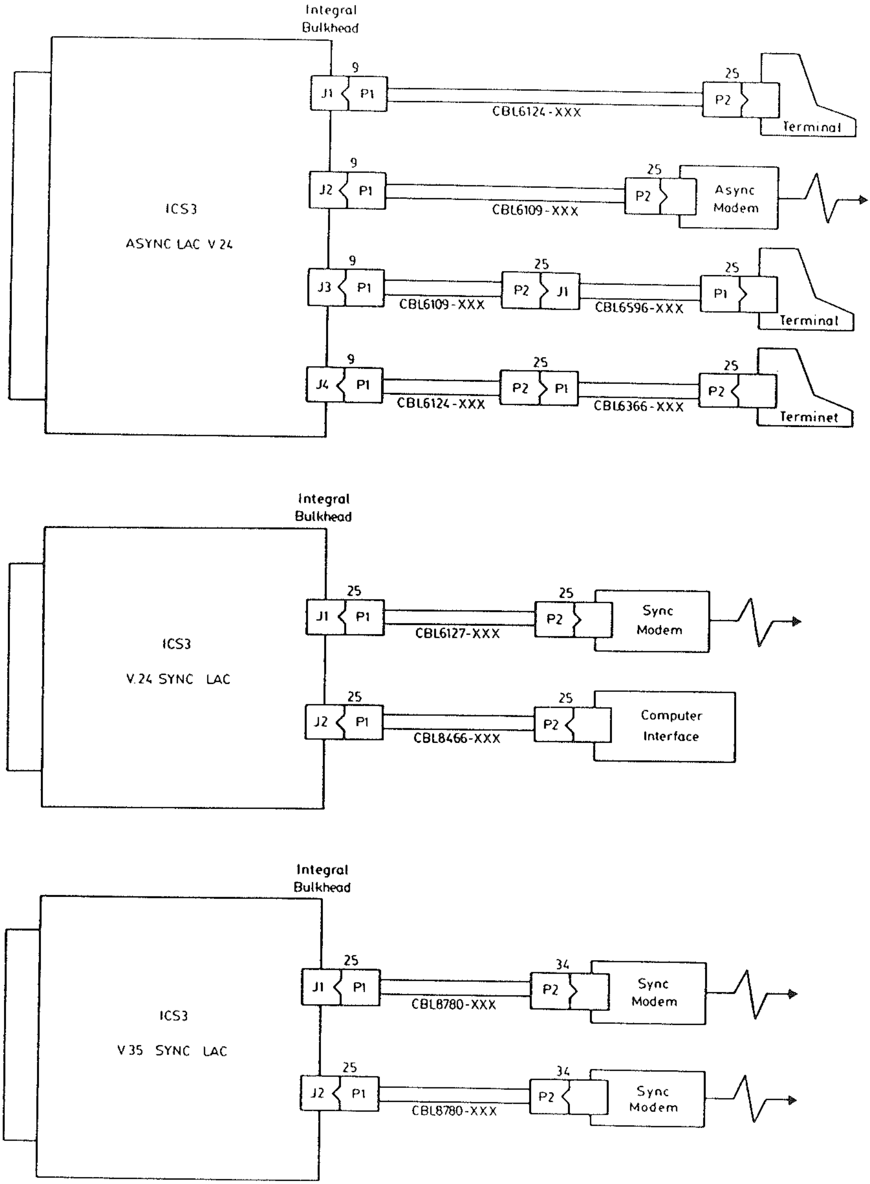


FIGURE 2-38: ICS3 DEVICE CABLING

To transfer the card cage, follow these steps:

1. Power down the system and remove the ICS3 card cage from the mainbay bulkhead (refer to Removing and Replacing the ICS3 in Chapter 7 of this manual).

2. Install exhaust duct cover MEC10476-001 on the mainbay tilt bulkhead (see Figure 2-39).

   CAUTION

   Failure to install the exhaust duct cover will recirculate exhaust air through the cabinet and will cause overtemperature conditions.

3. Install the two-row bulkhead panel to cover the opening left by the ICS3 card cage on the mainbay tilt bulkhead.

4. Replace ICS3 exhaust tray MEC10505-001 with ICS3 fan tray MEC10037-001 by following these steps:

   CAUTION

   Installation of an ICS3 in a peripheral cabinet without the fan tray will cause the ICS3 to overheat and fail.

   A) Remove the four screws securing the exhaust tray assembly to the ICS3 card cage chassis.

   B) Pull the tray assembly forward and remove it from the ICS3 card cage chassis.

   C) Slide the fan tray assembly (from the front) into the card cage chassis.

   D) Insert and tighten the four screws securing the fan tray assembly to the card cage chassis.

   E) Connect the fan tray assembly's dc power cable (CBL10153-001) to the power supply.

5. At the mainbay, remove the front panel, the floppy disk drive access door, and the top cover (refer to Removing and Replacing System Cabinet Covers in Chapter 7 of this manual).

6. Disconnect and remove CBL10136-002 from the ICS3 controller board and the card cage.

7. Connect P1 of CBL10394-002 to connector J02 on the ICS3 controller board (refer to Figure 2-29). Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough. Then connect the free end to a 50 pin connector panel on the system bulkhead (refer to Figure 2-19 for a recommended bulkheading scheme).

8. Refer to Installing an ICS3 in the 30-Inch Peripheral Cabinet in this chapter for card cage installation and bulkheading instructions.

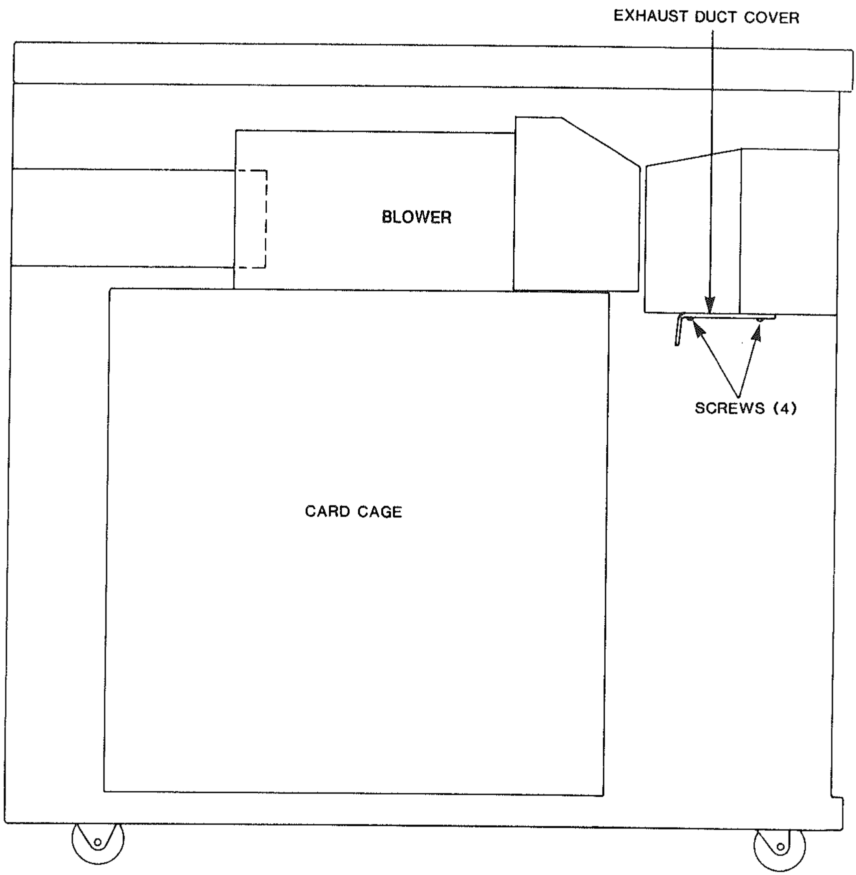


FIGURE 2-39: EXHAUST DUCT COVER INSTALLATION

2.8.6.7.2 Card Cage Transfer From Mainbay to 53-Inch Peripheral Bay

Transferring an ICS3 card cage from the 4050/4150 mainbay to a 53-inch peripheral cabinet requires conversion kit KIT10173-001.

Table 2-20 lists kit components:

TABLE 2-20: ICS3 CARD CAGE TRANSFER KIT KIT10173-001 PARTS

COMPONENT	PART NUMBER
Exhaust Duct Cover	MEC10476-001
Fan Tray	MSA10037-001
Bulkhead-to-Bulkhead Cable	CBL6796-005
Controller-to-Bulkhead Cable	CBL10394-002
Bulkhead to Card Cage Cable	CBL10137-001
Two-Row Bulkhead Panel	MEC10474
Assorted Bulkhead Panels	
Mounting Hardware	

To transfer the card cage, follow these steps:

1. Power-down the system and remove the ICS3 card cage from the mainbay bulkhead (refer to Removing and Replacing the ICS3 in Chapter 7 of this manual).

2. Install exhaust duct cover MEC10476-001 on the mainbay tilt bulkhead (see Figure 2-39).

CAUTION

Failure to install the exhaust duct cover will recirculate exhaust air through the cabinet and will cause overtemperature conditions.

3. Install the two-row bulkhead panel to cover the opening left by the ICS3 card cage on the mainbay tilt bulkhead.

4. Replace ICS3 exhaust tray MEC10505-001 with ICS3 fan tray MEC10037-001 by following these steps:

CAUTION

Installation of an ICS3 in a peripheral cabinet without the fan tray will cause the ICS3 to overheat and fail.

A) Remove the four screws securing the exhaust tray assembly to the ICS3 card cage chassis.

B) Pull the tray assembly forward and remove it from the ICS3 card cage chassis.

C) Slide the fan tray assembly (from the front) into the card cage chassis.

D) Insert and tighten the four screws securing the fan tray assembly to the card cage chassis.

E) Connect the fan tray assembly's dc power cable (CBL10153-001) to the power supply.

5. At the mainbay, remove the front panel, the floppy disk drive access door, and the top cover (refer to Removing and Replacing System Cabinet Covers in Chapter 7 of this manual).

6. Disconnect and remove CBL10136-002 from the ISC3 controller board and the card cage.

7. Connect P1 of CBL10394-002 to connector J02 on the ICS3 controller board (refer to Figure 2-29). Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough. Then connect the free end to a 50 pin connector panel on the system bulkhead (refer to Figure 2-19 for a recommended bulkheading scheme).

8. Refer to Installing an ICS3 in the 53-Inch Peripheral Cabinet in this chapter for card cage installation and bulkheading instructions.

2.8.6.7.3 Card Cage Transfer From 30-Inch Peripheral Bay to Mainbay

Transferring an ICS3 card cage from the 30-inch peripheral cabinet to the 4050/4150 mainbay requires conversion kit KIT10217-001.

Table 2-21 lists kit components:

TABLE 2-21: ICS3 CARD CAGE TRANSFER KIT KIT10217-001 PARTS

COMPONENT	PART NUMBER
Exhaust Tray	MEC10505-001
Controller-to-Buffer Cards Cable	CBL10136-002
Assorted Bulkhead Panels	
Mounting Hardware	

To transfer the card cage, follow these steps:

1. Power-down the mainbay and peripheral cabinet.

2. Disconnect the ICS3 bulkhead-to-bulkhead cable CBL6796-005.

3. Disconnect and remove the ICS3 power and controller cables, then remove card cage from the peripheral cabinet bulkhead (refer to Removing and Replacing the ICS3 in Chapter 7 of this manual).

4. Remove the ICS3 fan tray MEC10037-001 from the bottom of the card cage and install ICS3 exhaust tray MEC10505-001 in its place by following these steps.

   A) Disconnect the fan tray assembly's dc power cable (CBL10153-001) from the power supply.

   B) Remove the four screws securing the fan tray assembly to the ICS3 card cage chassis.

C) Pull the tray assembly forward and remove it from the ICS3 card cage chassis.

D) Slide the exhaust tray assembly (from the front) into the card cage chassis.

E) Insert and tighten the four screws securing the exhaust tray assembly to the card cage chassis.

5. At the mainbay, remove the front panel, the floppy disk drive access door, and the top cover (refer to Removing and Replacing System Cabinet Covers in Chapter 7 of this manual).

6. Disconnect and remove CBL10394-002 from the ISC3 controller board and the mainbay bulkhead.

7. Connect P1 of CBL10136-002 to connector J02 on the ICS3 controller board (refer to Figure 2-28). Feed the cable through a vacant slot in the cable dress comb and into the wireform cable trough.

8. Refer to Installing an ICS3 in the Mainbay Cabinet in this chapter for card cage installation and bulkheading instructions.

2.8.6.7.4 Card Cage Transfer From 30-Inch To 53-Inch Peripheral Bay

Transferring an ICS3 card cage from a 30-inch peripheral cabinet to a 53-inch peripheral cabinet requires conversion kit KIT10174-001.

Table 2-22 lists kit components:

TABLE 2-22: ICS3 CARD CAGE TRANSFER KIT KIT10174-001 PARTS

COMPONENT	PART NUMBER
Mounting Hardware	KIT10131-001

To transfer the card cage, follow these steps:

1. Power-down the 30-inch peripheral cabinet.

2. Disconnect the ICS3 bulkhead-to-bulkhead cable CBL6796-005 from J1 on the 30-inch peripheral cabinet.

3. Remove the rear panel from the 30-inch peripheral cabinet and install the filler panel.

4. Disconnect and remove the ICS3 power and controller cables, then remove card cage from the 30-inch peripheral cabinet rails (refer to Removing and Replacing the ICS3 in Chapter 7 of this manual).

5. Power down the 53-inch peripheral cabinet.

6. Using a Phillips screwdriver, loosen and remove the four screws securing the bulkhead cover plate at the rear of the cabinet. Remove the cover plate (see Figure 2-34).

7. Using a Phillips screwdriver, insert and tighten the screws securing the narrow filler cover plate to the cabinet rails.

8. Guide the 16-slot card cage through the bulkhead opening (see Figure 2-35).

9. Using a Phillips screwdriver, insert and tighten the screws securing the card cage to the cabinet.

10. Open the top rear door panel of the 53-inch peripheral cabinet.

11. Pull the spring-loaded pins located on either side of the tilt-bulkhead panel inward, and tilt the bulkhead.

12. Connect P1 and P2 of controller board interface cable CBL10137-001 to the ICS3 buffer cards. Connect the free end (J1) to a 50 pin panel inside the peripheral cabinet bulkhead.

13. Locate the PDU adapter cable (CBL10368-001).

14. Plug cable end J1 securely into the power supply of the card cage.

15. Connect the adapter cable's 5-pin connector into one of the unused power supply cards (PCB10106-001) located in the peripheral cabinet's PDU (ESA10175-001).

16. Return the tilt-bulkhead to its full upright position, and ensure that the spring-loaded pins lock.

17. Close the top rear door panel of the 53-inch peripheral cabinet.

18. Reconnect the ICS3 bulkhead-to-bulkhead cable CBL6796-005 to J1 on the 53-inch cabinet.

2.8.7 CONFIGURING AND CABLING THE PRIMENET NODE CONTROLLER (PNC)

The Model 4050/4150 can support a PNC and PRIMENET software that connects the system to a local ring network. A maximum of 128 systems can be configured in this ring. This subsection provides procedures for installing the PNC subsystem, which includes the following:

- PNC/PNC-II Controller Board
- PNC Modular Junction/Relay Box and Cable

NOTE

Systems must be no further than 750 feet apart to allow the network to continue to function should one node fail.

The Model 4050/4150 system requires the PNC <u>modular</u> junction box (ESA10046-001).

2.8.7.1 Configuring the PNC Controller

The PNC controller address is factory pre-configured to '07. Configuration is not required.

2.8.7.2 Installing the PNC/PNC-II Controller Board

To install the PNC/PNC-II board in the system card cage, follow these steps:

1. Slide the controller into the appropriate I/O slot in the system chassis. Refer to I/O Configuration Guidelines in this chapter for slot selection rules. The PNC board should occupy a low priority slot.

2. Using the board ejector keys, seat the board firmly in the backplane.

3. Connect one end of control cable CBL10395-002 to connector CD on the controller board (see Figure 2-40).

4. Feed the cable through a vacant slot in the cable dress comb, into the wireform cable trough, and down into the opening between the bulkhead and the backplane.

5. Proceed to PNC Modular Junction Box Installation.

2.8.7.3 Installing the PNC Modular Junction Box

Install the PNC modular junction box into the system bulkhead panel. To install the junction box, complete the following procedure (refer to Figure 2-41):

1. Remove the cover plate from the system bulkhead (refer to Figure 2-41).

2. Install the MJ-Box in the bulkhead cutout and secure it in place with four screws.

3. Tilt open the rear door assembly.

4. Connect the free end of controller cable CBL10395-002 to the rear of the junction box.

5. Connect the twinax cables to the junction box. Be sure to couple the input and output cables correctly.

6. Toggle the manual disconnect switch to NORMAL.

For installation checkout and corrective maintenance procedures refer to PRIMENET Node Controller Service Module (SMN601).

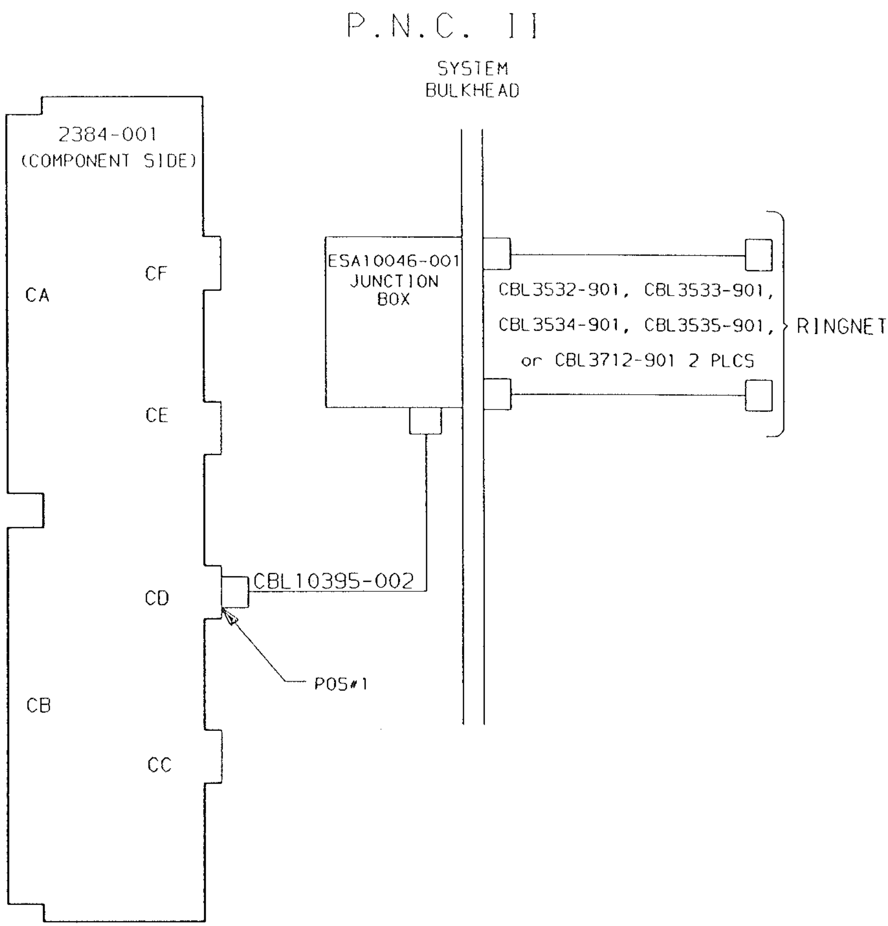


FIGURE 2-40: PNC-II CABLING

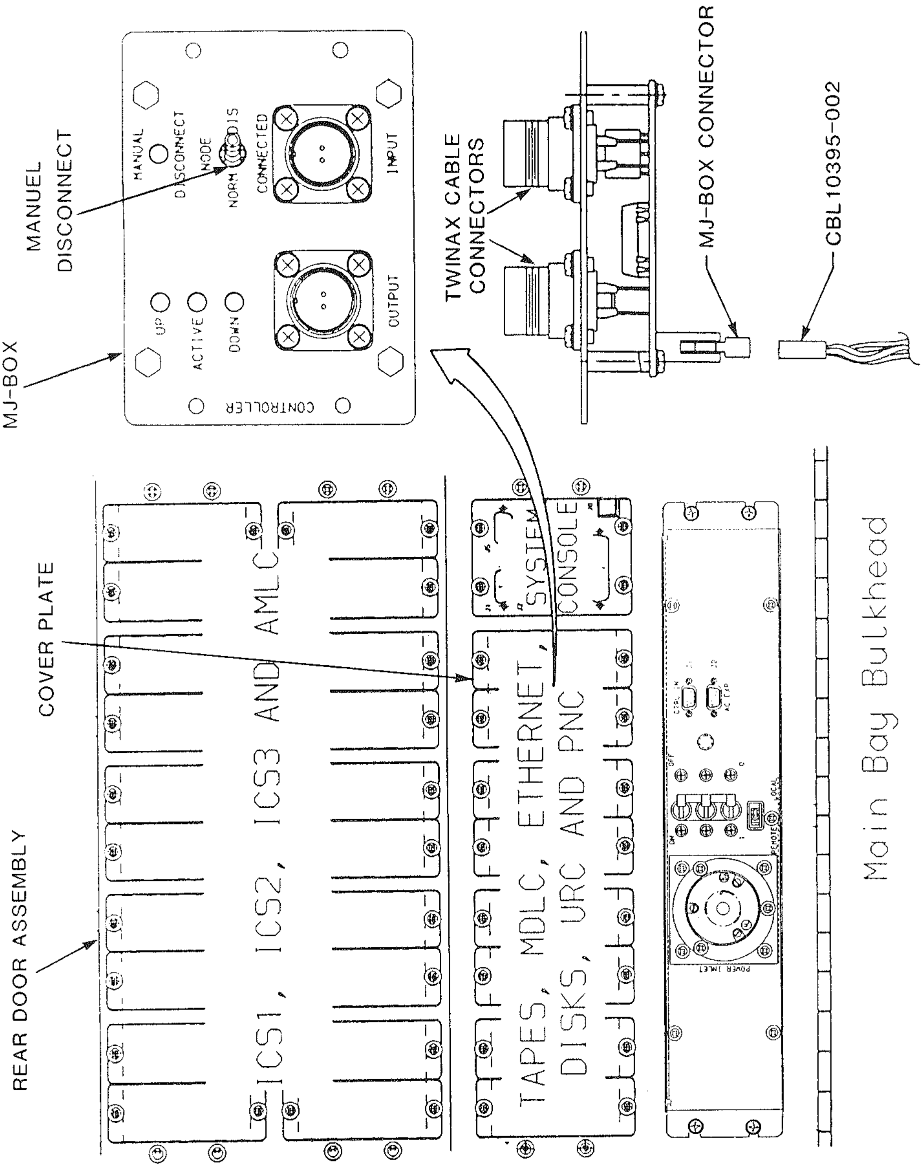


FIGURE 2-41: PNC MJ-BOX INSTALLATION

2.8.8 INSTALLING THE LHC300 CONTROLLER

Refer to LAN300 Local Area Network Service Manual (SMN603) for LHC300 controller installation procedures.

2.8.9 INSTALLING THE MODEL 4735 (496 MB) DISK DRIVE

Model 4735 disk drives are generally shipped preconfigured and partially cabled in the model 7730H 30-inch peripheral cabinet, or as an add-on drive in a separate shipping carton. This section provides procedures to verify configuration and complete the cabling of a pre-installed drive, and to configure, install and cable a Model 4735 disk drive as an expansion of an existing system.

NOTE

If you are installing an add-on disk drive in one peripheral cabinet of a daisy-chain, power down the peripheral cabinet and install the disk drive before you power down the mainbay to install cables to the controller. This sequence reduces system down time and avoids powering down the mainbay more than once to complete the drive to controller connections.

This section provides the following disk drive installation procedures:

- Installing a Premounted Drive provides a procedure for installing a pre-mounted disk drive as part of an initial system install or upgrade.

- Installing an Add-On Drive provides a precedure for installing a drive as an expansion of an existing system.

A procedure for installing the disk drive controller (IDC1) is provided in Installing the IDC1 in this chapter.

2.8.9.1 Installing a Premounted Drive

This section provides a procedure to configure and complete the cabling of a pre-mounted disk drive. The procedure consists of two major steps:

- Verifying/Converting Operating Voltage

- Verifying/Completing Premounted Drive Cabling

2.8.9.1.1 Verifying/Converting Drive Voltage

Roll the peripheral cabinet containing the drive(s) into position next to the mainbay, then verify the correct operating voltage as follows:

1. Label all the cables at the drive and at the bulkhead.

WARNING

Be sure to extend the cabinet's two anti-tip legs before continuing with this procedure.

2. Lift the small latch at the lower left front corner of the drive, and pull the drive toward you until it is fully extended. You may need a screwdriver to reach the release latch of the drive.

3. Locate Switch S2 on the power supply (see Figure 2-42). It may be covered by a sticker or a protective plate. Verify the switch setting by peeling back/removing the label/protective plate and looking at the switch. Correct voltages are as follows: Domestic 120 V, International 240 V.

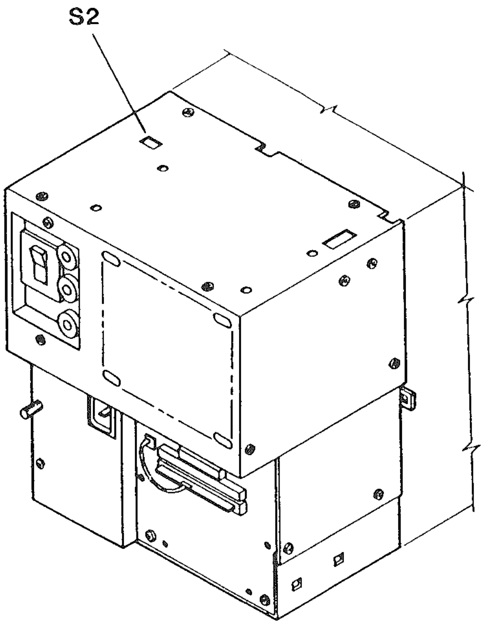


FIGURE 2-42: 496MB DISK DRIVE POWER VERIFICATION

2.8.9.1.2 Verifying and Completing Premounted Drive Cabling

After completing the voltage check-out/conversion, verify cabling as follows:

1. Remove the two screws that secure the disk drive I/O shield to the I/O plate (see Figure 2-43).

2. Verify the connection of the control cable CBL10322-001 from J4 on the drive(s) I/O plate to the cabinet bulkhead (see Figure 2-44).

3. Verify the connection of the data cable CBL10321-002 from J2 on the drive(s) I/O plate to the cabinet bulkhead (see Figure 2-44).

4. In multi-drive configurations, verify the connection of the daisy chain cable (CBL10320-001) from J3 on drive 0 to J4 on drive 1.

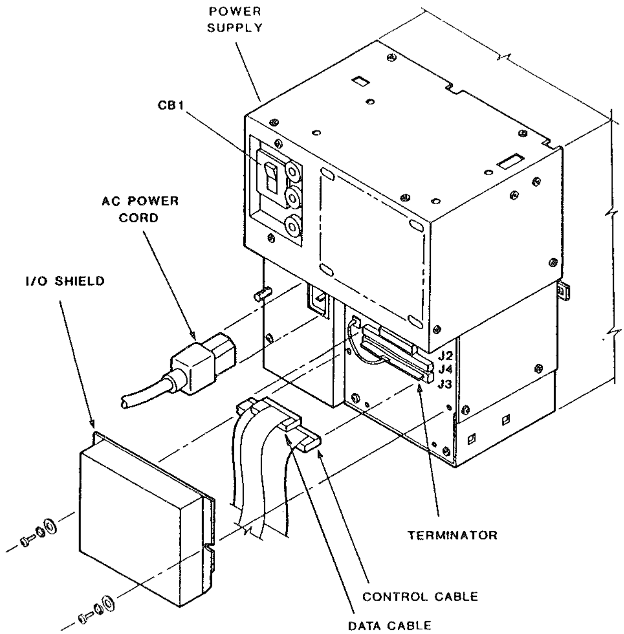


FIGURE 2-43: I/O SHIELD REMOVAL

5. Verify that the LAST drive in each chain has a terminator installed in connector J3 of the I/O plate (see Figure 2-43).

6. Replace the disk drive's I/O shield.

7. Verify that drive power cable CBL10662-001 (120 Vac) or CBL10662-002 (240 Vac) is connected to the port labelled AC In (J1) at the drive and to the peripheral bay PDU.

8. Connect control cable, CBL6382, to connector J1 on the appropriate peripheral cabinet connector panel. Connect the opposite end to connector J1 on the mainbay bulkhead.

CAUTION

> Verify that the mainbay and peripheral cabinet are powered down before completing the bulkhead-to-bulkhead connection.

9. Connect data cable, CBL10378, to connector J2 on the appropriate peripheral cabinet connector panel. Connect the opposite end to connector J2 on the mainbay bulkhead.

Refer to 496MB Fixed Module Disk Subsystem Service Procedures Manual (SPM470) for disk drive verification and troubleshooting procedures.

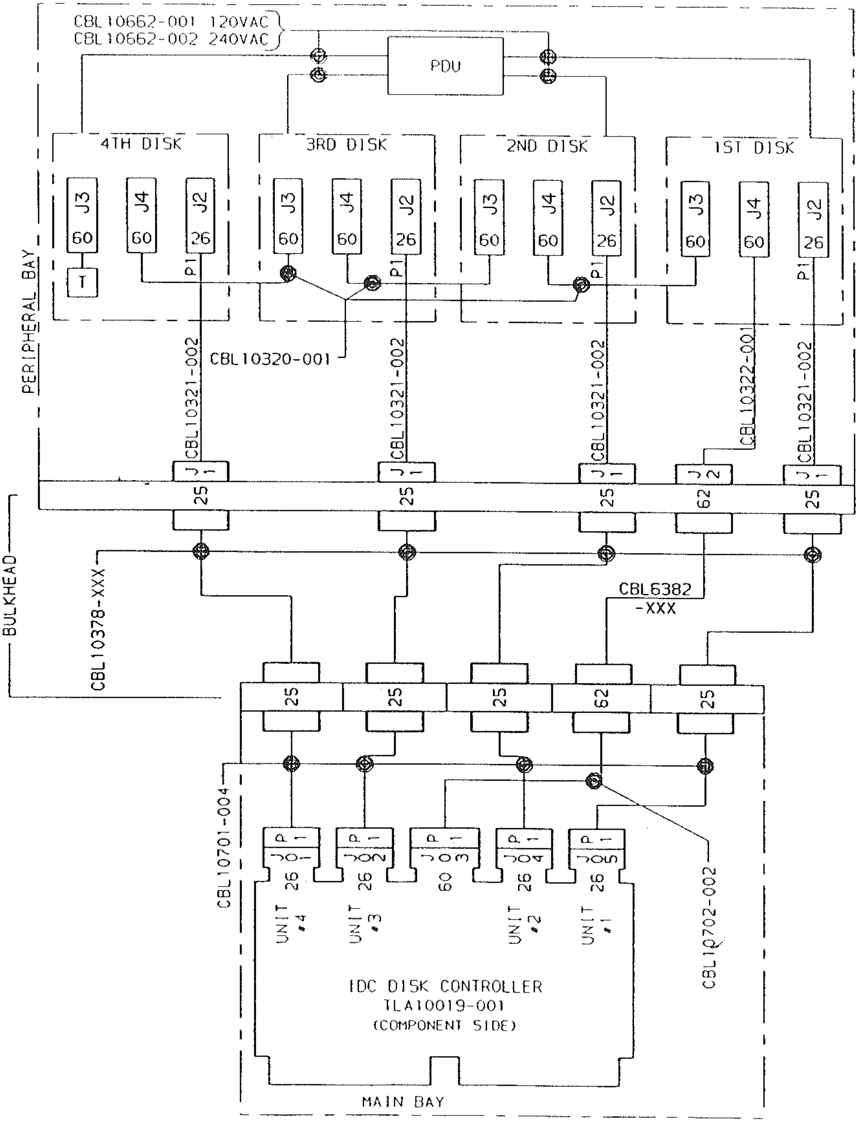


FIGURE 2-44: 496MB DISK DRIVE CABLING

2.8.9.2 Installing An Add-On Drive

This section provides a procedure for installing a 496 Mb drive into a 7730H 30-inch peripheral cabinet. The procedure consists of the following major steps:

- Allocating Cabinet Space
- Converting the Operating Voltage
- Organizing the Mounting Hardware
- Assembling the T-Bar Mounting Hardware
- Mounting the Hardware in the Cabinet
- Installing the Rails
- Installing the Filler Panel, Inner Rails, and Disk Drive
- Cabling the Disk Drive and Cabinets

WARNING

> Before beginning the add-on installation, be sure to power down the peripheral cabinet and unplug the ac power cable from the power source and the PDU.

2.8.9.2.1 Allocating Cabinet Space

The peripheral cabinet has two zones allotted for peripheral device installation. Each zone can accommodate two disk drives, for a total of four in each cabinet. Each zone has a corresponding zone on the bulkhead for cable connection to the CPU.

Refer to Peripheral Cabinet Configuration Guidelines in this chapter for disk drive location instructions.

2.8.9.2.2 Converting Drive Voltage

Set the disk drive's operating voltage as follows:

1. Locate Switch S2 on the power supply. It may be covered by a sticker or a protective plate.
2. Peel back the sticker or remove the protective plate.
3. Set the switch to 120 V for domestic operation or to 240 V for international operation.

2.8.9.2.3 Organizing the Mounting Hardware

Cabinet mounting hardware is a combination of CDC and Prime parts. The carton containing the disk drive has four rolls and one box. Table 2-23 identifies mounting hardware required for installation. Roll B contains extra parts. Disregard them. The box containing the filler panel contains CDC instructions. Disregard them as well.

Before you begin the installation locate the hardware listed on the parts tables. Separate those parts not used in the installation. If this is your first installation attempt, it helps to locate an existing 496MB installation in any cabinet. Make a mental note of the finished installation to ease the difficulty of the procedures.

TABLE 2-23: 496MB DISK DRIVE MOUNTING HARDWARE

ROLL A: ONE CLEAR PLASTIC BAG	
DESCRIPTION	QUANTITY
Metallic Stand-off	4
Cable Retainer Bar	1
Screws, panhead philips .625L	20
Nut Bar	4
Cable Tie	3
Nut, clip w/grnd	8
Clamp	2
Label,Caution	1
Screw, .31L	4
Support Bracket (LH)	2
Support Bracket (RH)	2
1/2" Flathead Phillips Screw	8
3/4" Panhead screw	1
ROLL B: SEVERAL SMALL PLASTIC BAGS	
Slide Stop Plate	2
1/4" Flathead Phillips screws	4
Hex Nut	1
Dished Lock Washer	3
Panhead screw, .5L, with star	4
Panhead screw, .5L,	2
Star washer	1
Dished washer	2
ROLL C	
Front slotted T-Bar	1
Rear T-Bar	1
ROLL D	
Trim Panel	2
BOX E	
Mounting hardware	1
Filler panel	1

2.8.9.2.4 Assembling the T-Bar Mounting Hardware

To assemble the T-bar and mounting hardware, refer to Figure 2-45 and follow these steps:

1. Verify that power is removed from the peripheral cabinet.

2. Locate the parts shown in Figure 2-45.

3. Locate the mounting brackets and T-bar supports.

4. Attach two of the mounting brackets to the ends of each T-bar using the 1/2" flathead phillips screws. Use the following guidelines when assembling the mounting brackets and T-bars.

   A) When facing the front of the cabinet, the front left-hand mounting bracket is part number MEC10550-001 and the right-hand mounting bracket is MEC10550-002. The front T-bar has two cut-outs on the top surface. Position the cut-outs towards the left side of the cabinet.

   B) The rear left-hand mounting bracket is MEC10550-002.

   C) The rear right-hand mounting bracket is MEC10550-001.

5. Insert the screws into the mounting bracket holes marked F for the front T-bar and into the holes marked S for the rear T-bar.

2.8.9.2.5 Mounting the T-Bar in the Cabinet

To mount the T-bar in the cabinet, refer to Figure 2-46 and follow these steps:

1. Remove the cabinet rear panel.

2. Measure and mark the location on the cabinet mounting rails where the top screw in the nut bar will go. The top screw goes into the second to bottom hole on the nut bar. If you are installing the assembly in Zone 1 measure 8.75 inches from the center of datum 0 and mark the location on the left and right, front and rear rails. Datum 0 is the topmost hole on the mounting rail. Another way to determine the correct location is to count holes from the bottom, up. Table 2-24 provides nut bar location measurements for each zone in the cabinet.

3. Line up the nut bars so that the first screw hole location lines up with the mark you just made. The keypost goes into the retma rail. Attach the nut bars to the mounting rails by inserting one 5/8" screw and lock washer in the top hole of each nut bar.

4. Push the front T-bar assembly into place. The T-bar assembly cannot be pushed straight into the cabinet. It must be inserted at an angle to the mounting rails and then dropped into position.

5. Secure the T-bar assembly to the mounting rails and nut bar using four 5/8" screws with lock washers.

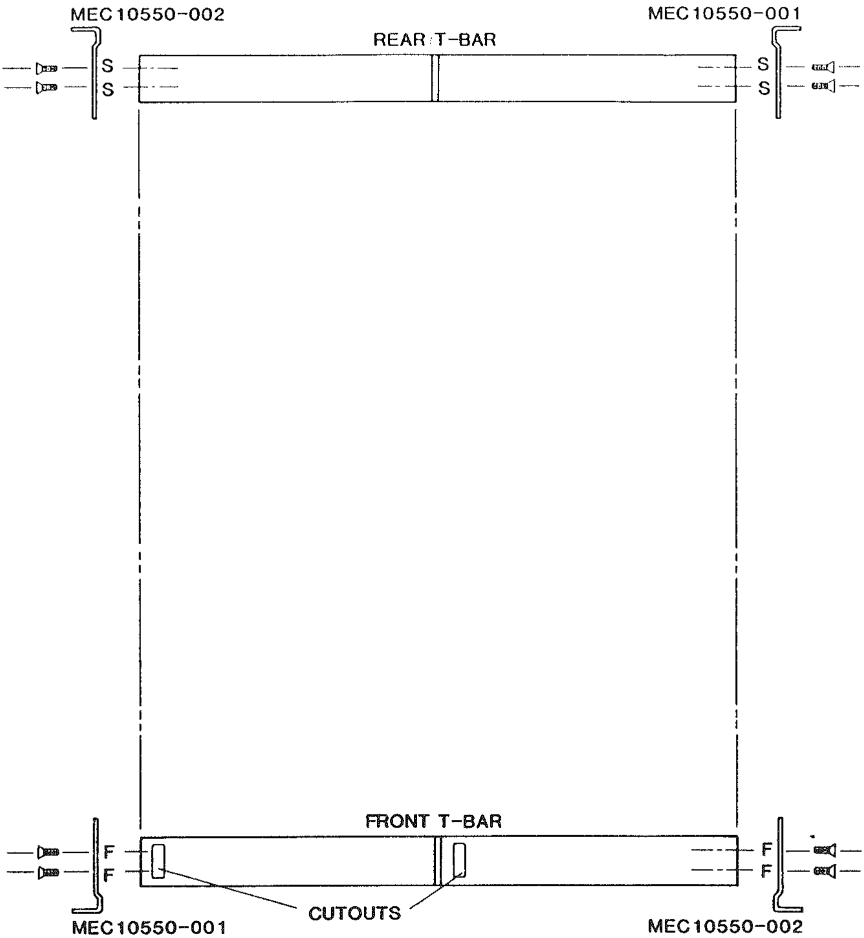


FIGURE 2-45: T-BAR ASSEMBLY

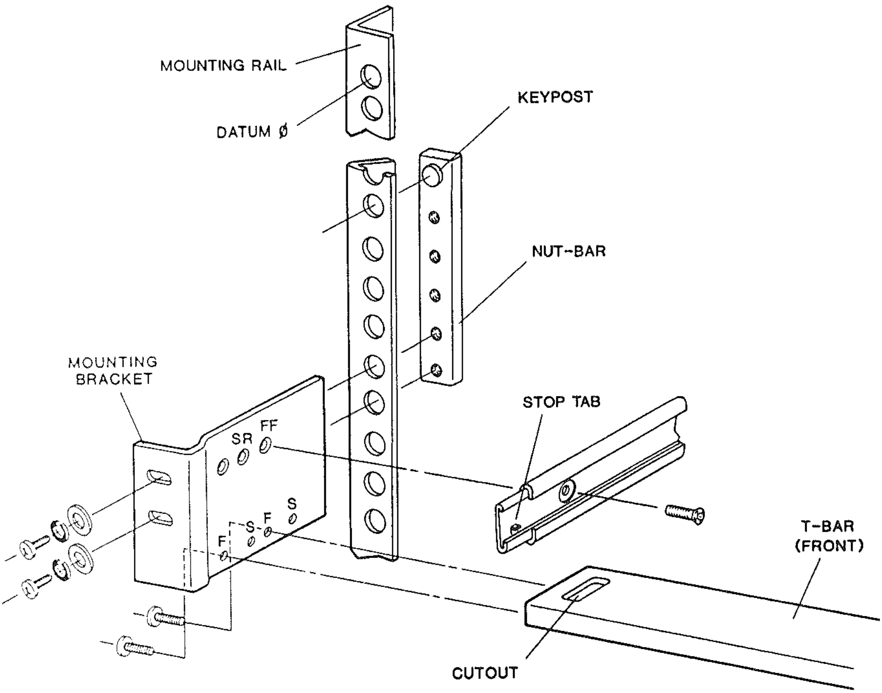


FIGURE 2-46: MOUNTING THE T-BAR

6. Remove the two screws that you installed in step 3.

7. Repeat steps 4 through 6 for the rear T-bar assembly.

TABLE 2-24: CABINET FRONT/REAR RAIL MEASUREMENTS

ZONE 1, TOP	ZONE 2, BOTTOM
8.75 in. (222.3 mm)	19.25 in. (489.0 mm)
FRONT RAILS: Holes are counted from bottom up	
ZONE 1, KEYPOST 29 HOLES	ZONE 2, KEYPOST 11 HOLES
REAR RAILS: holes are counted from bottom up	
ZONE 1, KEYPOST 31 HOLES	ZONE 2, KEYPOST 13 HOLES

2.8.9.2.6 Installing the Intermediate and Outer Rails

To install the intermediate and outer rails, refer to Figure 2-47 and follow these steps:

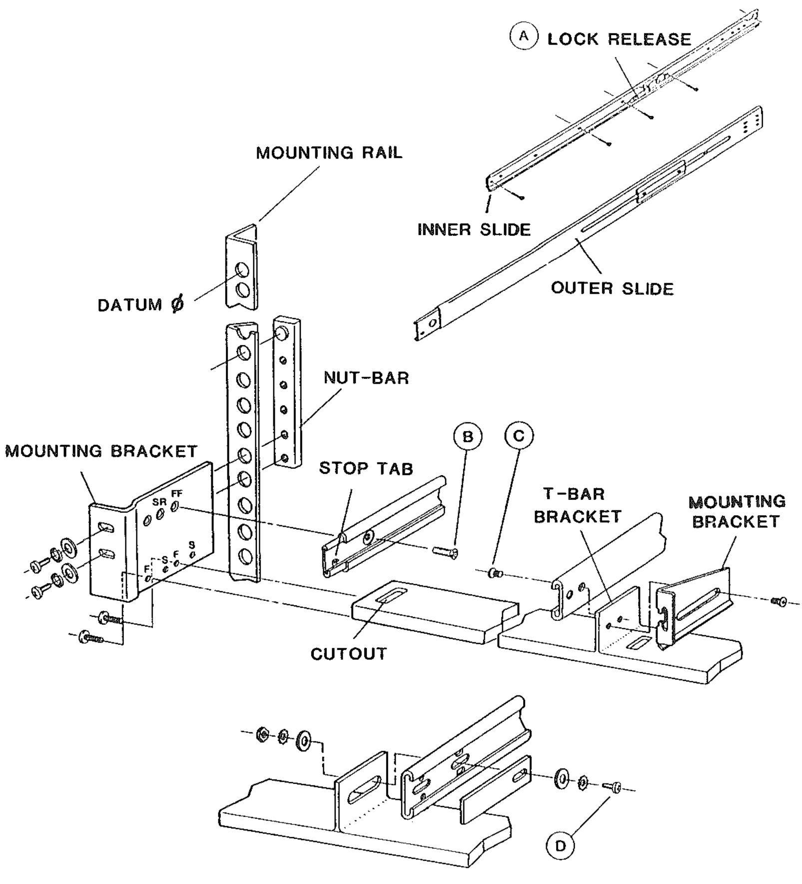


FIGURE 2-47: INSTALLING THE RAILS

1. Remove the inner slide rails from the intermediate and outer assembly by pressing the release arm on the inner slide, and set them aside for attachment to the drive (A). The outside of the rails include LH for left and RH for right-hand rail.

2. Secure the front of the LH rail to the cabinet using one of the four 1/4" flathead phillips screws. Orient the rail so that the stop tab is at the bottom of the rail towards the front. Insert the screw through the second hole in the rail and into the FF hole on the mounting bracket (B). You may have to loosen the mounting bracket screws before installing the outer slides.

3. Secure the front of the RH rail to the cabinet using one of the four 1/4" flathead phillips screws. Orient the rail so that the stop tab is at the bottom of the rail towards the front. Insert the screw through the second hole in the rail and into the second hole on the T-bar mounting bracket (C).

4. Secure the rear of LH rail using a 1/2" panhead phillips screw, with star washer. Insert the screw through the slide and into the mounting bracket hole labeled SR.

5. Hold the two stop plates flush with the center rail ends, one on either side of the rear T-bar mounting bracket. Move the center slide forward to expose an opening to install the screw washer nut assembly (D). Secure the stop plates and center rail to the T-bar mounting bracket using a 3/4" panhead phillips screw, washers, and nut. You will find the two flat washers in a plastic kit that comes in the same box as drive.

2.8.9.2.7 Installing the Filler Panel, Inner Rails, and Disk Drive

To install the filler panel, the inner rails, and install the drive in the cabinet, refer to Figure 2-48 and follow these steps:

1. From the filler panel kit, remove the panel and the mounting bracket. Attach the mounting bracket to the T-bar bracket with a 1/4" panhead phillips screw. Hand tighten only.

2. Install the standoffs, each with two lockwashers, to the bottom most position in each set of holes on the two trim pieces. Hand-tighten only at this time. The insert closest to the end is the top.

3. Mount one of the two trim pieces onto the filler panel. Leave a 1/4" gap between the trim piece and filler panel when mounting.

4. Place the filler panel with the attached trim piece against the mounting rail. Attach the panel to the mounting rails using two 1/2" panhead phillips screws and washers. Secure the filler panel mounting bracket to the T-bar mounting bracket using a 1/4" flathead phillips screw.

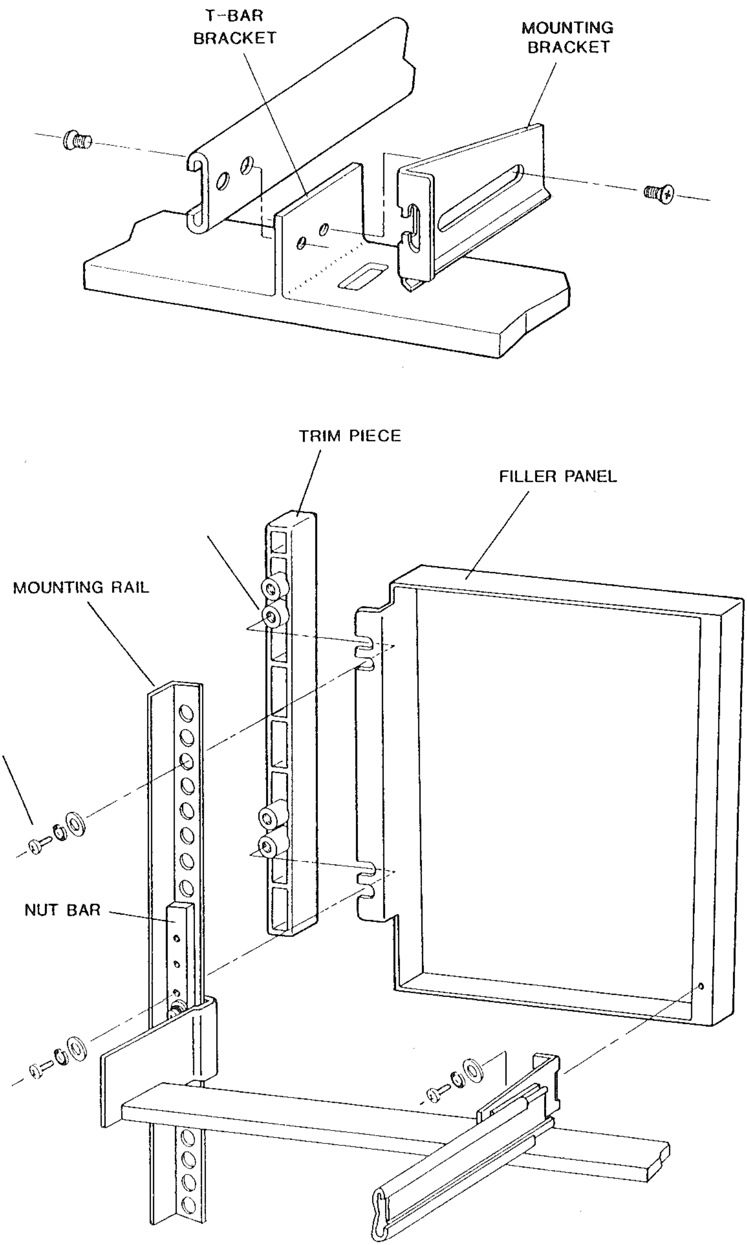
5. Install the remaining trim piece on the opposite front mounting rail using two 1/2" panhead phillips screws and washers.

6. Align the filler panel and trim pieces and tighten the attaching hardware.

7. Remove the two shipping brackets from either side of the disk drive. Discard the brackets and retain the six screws for use in installing the inner slide assembly.

8. Identify the right and left inner slides. They are labeled RH and LH as described previously.

9. Attach the inner slides to the drive using twelve 1/2" self-tapping screws (six for each side), by inserting the screws through the slide holes into the square nuts on the drive. Six screws are found in a plastic bag that comes with the drive.



VIEWED FROM INSIDE THE CABINET

FIGURE 2-48: INSTALLING FILLER PANEL

10. At the cabinet, push each intermediate slide into a fully retracted position inside the outer slide.

11. Lift the drive into position in front of the cabinet rails. Guide the inner slides of the drive into the intermediate slides.

CAUTION

The disk drive is heavy. Lifting the drive into position requires two persons.

12. Push the drive toward the cabinet until the lock release clicks, signaling that the lock is engaged. Then push the drive all the way into the cabinet.

2.8.9.2.8 Cabling the Disk Drive and Cabinets

To cable the disk drive(s) to the peripheral cabinet bulkhead, refer to Figure 2-44 and follow these steps:

NOTE

If the disk drive being installed is equipped with a dual channel I/O board (FVJX) make all connections to the Channel 1 connectors on the I/O plate (1J2 - 1J4).

1. Install CBL10321-002 from the bulkhead to J4 of the first device.

NOTE

When routing the cable allow only enough cable to reach the disk with the unit fully extended from the cabinet. Excess cable promotes pinching with the drive retracted. Fold excess cable and secure it to the side of the cabinet with the cable retaining clips.

2. If there are two drives in the cabinet, install CBL10320-001 from J3 of the first device to J4 of the second device.

3. Terminate J3 of the last drive in the chain.

4. Install CBL10321-002 from the bulkhead to J2 of each drive.

5. Connect ac power cord CBL10662-001 (-002) to each drive. Feed the free end into the narrow space between the cabinet chassis and the left or right side panel.

6. From the front of the cabinet, remove the lower cover panel from its ball stud fasteners, then remove the two screws that secure the cover plate to the cabinet chassis to access the peripheral device power cables. Reach into the opening and locate the free end of power cable, and connect the cable to the peripheral cabinet PDU.

7. Replace the I/O shields. Secure them in place with the screws removed earlier.

8. If the disk drive is to be connected into a dual port configuration, repeat steps 1 through 4 to cable the drive to System B. System B cable connections should be made to the Channel 2 connectors on the I/O plate, labeled 2J2 - 2J4.

9. Replace the peripheral cabinet rear panel.

10. Connect bulkhead-to-bulkhead control cable CBL6382 to connector J1 on the appropriate peripheral cabinet connector panel. Do not connect the opposite end of the cable at this time.

11. Connect bulkhead-to-bulkhead data cable CBL10378 to connector J2 on the appropriate peripheral cabinet connector panel. Do not connect the opposite end of the cable at this time.

12. Complete the IDC1 controller installation procedure described in Installing the Intelligent Disk Controller in this chapter, then return to this procedure and continue with step 13.

13. Connect the free end of bulkhead-to-bulkhead control cable CBL6382 to connector J1 on the appropriate mainbay cabinet connector panel.

14. Connect the free end of bulkhead-to-bulkhead data cable CBL10378 to connector J2 on the appropriate mainbay cabinet connector panel.

15. Refer to <u>496 Megabyte Fixed Module Disk Subsystem Service Procedures Manual</u> (SPM470-01) for disk drive verification and troubleshooting information.

2.8.10 INSTALLING THE MODEL 4835 (770 MB) DISK DRIVE

Model 4835 disk drives are generally shipped preconfigured and partially cabled in the model 7730H 30-inch peripheral cabinet, or as an add-on drive in a separate shipping carton. This section provides procedures to verify configuration and complete the cabling of a pre-installed drive, and to configure, install and cable a Model 4835 disk drive as an expansion of an existing system.

NOTE

> If you are installing an add-on disk drive in one peripheral cabinet of a daisy-chain, power down the peripheral cabinet and install the disk drive before you power down the mainbay to install cables to the controller. This sequence reduces system down time and avoids powering down the mainbay more than once to complete the drive to controller connections.

This section provides the following disk drive installation procedures:

- Installing a Premounted Drive provides a procedure for installing a pre-mounted disk drive as part of an initial system install or upgrade.
- Installing an Add-On Drive provides a precedure for installing a drive as an expansion of an existing system.

A procedure for installing the disk drive controller (IDC1) is provided in Installing the IDC1 in this chapter.

2.8.10.1 Installing a Premounted Drive

This section provides a procedure to configure and complete the cabling of a pre-mounted disk drive. The procedure consists of two major steps:

- Verifying/Converting Operating Voltage
- Verifying/Completing Premounted Drive Cabling

2.8.10.1.1 Verifying/Converting Drive Voltage

Roll the peripheral cabinet containing the drive(s) into position next to the mainbay, then verify the correct operating voltage as follows:

1. Remove the peripheral bay rear panel.

2. Locate the voltage conversion switch cover plate (see Figure 2-49). With the voltage plate on, the voltage that is displayed is the current operating voltage.

3. Correct operating voltages are as follows:

Domestic	100-120 Vac
International	200-220Vac

4. If the switch is set incorrectly, remove the cover plate by removing the two small phillips screws and press the switch to the desired voltage. Replace the cover plate.

2.8.10.1.2 Verifying and Completing Premounted Drive Cabling

After completing the voltage check-out/conversion, verify and complete disk drive cabling as follows (refer to the cabling diagram shown in Figure 2-50):

1. Verify the connection of the control cable CBL10322-003 from the P3 Channel I connector on the front of the distribution panel to J1 on the inside of the peripheral cabinet bulkhead. This step applies to the first drive in the peripheral bay.

2. If the drive is daisy-chained, verify the connection of daisy-chain cable CBL10320-002 from P4 of the drive's distribution panel to P3 of the distribution panel of the previous drive.

3. Verify the connection of the blue 60-pin ribbon control cable (NEC158-062000-200) from the P3 Channel I connector on the rear of the distribution panel to the P3 Channel I connector on the rear of the disk drive.

4. Verify connection of of data cable CBL10695-001 from the P2 Channel I connector on the drive to J2 on the inside of the peripheral bay bulkhead.

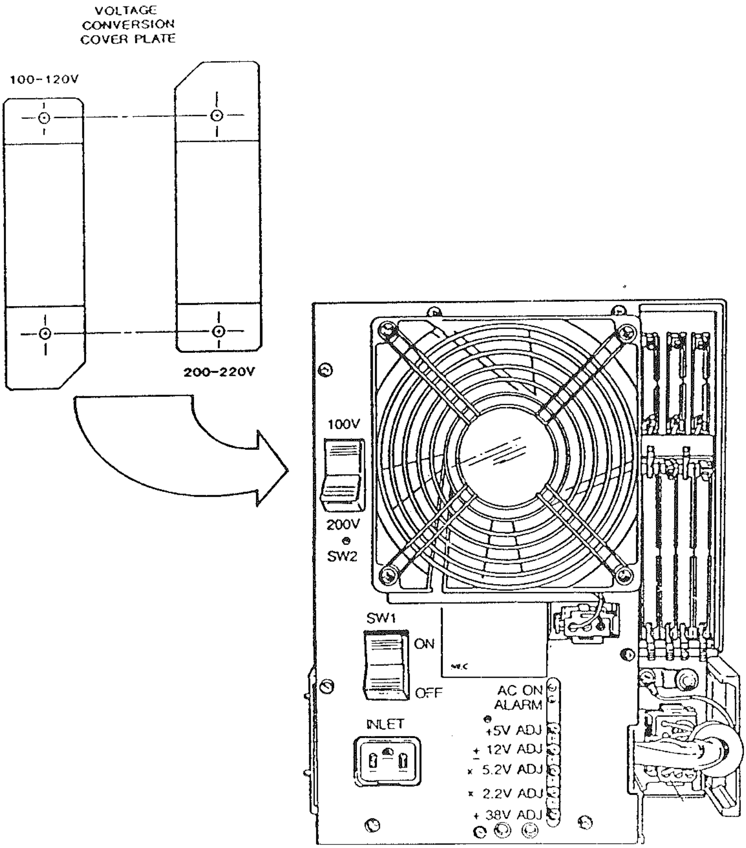


FIGURE 2-49: 770MB DISK DRIVE VOLTAGE VERIFICATION

5. Verify installation of ground wire (NEC158-062000-202) from the grounding lug at the rear of the distribution panel to the Channel I tab on the disk drive.

6. Verify that the LAST drive in each chain has a terminator installed in the P4 Channel 1 connector of its distribution panel.

7. Verify that drive power cable CBL10662-001 (120 Vac) or CBL10662-002 (240 Vac) is connected to the ac cord receptacle at the rear of the drive and to the peripheral bay PDU.

8. Connect control cable, CBL6382, to connector J1 on the appropriate peripheral cabinet connector panel. Connect the opposite end to connector J1 on the mainbay bulkhead.

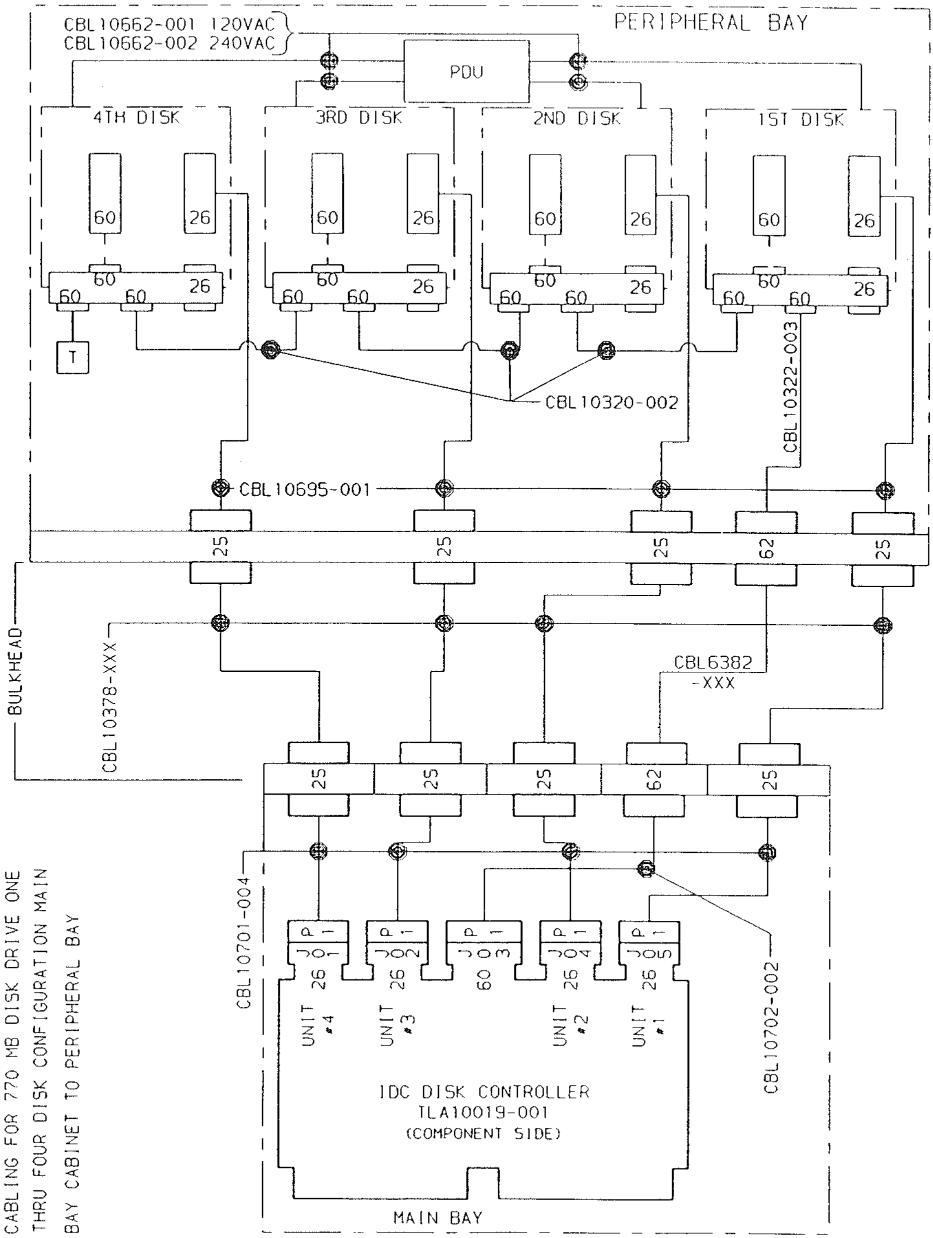


FIGURE 2-50: 770MB DISK DRIVE CABLING

9. Connect data cable, CBL10378, to connector J2 on the appropriate peripheral cabinet connector panel. Connect the opposite end to connector J2 on the mainbay bulkhead.

NOTE

Verify that the mainbay and peripheral cabinet are powered down before completing the bulkhead-to-bulkhead connection.

Refer to <u>770 Megabyte Fixed Storage System Service Procedures Manual</u> (SPM390) for disk drive verification and troubleshooting procedures.

2.8.10.2 Installing An Add-On Drive

This section provides a procedure for installing a 770 Mb drive into a 7730H 30-inch peripheral cabinet. The procedure consists of the following major steps:

- Allocating Cabinet Space
- Verifying/Converting the Operating Voltage
- Organizing the Mounting Hardware
- Assembling the Tray
- Securing the Tray to the Cabinet
- Installing the Trim Panel
- Installing the Filler Panel
- Installing and Cabling the Drive

WARNING

Before beginning the add-on installation, be sure to power down the peripheral cabinet and unplug the ac power cable from the power source and the PDU.

2.8.10.2.1 Allocating Cabinet Space

The peripheral cabinet has two zones allotted for peripheral device installation. Each zone can accommodate two disk drives, for a total of four in each cabinet. Each zone has a corresponding zone on the bulkhead for cable connection to the CPU.

Refer to Peripheral Cabinet Configuration Guidelines in this chapter for disk drive location instructions before beginning the installation procedure.

2.8.10.2.2 Verifying/Converting Drive Voltage

To verify the disk drive's operating voltage, follow these steps:

1. Locate the voltage conversion switch cover plate (see Figure 2-49). With the voltage plate on, the voltage that is displayed is the current operating voltage.

2. Correct operating voltages are as follows:

Domestic	100-120 Vac
International	200-220Vac

3. If the switch is set incorrectly, remove the cover plate by removing the two small phillips screws and press the switch to the desired voltage. Replace the cover plate.

2.8.10.2.3 Organizing the Mounting Hardware

Installing the mounting hardware and the drive takes two people. The weight of the tray is 30 pounds and it is to cumbersome to hold in place while the rear mounting brackets are installed.

CAUTION

> Before beginning the add-on installation, be sure to power down the peripheral cabinet.

The add-on installation should take approximately one hour.

Table 2-25 lists the parts necessary for an add-on installation. Locate all parts before beginning the installation.

TABLE 2-25: 770MB DISK DRIVE MOUNTING HARDWARE PARTS

Tray Hardware	
DESCRIPTION	QUANTITY
Tray	1
Rear mounting bracket L	1
Rear mounting bracket R	1
Nut & star washer	8
Philips flat head	34
Philips pan head 8-32 & star washer	8
Nut clips (not used)	
Flat washers	8
Flat washers	8
Stop plate with large screw	2
Stud plates	2

TABLE 2-25: 770MB DISK DRIVE MOUNTING HARDWARE PARTS (CONT.)

DESCRIPTION	QUANTITY
Trim Kit	
Nut clips	4
Screws 10-32	4
Washers	4
Trim Strip	2
Trim panel	2
Filler Panel	
Filler panel	1
Screws pan head with star washer	4
Washers	4
Distribution Panel	
PCB	1
Bracket	1
Control cables	2
Ground Strap	1
Screws 8-32, 5/16	4
Washers	4

2.8.10.2.4 Assembling the Tray

To assemble the tray, refer to Figure 2-51 and follow these steps:

1. Unpack the disk drive and mounting hardware.

2. Locate all the mounting hardware.

3. Remove the rails from the drive by extending the rails, then pressing the lock button on both sides.

4. Position the tray so that the rear is away from you.

5. Extend the rails to expose the eight flat head screws securing the panels on each rail. Use a large flat head screwdriver to remove these screws. Discard the panel and the screws.

6. Position the rails in the tray so that the lock button sticker is on the outside of the rail towards you, and the locking tab on the left rail is on the bottom.

7. Use 16 metric flat head screws to mount the rails to the tray. There are eight screws per rail. The screws are installed from the inside of the tray.

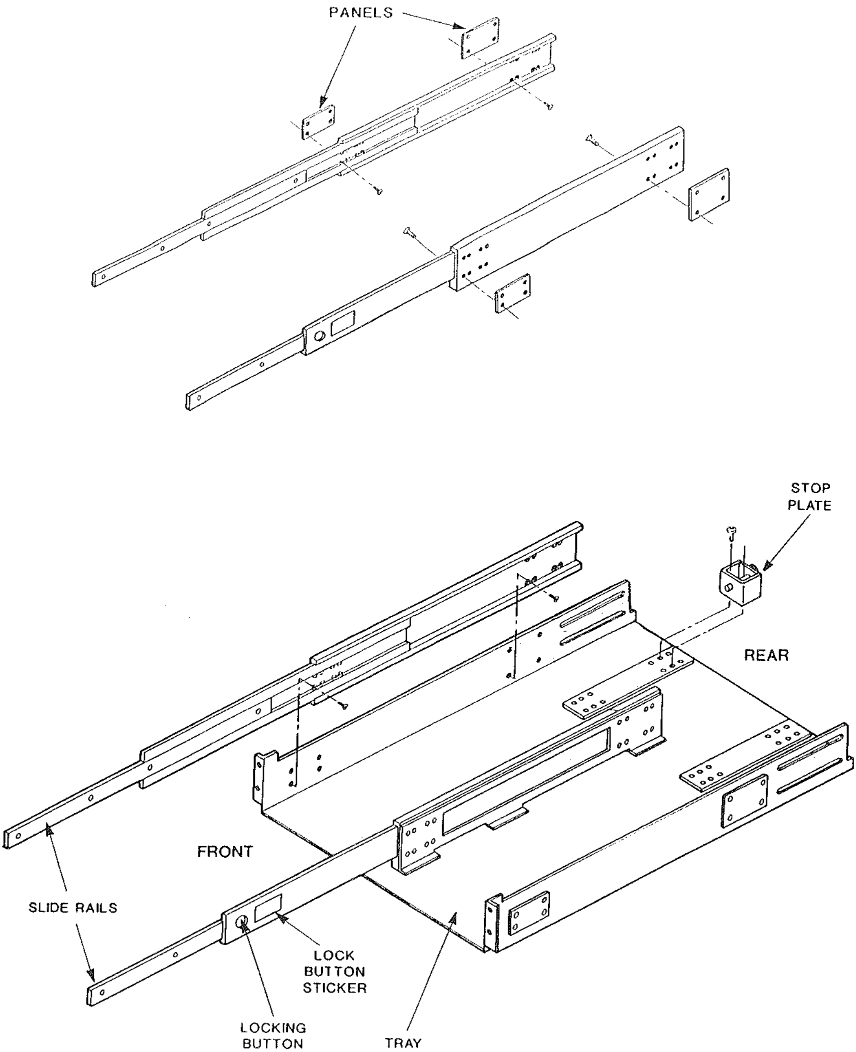


FIGURE 2-51: ASSEMBLING THE TRAY

NOTE

Use a blunt head screwdriver to avoid stripping the screws.

8. Loosely install the stop plate in the rear of the tray using four panhead screws for each stopper. The opening end of the stop plate should face upwards.

2.8.10.2.5 Securing the Tray to the Cabinet

To secure the tray to the peripheral cabinet, refer to Figure 2-52 and follow these steps:

1. Identify the location of the four nut bars that secure the tray to the four front and rear cabinet mounting rails. Using Table 2-26, measure down from the middle of the top mounting rail hole (Datum 0). Mark the mounting rail. The mark specifies the location of the keypost of the nut bar.

TABLE 2-26: 7730H CABINET NUT BAR MEASUREMENTS

ZONE 1	ZONE 2
7.00 in. (177.8mm)	17.50 in. (444.5mm)

2. Slide the tray in place, then line up the front bracket of the tray with the nut bar. Install two screws in both front brackets to secure the tray to the cabinet (A).

CAUTION

The tray is heavy and requires two people to install it into the cabinet.

3. Fasten the rear brackets with holding plates to the cabinet by following these steps:

   A) Using four nuts on each side, install the holding plate and the rear bracket to each side (B).

   B) Position the tray in place. Secure the rear brackets to the mounting rails and nutbar using the large Phillips screws, flat washers and star washers (C).

   C) Tightening all mounting hardware.

4. Secure the distribution panel to the bracket using two screws and washers (D).

5. Secure the distribution panel to the tray using two screws with washers (E).

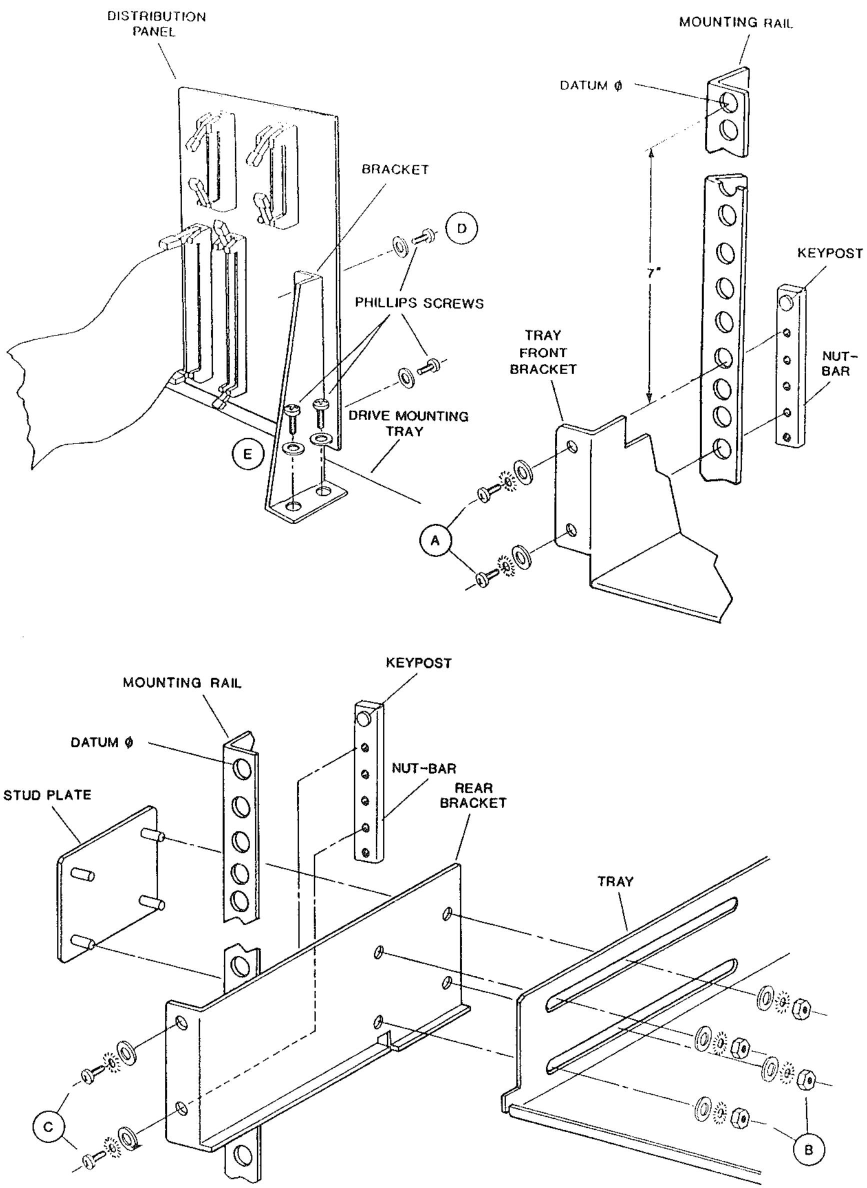


FIGURE 2-52: SECURING THE TRAY TO THE CABINET

2.8.10.2.6 Installing the Trim Panel

To install the trim panels, refer to Figure 2-53 and follow these steps:

1. Identify the location of the nut clips that secure the trim strip to the mounting rails. Refer to Table 2-27. Measure and mark from the center of Datum 0 the nut clip locations for your cabinet. The mark identifies the location of the top screw hole in the trim strip.

TABLE 2-27: 7730H CABINET NUT CLIP MEASUREMENTS

ZONE 1	ZONE 2
1.12 in. (28.6mm)	11.75 in. (298.4mm)

2. Snap on the nut clips you received with the trim panels at the locations marked.

3. Secure the trim strips to the mounting rails using the screw washer combination.

4. Snap the trim panels in place.

2.8.10.2.7 Installing the Filler Panel

To install the dummy filler panel, refer to Figure 2-53 and follow these steps:

1. Align the filler panel with the screw holes in the mounting tray.

2. Secure both sides of the panel to the tray using two screws and washers on each side.

2.8.10.2.8 Installing and Cabling the Drive

To install and cable the drive, refer to Figures 2-50 and 2-54 and follow these steps:

CAUTION

Be sure to extend the two anti-tip legs at the front of the peripheral cabinet before installing the drive onto the tray.

1. Remove the four rubber feet from the drive.

2. Install the control cables (from the distribution Panel Kit) to P3 Channel I and P3 Channel II on the drive (A).

3. Install data cable CBL10695-001 to P2 channel I, II or both on rear of the drive. The stripped shield of the data cable must go through the plate on the power supply (B).

CAUTION

The drive is heavy. The next step requires two persons.

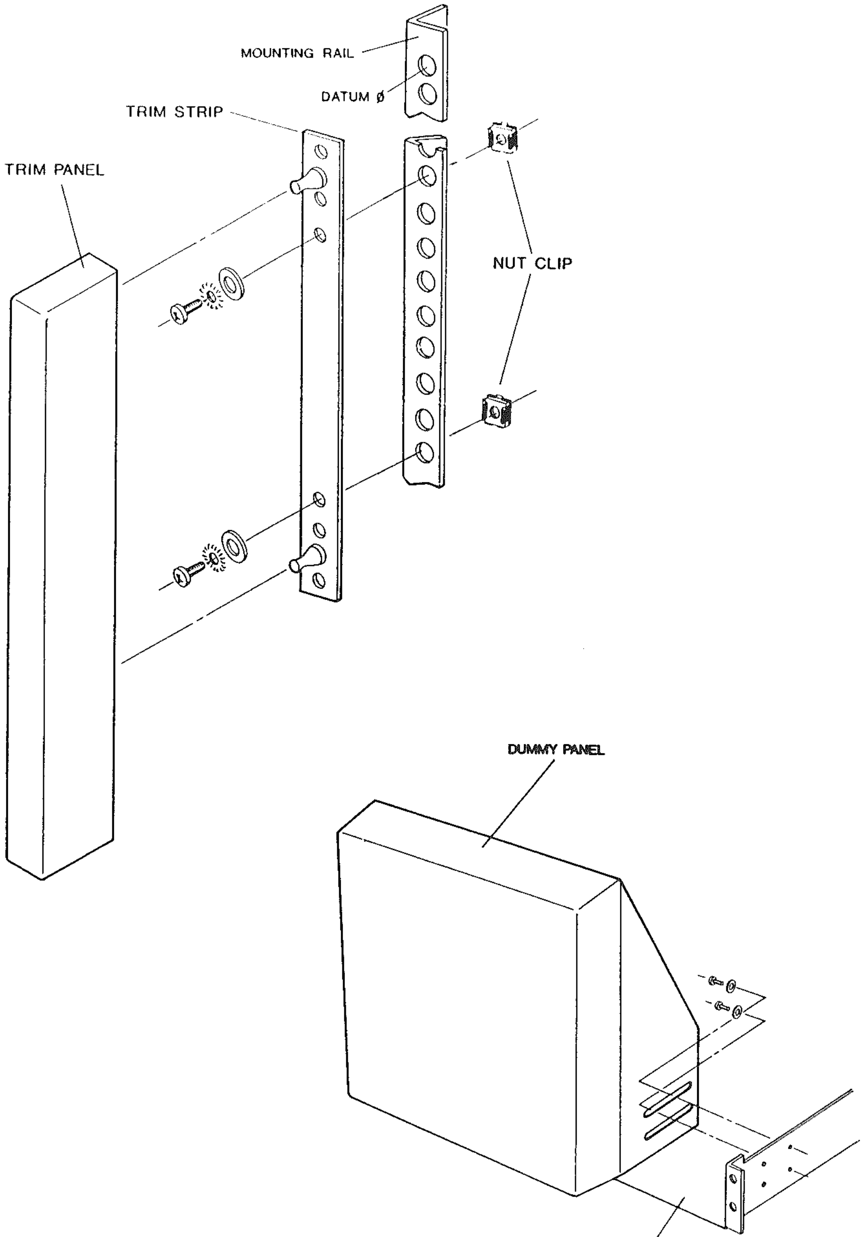


FIGURE 2-53: INSTALLING TRIM AND FILLER PANELS

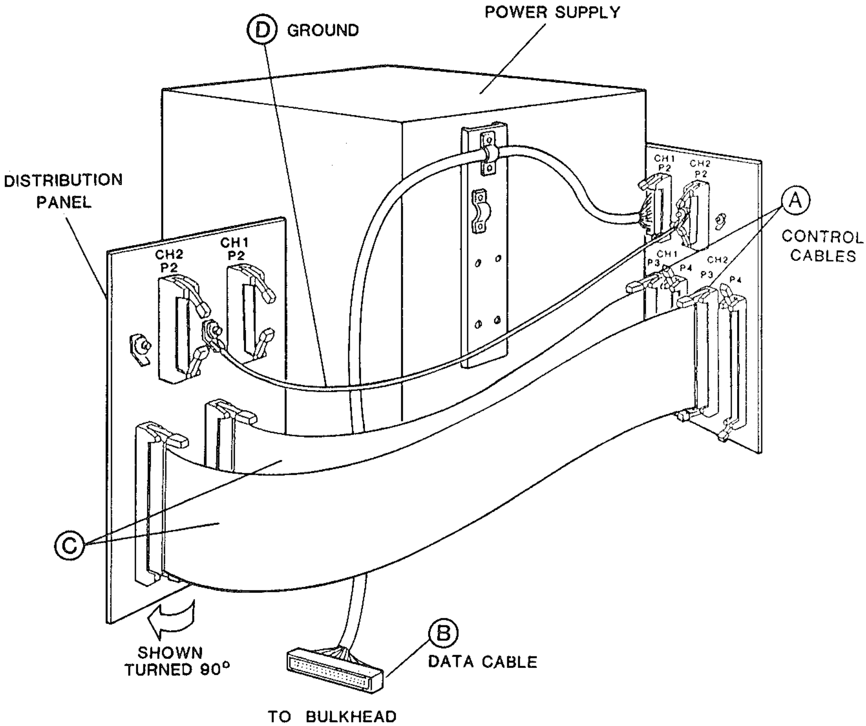


FIGURE 2-54: DISTRIBUTION PANEL CABLING

4. Line up the rear of the drive with the rails in the cabinet. Push it in all the way into the cabinet until the rear of the drive rests against the stop plate. Take care not to damage the control cables or data cable(s).

5. Connect the control cables to the distribution panel (C).

6. Connect the ground strap between the distribution panel and the channel I tab of the disk drive (D).

7. Install the free end of data cable CBL10695-001 to the bulkhead.

8. If you are installing Drive Unit 0, install control cable CBL10322-003 from the bulkhead to P3 of the appropriate channel on the distribution panel. Otherwise, skip this step and proceed to the step that follows.

9. Install daisy chain cable CBL10320-002 from P4 of the last drive's distribution panel to P3 of the distribution panel you just installed.

10. Terminate the last drive in the daisy chain at P4 on the distribution panel associated with it.

11. Connect ac power cord CBL10662-001 (-002) to each drive. Feed the free end into the narrow space between the cabinet chassis and the left or right side panel.

12. From the front of the cabinet, remove the lower cover panel from its ball stud fasteners, then remove the two screws that secure the cover plate to the cabinet chassis to access the peripheral device power cables. Reach into the opening and locate the free end of power cable, and connect the cable to the peripheral cabinet PDU.

13. Replace the peripheral cabinet rear panel.

14. Lift the front panel of the drive and verify that both channel enable switches are up. Verify the top left switch is down and the bottom left switch is down.

15. Set the unit select rotary switch to the desired logical number (D).

16. Connect bulkhead-to-bulkhead control cable CBL6382 to connector J1 on the appropriate peripheral cabinet connector panel. Do not connect the opposite end of the cable at this time.

17. Connect bulkhead-to-bulkhead data cable CBL10378 to connector J2 on the appropriate peripheral cabinet connector panel. Do not connect the opposite end of the cable at this time.

18. Complete the IDC1 controller installation procedure described in Installing the Intelligent Disk Controller in this chapter, then return to this procedure and continue with step 19.

19. Connect the free end of bulkhead-to-bulkhead control cable CBL6382 to connector J1 on the appropriate mainbay cabinet connector panel.

20. Connect the free end of bulkhead-to-bulkhead data cable CBL10378 to connector J2 on the appropriate mainbay cabinet connector panel.

21. Refer to <u>770 Megabyte Fixed Storage System Service Procedures Manual</u> (SPM390) for disk drive verification and troubleshooting information.

2.8.11 INSTALLING THE MODEL 4587 (QUAD DENSITY) TAPE DRIVE

Model 4587 quad density tape drives are generally shipped preconfigured and partially cabled in the model 7730H 30-inch peripheral cabinet. This section provides procedures to verify configuration and complete the cabling of a pre-installed drive.

Due to cable length restrictions, each tape drive requires its own SCSI Tape Controller (MSTC). A procedure for installing an MSTC in the mainbay cabinet is provided in Installing the MSTC in this chapter.

This section provides a procedure to configure and complete the cabling of a pre-mounted tape drive. The procedure consists of two major steps:

- Verifying/Converting Operating Voltage
- Verifying/Completing Premounted Drive Cabling

Complete the procedures that follow before powering up the tape drive.

NOTE

Each tape drive contains a SCSI printed circuit board with configuration switches and SCSI bus terminators. These switches and terminators are pre-set and installed at the factory and must not be changed.

2.8.11.1 Verifying/Converting Drive Voltage

Roll the peripheral cabinet containing the drive(s) into position next to the mainbay, then verify the correct operating voltage as follows:

1. Verify that the peripheral bay is powered-down and that the PDU is disconnected from the power source.

2. Remove the peripheral bay rear panel.

3. Remove the ac power cord from the tape drive power in assembly (see Figure 2-55).

4. Slide the plastic fuse cover to the left (see Figure 2-55).

5. Rotate the "FUSE PULL" lever to the left and remove the fuse (see Figure 2-55). Verify that the correct fuse is installed as follows:

   Three-amp slo-blo for 240 Vac for International operation

   Six-amp slo-blo for 120 Vac for North American operation

6. Inspect the voltage selector card (see Figure 2-55). The operating voltage appears on the card.

7. To change the operating voltage, use long-nose pliers to remove the voltage selector card and replace the card with a card of the proper value.

8. Replace the fuse with the correct value, if necessary. Otherwise, replace the existing fuse.

9. Slide the fuse cover to the right and replace the power cord.

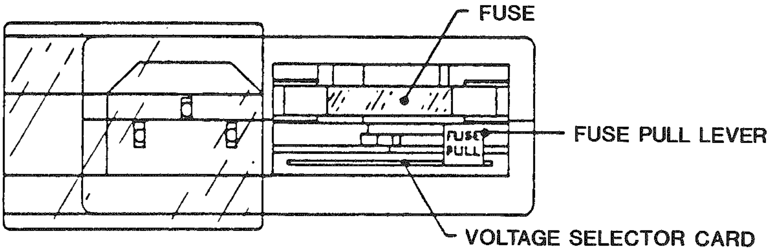


FIGURE 2-55: QUAD-DENSITY TAPE DRIVE VOLTAGE VERIFICATION

2.8.11.2 Verifying and Completing Premounted Tape Drive Cabling

After completing the voltage check-out/conversion, verify and complete disk drive cabling as follows (refer to the cabling diagram shown in Figure 2-56):

1. Verify that drive-to-bulkhead cable CBL10856-001 is connected from the drive to connector J1 on the inside of the peripheral bay bulkhead.

2. Connect bulkhead-to-bulkhead cable CBL6796-001 from J1 on the peripheral cabinet bulkhead to J1 on the mainbay bulkhead.

NOTE

Verify that the mainbay and peripheral cabinet are powered down before completing the bulkhead-to-bulkhead connection.

Refer to Model 4587 Tape Drive Service Procedures Manual (SPM920) for tape drive verification and troubleshooting procedures.

2.8.12 I/O SUBSYSTEM CABLING DIAGRAMS

Figures 2-57 through 2-69 illustrate cabling schemes for 50 Series controllers and subsystems supported by the 4050/4150 system. Figure 2-70 shows the bulkhead panels and part numbers that are available during system bulkheading. Use these figures and the appropriate service manual during controller installation.

2.9 HARDWARE INSTALLATION CHECKOUT

After the system is installed, perform the power-up and installation checkout procedure as follows:

NOTE

If the system fails to verify during initial AutoBoot, be sure to record the failure in your installation report and refer to Chapter 6 of this manual for troubleshooting procedures.

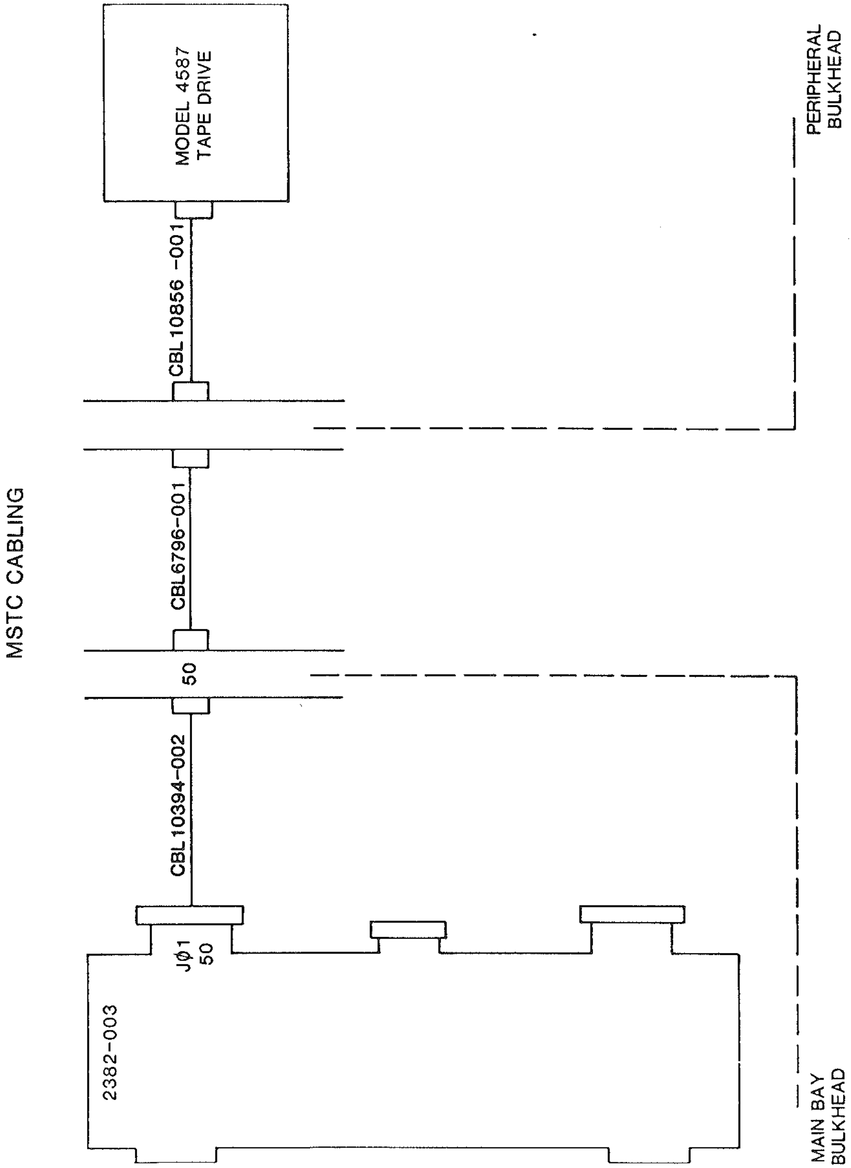


FIGURE 2-56: QUAD-DENSITY TAPE DRIVE CABLING

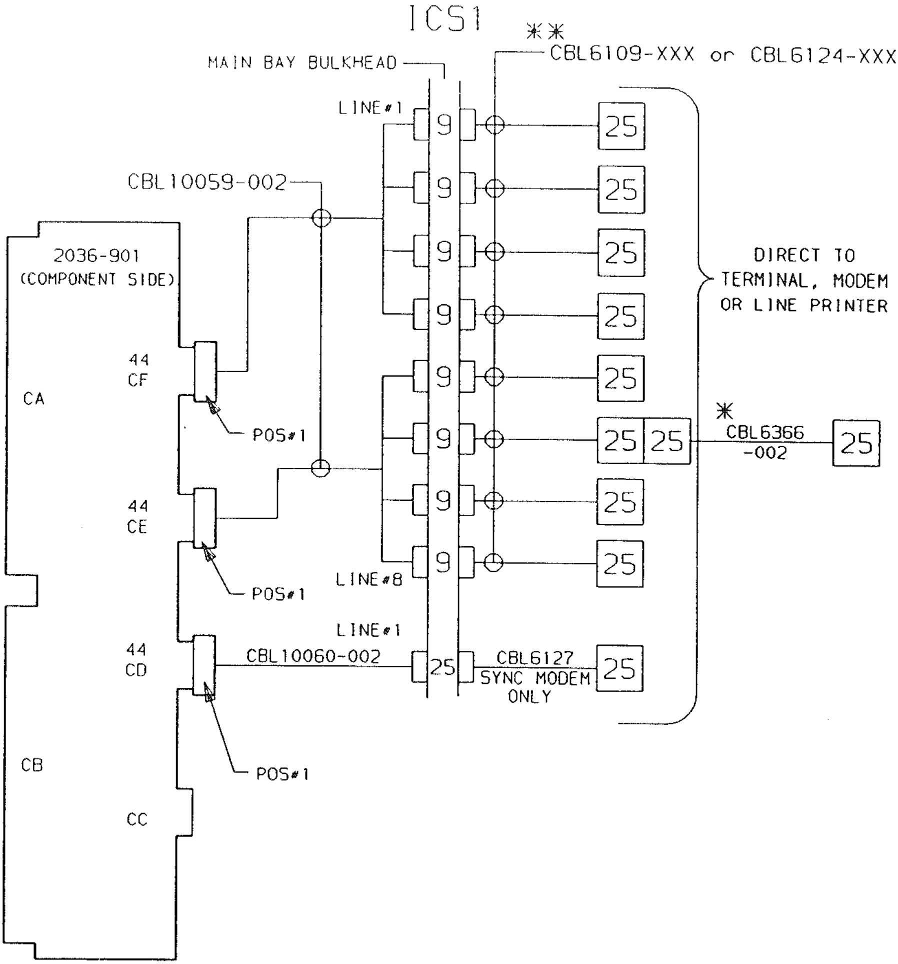


FIGURE 2-57: ICS1 CABLING

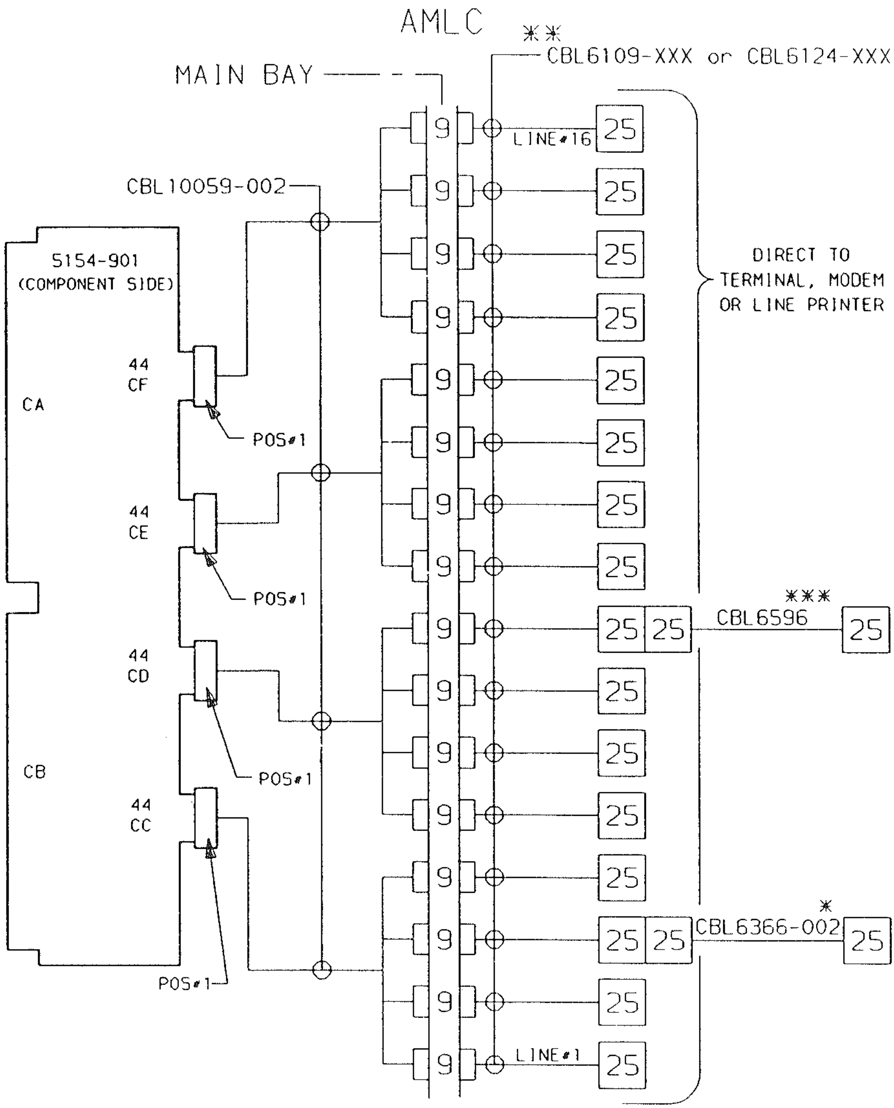


FIGURE 2-58: AMLC CABLING

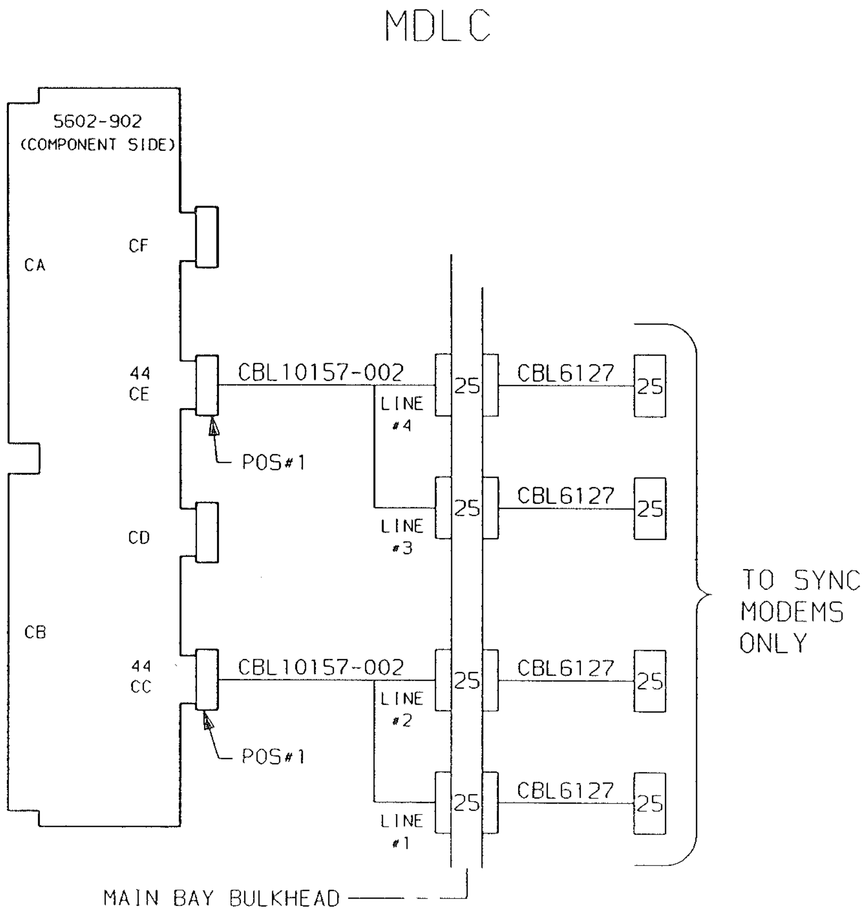


FIGURE 2-59: MDLC CABLING

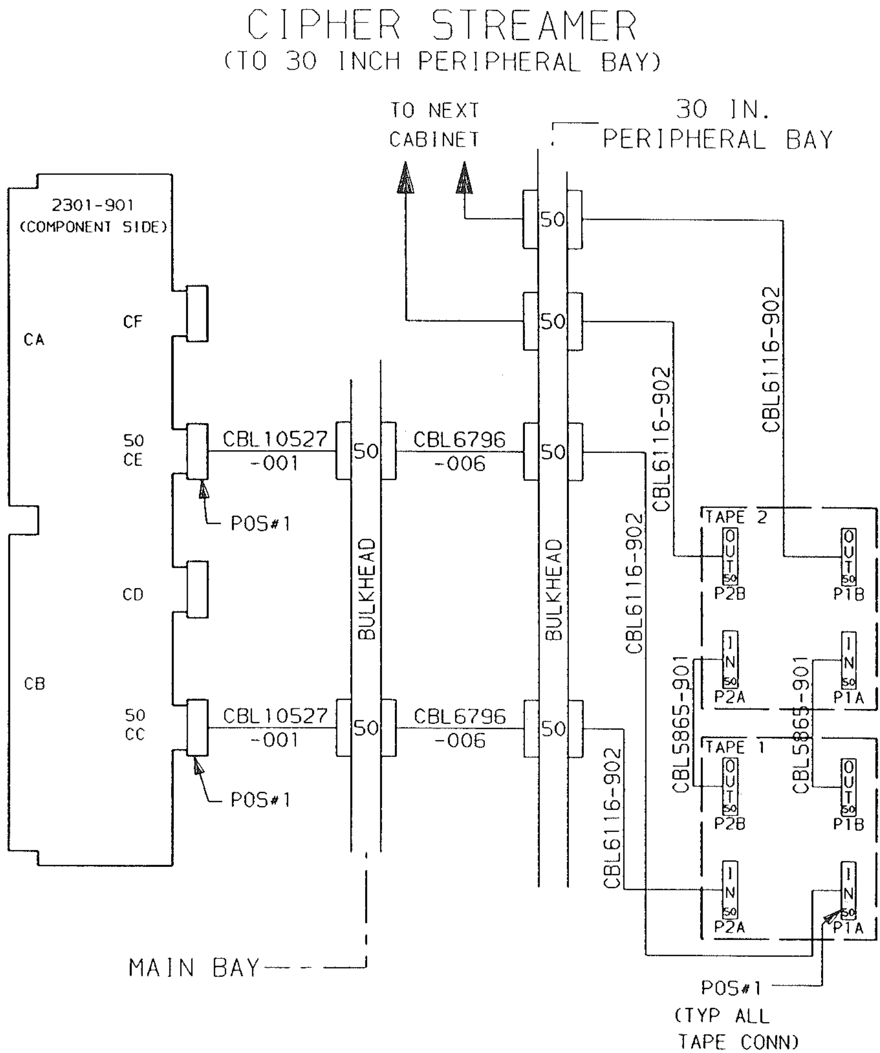


FIGURE 2-60: CIPHER STREAMER CABLING (30-INCH PERIPHERAL BAY)

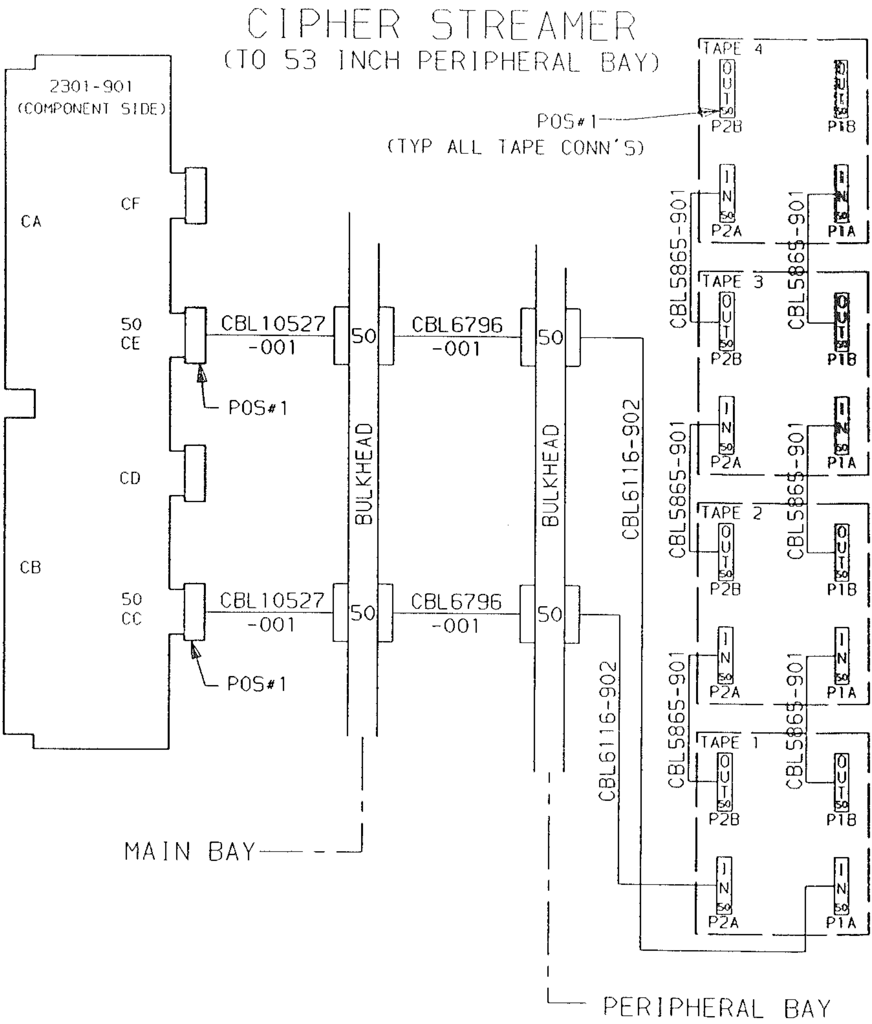


FIGURE 2-61: CIPHER STREAMER CABLING (53-INCH PERIPHERAL BAY)

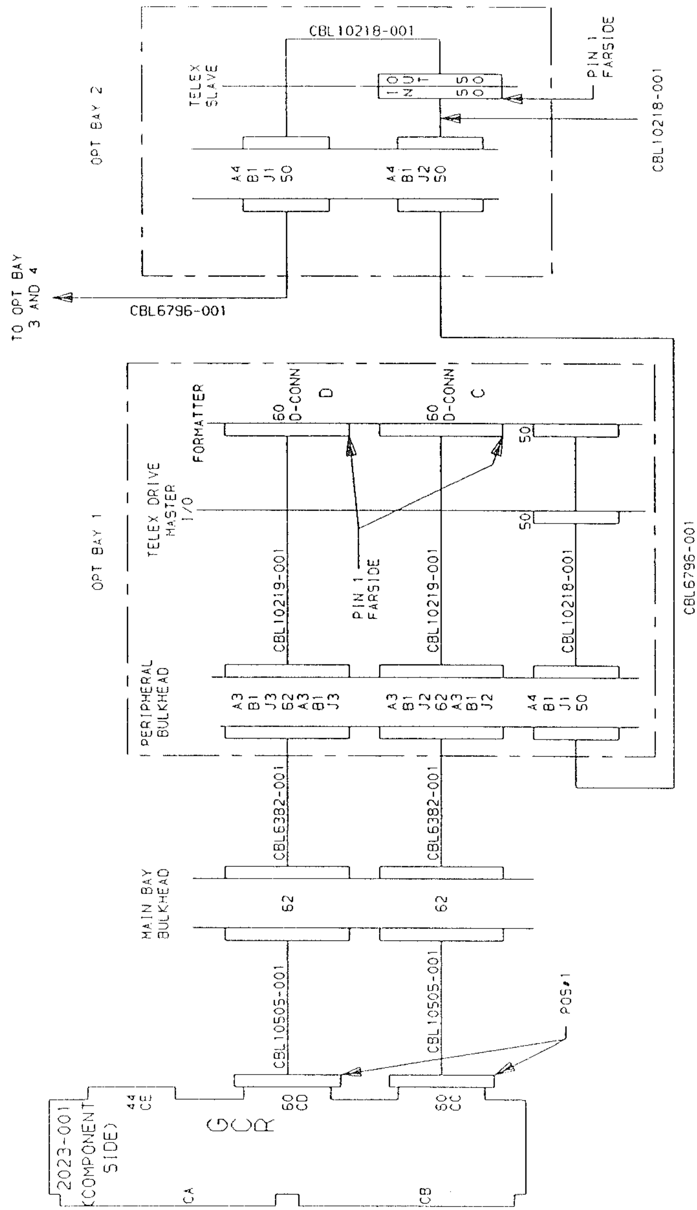


FIGURE 2-62: GCR CABLING

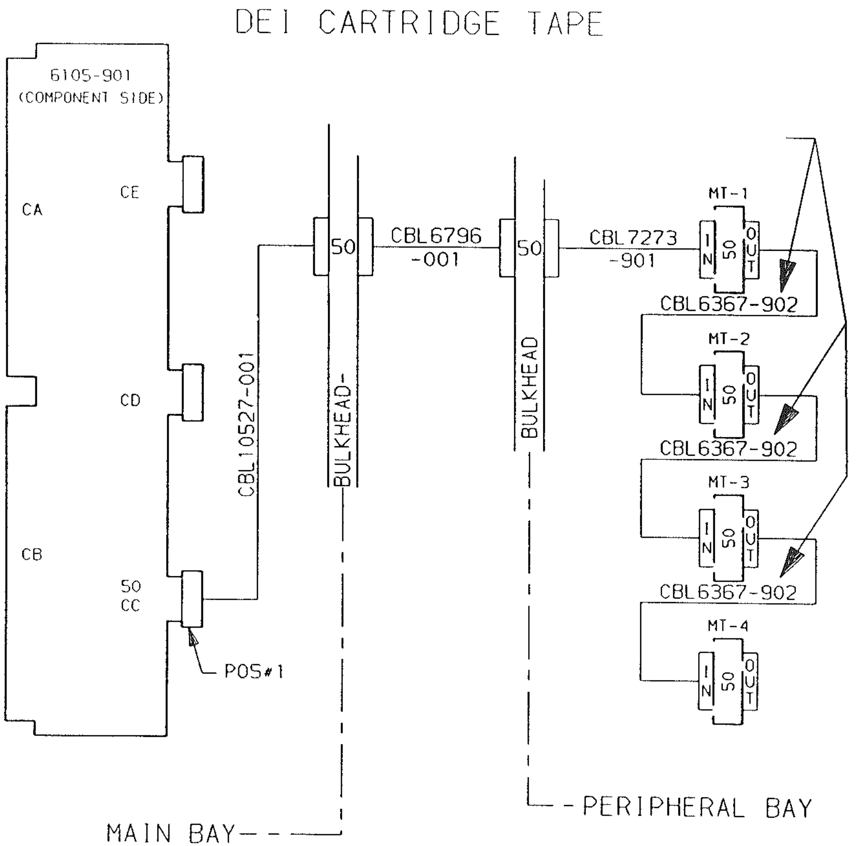


FIGURE 2-63: DEI CARTRIDGE TAPE CABLING

KENNEDY MTT

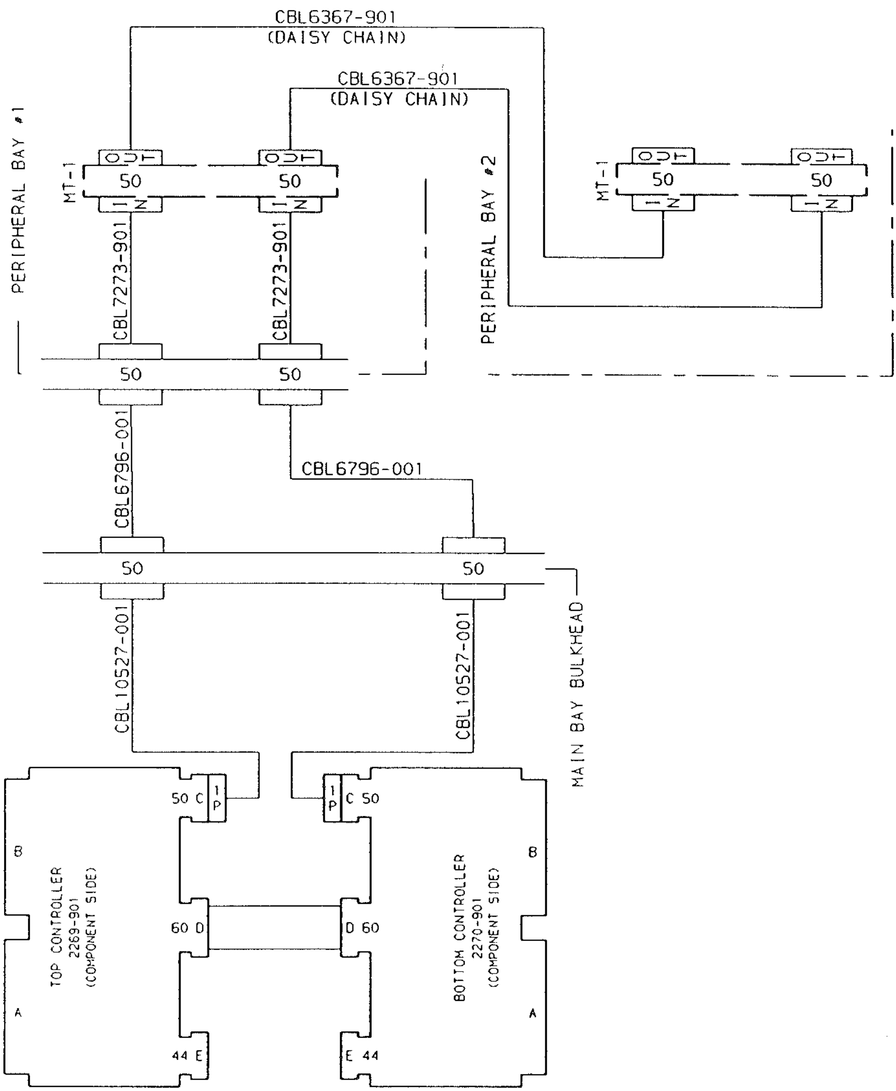


FIGURE 2-64: KENNEDY MTT CABLING

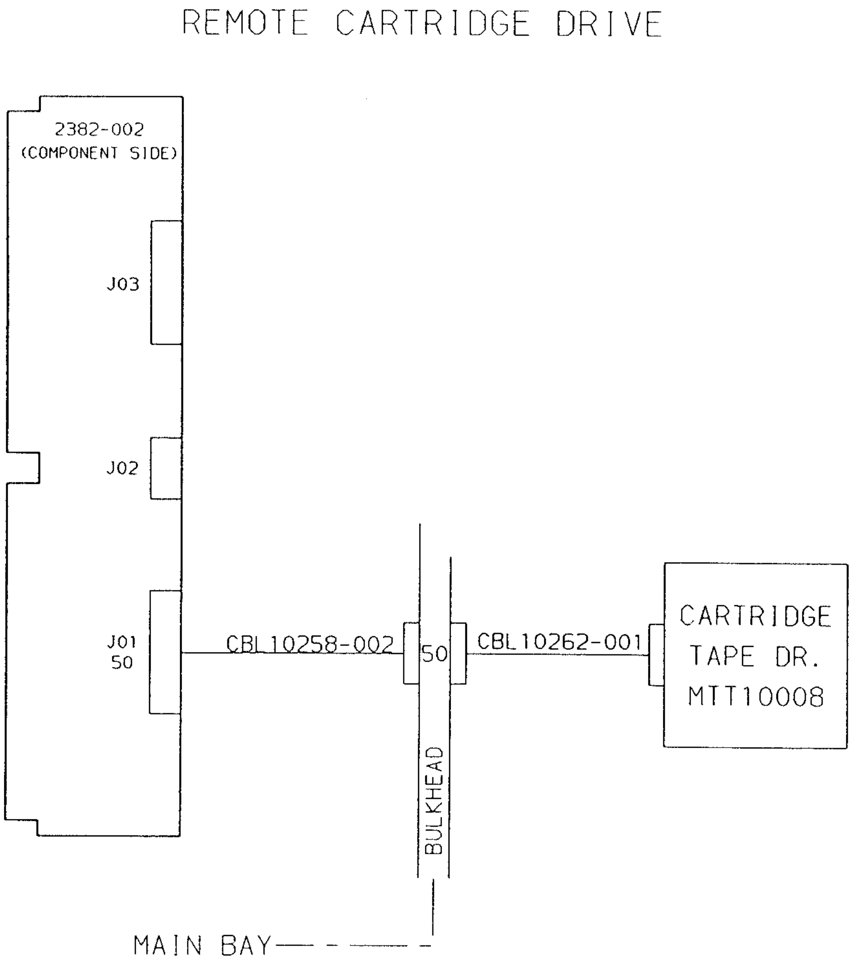


FIGURE 2-65: REMOTE CARTRIDGE TAPE CABLING

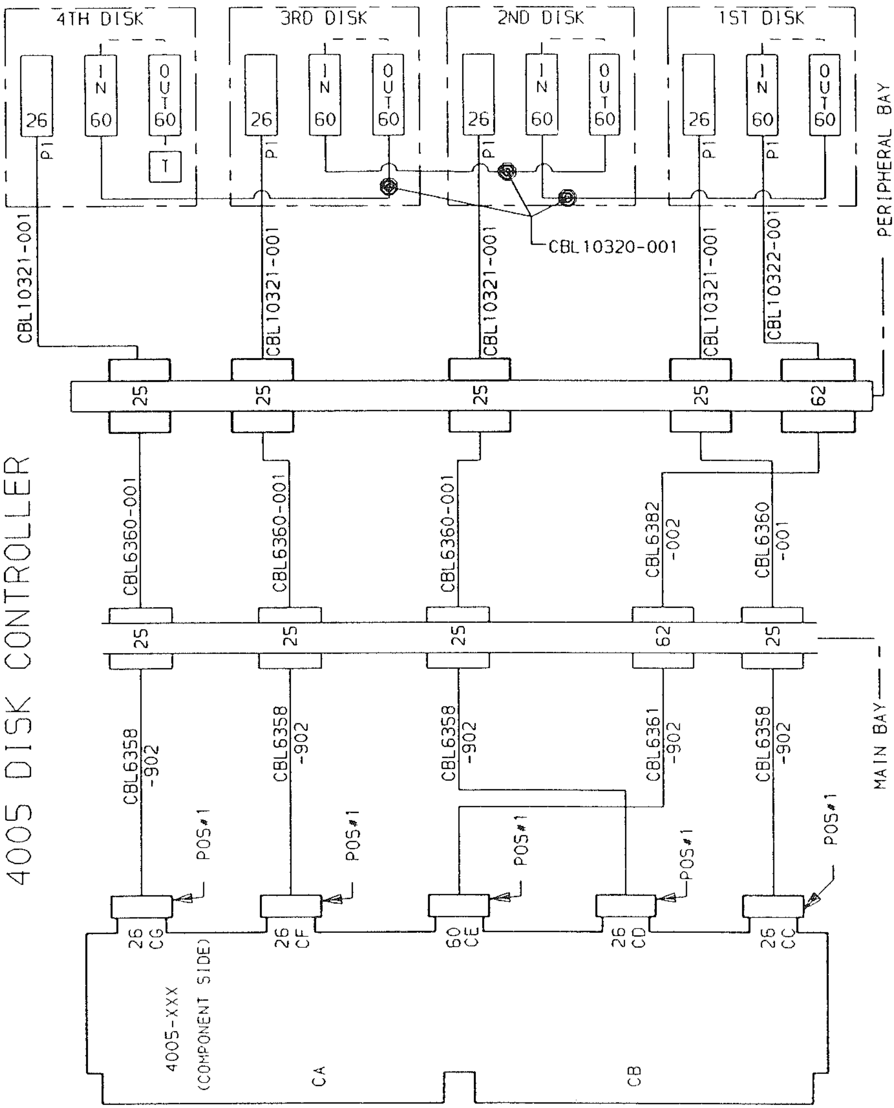


FIGURE 2-66: 4005 DISK CONTROLLER CABLING

URC

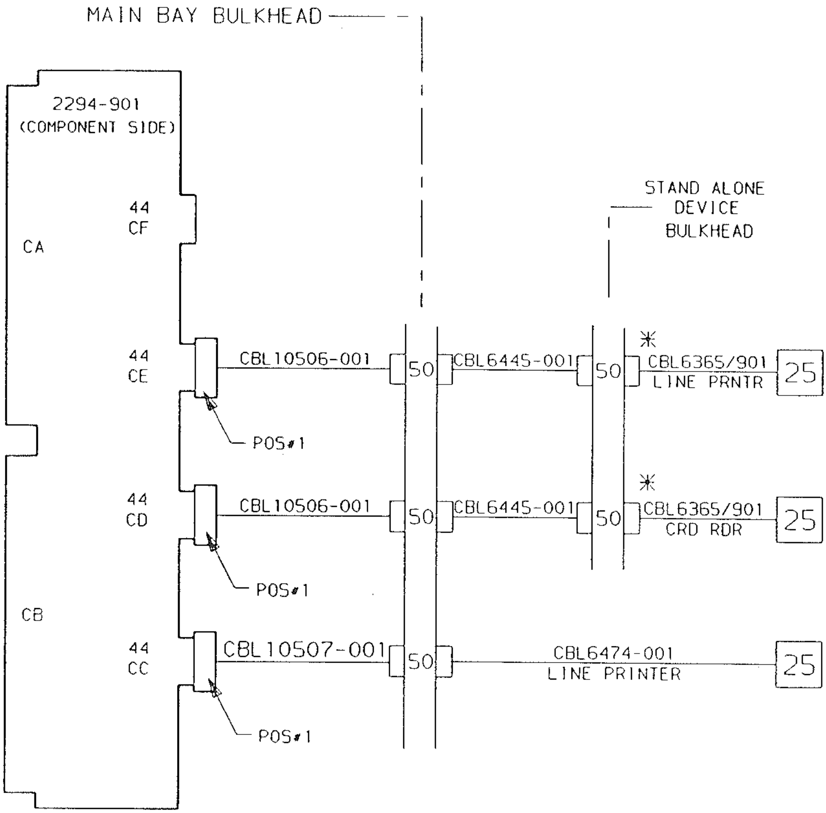


FIGURE 2-67: URC CABLING

IEEE 802.3/ ETHERNET

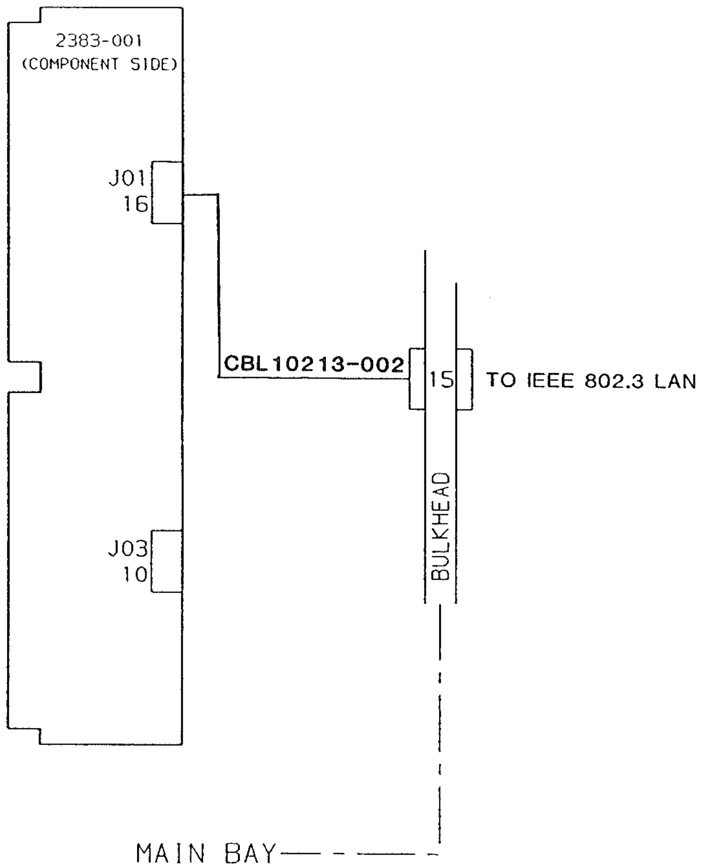


FIGURE 2-68: LHC CABLING

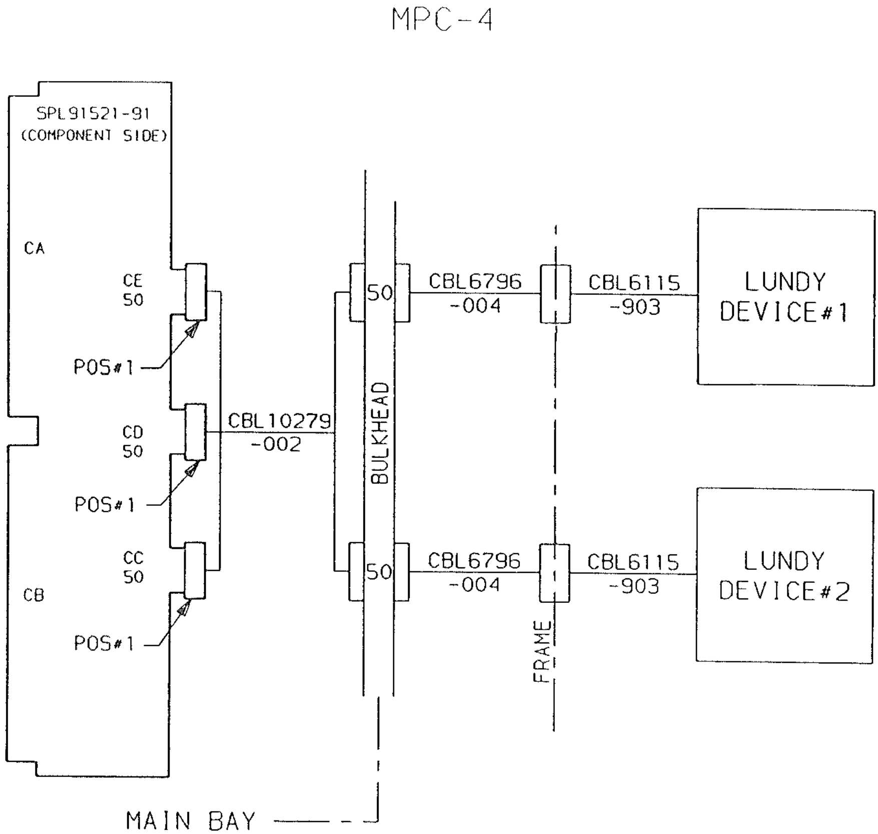


FIGURE 2-69: MPC-4 CABLING

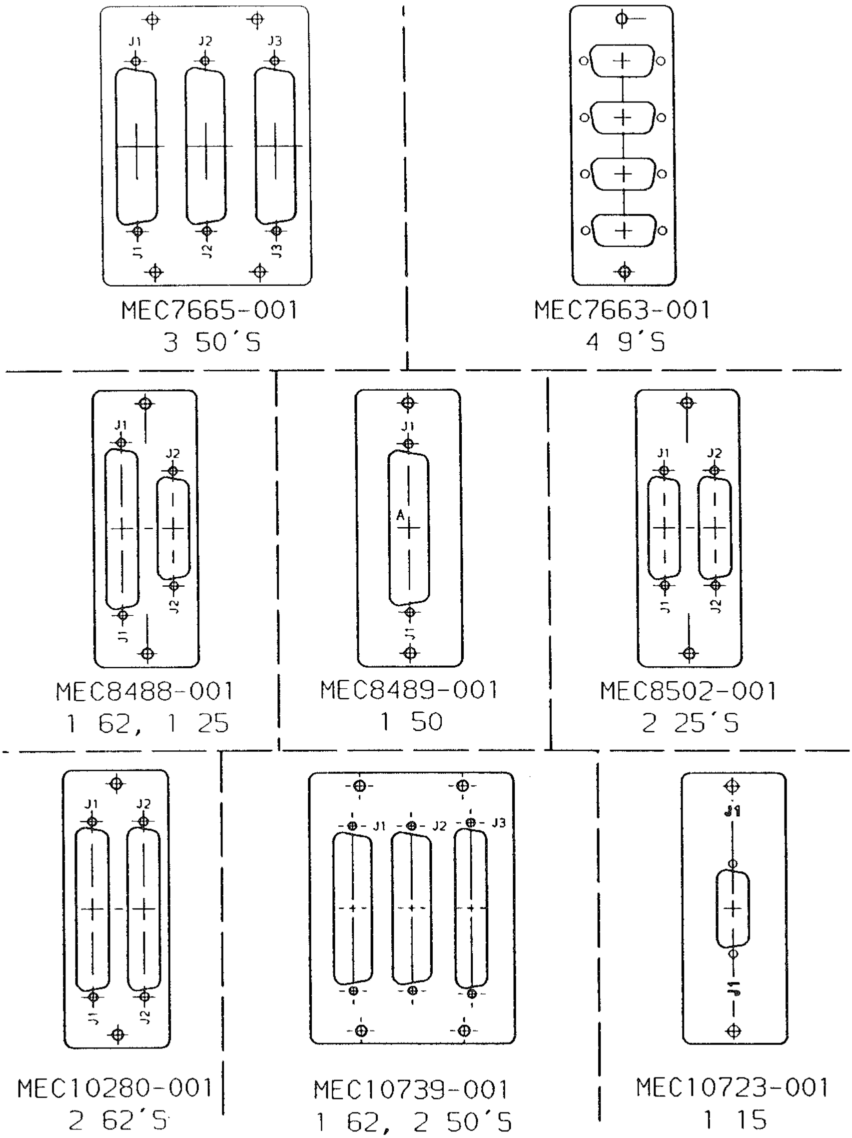


FIGURE 2-70: BULKHEAD PANEL TAPES

1. Verify that the system ac cable is properly connected to the PDU connector and the external power source.

2. Switch the PDU circuit breaker to the ON position. Verify that the PDU power indicator light is on.

3. Power up the system terminal.

4. Verify that the system terminal and VCP-V processor are set to the same baud rate (refer to VCP-V Diagnostic Processor Configuration and Cabling).

5. Verify that the system terminal is set online (refer to the appropriate system terminal service manual).

6. Verify that the key switch behind the floppy disk drive access panel is set to ENABLE.

7. Press the ON/INITIATE SHUTDOWN switch on the control panel. This begins the power-up sequence. The following series of messages are displayed:

```
DPM000: Diagnostic Processor beginning self verification.
DPM020: Sequencing PDU.  Please wait.
DPM001: Diagnostic Processor self verification completed.
        16 Dec 87 14:51:16 Wednesday

DPM350: Loading Configuration Table <n>
DPM021: System power supplies and PDU being tested, please wait.


        Microdiagnostics and Control Program,
        Copyright Prime Computer, 1987.
        All Rights Reserved.

        Proprietary software of Prime Computer Inc.,
        provided under license for use only on a single CPU.
        Except as provided under such license this software
        may not be transferred, disclosed to third parties
        or copied in whole or in part.

DPM800: Sizing Control Store RAM
DPM803: 16K Control Store available
DPM807: Beginning control store address verification
DPM808: Verification completed.
DPM002: Beginning Central Processor verification, please wait.
DPM003: 'SYSV1' successfully completed.
DPM003: 'SYSV2' successfully completed.
DPM003: 'SYSV3' successfully completed.
DPM003: 'SYSV4' successfully completed.
DPM003: 'SYSV5' successfully completed.
DPM003: 'SYSV6' successfully completed.
DPM004: Central Processor system verified
        16 Dec 87 14:56:20 Wednesday

DPM005: Beginning Central Processor system
         Initialization, please wait
```

```
DPM006: Central Processor system initialization completed
        16 DEC 87 14:57:23 Wednesday

DMP007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) 1987, Prime Computer, Inc.]

BOOTING FROM 001060 PRIRUN>PRIRUN.SAVE

CONFIG -DATA CONFIG

Coldstarting PRIMOS, Please wait.

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987
...
...
...
```

8. If any badspots are identified, add them when you make the disk.

9. If any errors occur during power-up and system verification, refer to troubleshooting procedures in chapter 6 of this manual.

10. Run AutoPRIMOS software for several minutes to verify correct installation and system operation.

11. Proceed to Software Installation.

2.10 SOFTWARE INSTALLATION

This section provides a general summary of PRIMOS and chargeable software installation on a new system. For a detailed step-by-step procedure, refer to Module II, Software Installation (SSG082), of PRIMOS and Utilities Software Service Guide (SSG080).

Software installation consists of the following steps:

1. Make the command and paging partitions.

2. Boot PRIMOS from tape

3. Restore PRIMOS to the command partition

4. Install chargeable software

5. Create a CONFIG file

6. Customize the PRIMOS.COMI file

7. Install default SEARCH_RULES list

8. Set ACLs for DSM* Directory

9. Create SAD with Edit_Profile

10. Set up SPOOLER subsystem

11. Boot PRIMOS from disk

Complete the final checkout procedure described in the section that follows.

2.11 FINAL CHECKOUT

This section describes the final system checkout procedure. If any errors occur, refer to Chapter 6, Troubleshooting, in this manual.

1. Enter Control Panel mode by pressing ESCAPE ESCAPE. Run all microdiagnostic routines as outlined in Chapter 6 of this manual.

2. Reboot the system from disk to bring up PRIMOS.

3. Complete all Customer Service and System Installation reports.

2.12 DAMAGED/MISSING EQUIPMENT CORRECTIVE PROCEDURES

If damaged or missing equipment is noticed during unpacking, select the appropriate corrective action:

- Reporting Damaged Equipment
- Reporting Wrong Equipment Shipped
- Reporting Short Shipment
- Ordering Parts

2.12.1 REPORTING DAMAGED EQUIPMENT

If damaged equipment is discovered during unpacking, complete the following procedure:

1. DO NOT repair or install any damaged equipment before an insurance claim inspection is completed. Equipment may be opened to inspect for damage. When unpacking, retain all shipping material in case a module must be returned.

2. Get a copy of the waybill/delivery receipt from the customer. Record the following information on the installation report:

   - Customer Name
   - Customer Address
   - Sales Order (SO) Number
   - Delivery Date

3. If the delivering carrier is available, have his agent inspect the damage. Give a copy of the damage report to the Customer Service Administrator who will forward the report to:

   Prime Computer, Inc.
   Customer Service Material Control
   145 Pennsylvania Avenue
   Framingham, MA 01701

4. Finance will order a replacement device through Order Processing.

5. Order Processing will contact the Customer Service Administrator with the order number and status of order.

2.12.2 REPORTING WRONG EQUIPMENT SHIPPED

If the wrong equipment is shipped, complete the following procedure:

1. Record the following information on the installation report:

   - Customer Name
   - Customer Address
   - Sales Order (SO) Number

2. Call Order Processing to place an emergency wrong ship order. (Refer to Ordering Parts in this chapter).

3. Generate a packing slip on SIMS system and return wrong shipped items to your Logistics Administrator.

2.12.3 REPORTING SHORT SHIPMENT

If a short shipment is discovered during unpacking, complete the following procedure:

1. Record the following information on the Installaton Report:

   - Customer Name
   - Customer Address
   - Sales Order (SO) Number

2. Call Order Processing to place an emergency short ship order. (Refer to Ordering Parts in this chapter.)

3. Complete the installation of the system.

2.12.4 ORDERING PARTS

This subsection provides procedures for the following:

- Ordering Individual Parts
- Ordering Kit Parts

<u>2.12.4.1 Ordering Individual Parts</u>

To order individual parts:

1. Determine the priority of the part needed:

- Emergency (EM) - Customer is down (or initial install)
- Non-Emergency (RS) - Restock shelf spares.

2. Call your Logistics Administrator or Branch Manager to get the needed part. They will inform you if the part is available or if you will need to order it.

3. If the part is not available and it is an emergency order, call Order Processing to place the order. Provide the following information:

   - Customer Name
   - Sales Order (SO) Number
   - CSR Badge Number
   - Ship to Warehouse
   - Ship-To Address
   - Model/Serial Number of device
   - Part Number and quantity

4. After providing the information, ask for the order number.

<u>2.12.4.2 Ordering Kit Parts</u>

If a kit part was used to replace a missing or damaged part, complete the following procedure to order the kit part(s):

1. Complete defective tags as needed for <u>EACH</u> part used.

2. Tie the appropriate tag to each part and put the bad parts into the kit case.

3. Call your Logistics Administrator or Branch Manager to get the needed part. They will inform you if the part is available or if you will have to order it.

4. If the part is not available, provide the following information:

   - Customer Name
   - Sales Order (SO) Number
   - CSR Badge Number
   - Ship to Warehouse
   - Ship-To Address
   - Model/Serial Number of device
   - Part Number and quantity

5. After providing the information, ask for the order number.

CHAPTER 3
OPERATING INSTRUCTIONS

This chapter provides the operating instructions for the following Model 4050/4150 system components and operations:

- Controls and Indicators
- Floppy Disk Drive
- PRIMENET Node Controller (PNC)
- Intelligent Communications Controller 3 (ICS3)
- System Power-up and Autoboot to PRIMOS
- Power-Down
- Terminal Ports
- VCP-V Diagnostic Processor
- Informational Message Summary
- Basic PRIMOS Operations
- Distributed System Management (DSM) Operations

3.1 CONTROLS AND INDICATORS

Locations and functions for the following Model 4050/4150 system controls and indicators are provided in this section:

- Status Panel
- Power Distribution Unit (PDU)
- 7778 Power Supply
- Floppy Disk Drive
- Model 4735 Disk Drive (496Mb)
- Model 4835 Disk Drive (770Mb)
- Model 4587 Tape Drive (Quad-Density)
- PRIMENET Node Controller & Modular Junction Box
- Intelligent Communications Controller 3 (ICS3)
- Other System and Board Indicators

3.1.1 STATUS PANEL CONTROLS AND INDICATORS

Tables 3-1 and 3-2 describe status panel controls and indicators (see Figure 3-1).

NOTE

The On/Initiate Shutdown, Remote Enable, and Remote Privileged pushbutton control switches are also indicator lights.

TABLE 3-1: SYSTEM STATUS PANEL CONTROLS

CONTROL	FUNCTION
ON/INITIATE SHUTDOWN	When the system is OFF, and the main ac circuit breaker is ON, pressing ON/INITIATE SHUTDOWN instructs the Diagnostic Processor (VCP-V) to allow the PDU to begin supplying ac to the system card cage, initiating the AutoBoot Sequence. When the system is running, pressing ON/INITIATE SHUTDOWN instructs the VCP-V to begin a Soft Shutdown Sequence. The VCP-V logs out all users and shuts down PRIMOS, after the CPU halts, or a 10 minute timeout expires.
MASTER CLEAR	Pressing MASTER CLEAR halts the CPU, clears any errors on the CPU and peripheral controllers, and places the supervisor terminal in CP (Control Panel) mode. Pressing MASTER CLEAR disconnects all remote users on the system.
REMOTE ENABLE	Pressing REMOTE ENABLE allows an operator at a remote terminal to monitor the activity at the privileged local system console. Any keyboard input from the remote system console is ignored unless the terminal is privileged by pressing the REMOTE PRIVILEGE button. Pressing REMOTE ENABLE a second time disables the remote system console, preventing the operator from monitoring the activity of the privileged local system console.

TABLE 3-1: SYSTEM STATUS PANEL CONTROLS (CONT.)

CONTROL	FUNCTION
REMOTE PRIVILEGE	Pressing this switch allows an operator at a remote system console to execute commands from that console. Before the remote system console can be privileged, it must be enabled by pressing REMOTE ENABLE, causing the REMOTE ENABLE LED to light. The local system console may only monitor activity if the REMOTE PRIVILEGE, but not the REMOTE ENABLE button is pressed. Any keyboard input from the local console is ignored. When the remote console is privileged, pressing REMOTE PRIVILEGE removes that privilege, shifting it to the LOCALl system console. If REMOTE ENABLE is active the remote operator can still monitor system console activity.
LOCK/ENABLE KEYSWITCH	This two-position keyswitch enables the MASTER CLEAR, REMOTE ENABLE, and REMOTE PRIVILEGE buttons when the switch is in the ENABLE position. When the switch is in the LOCK position, pushing any of these buttons has no effect. Also, when the switch is in the LOCK position, the supervisor terminal is locked in its current terminal mode. LOCK/ENABLE does not affect operation of the ON/INITIATE SHUTDOWN button.

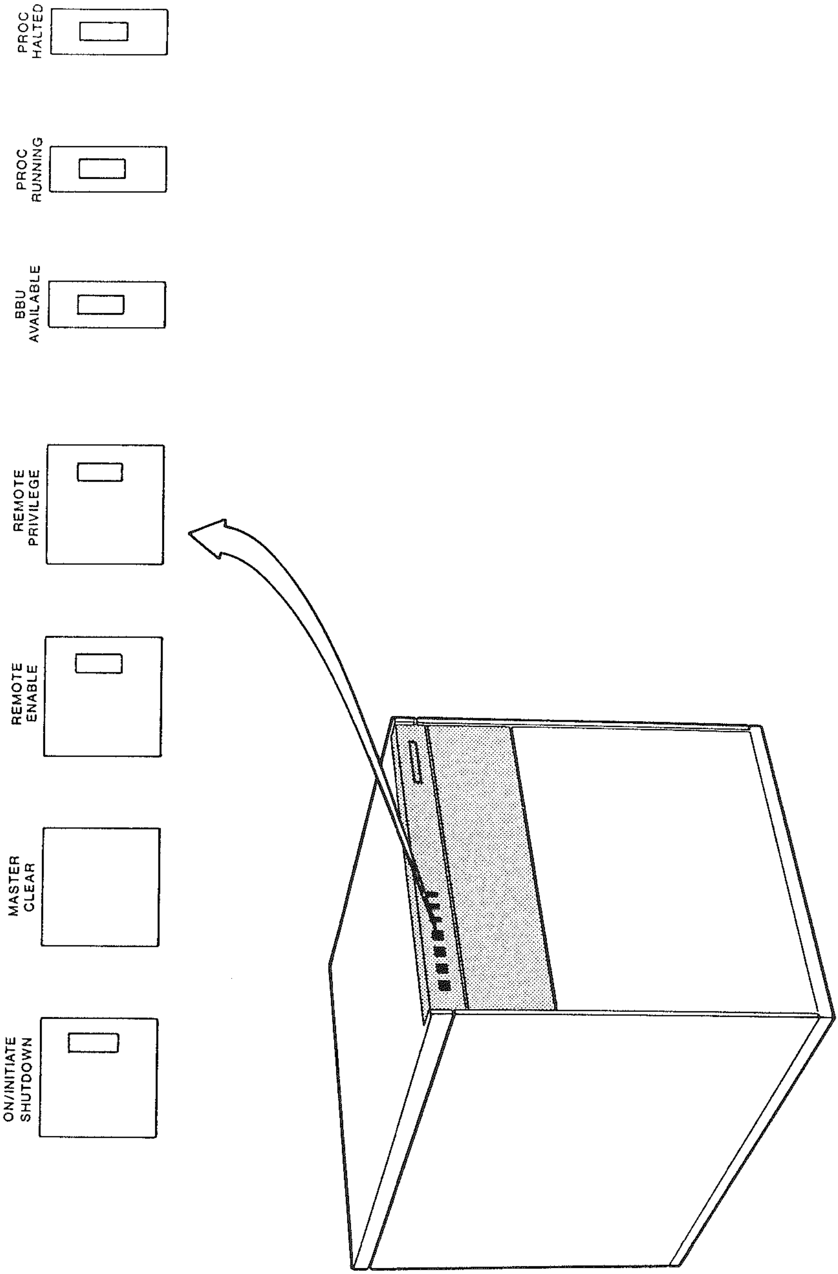


FIGURE 3-1: SYSTEM STATUS PANEL

Table 3-2 describes the six LED indicators on the status panel.

TABLE 3-2: STATUS PANEL INDICATORS

INDICATOR (LED)		DESCRIPTION
ON/INITIATE SHUTDOWN		
On		System is running
Off		System is shutdown
Blinking		Soft Shutdown Sequence in progress
REMOTE ENABLE	REMOTE PRIVILEGE	REMOTE TERMINAL IS:
Off	Off	Disabled and Inactive
On	Off	Enabled and Inactive
On	On	Enabled, Privileged, and Inactive
Blinking	Blinking	Disabled and Active
Blinking	Off	Enabled and Active
On	Blinking	Enabled, Privileged, and Active
BBU AVAILABLE		
Off		MBBU Power is not Available
On		MBBU Power is Available
Blinking		A Power Fail has occurred and the MBBU is preserving memory.
PROC RUNNING		
On		CPU is running, not halted
PROC HALTED		
On		CPU has halted, not running (The LED always lights when you press the MASTER CLEAR button.)

3.1.2 POWER DISTRIBUTION UNIT (PDU) CONTROLS AND INDICATORS

A circuit breaker, shown in Figure 3-2, controls ac power to the PDU.

When the circuit breaker is in the ON (LEFT) position, the status panel ON/INITIATE SHUTDOWN switch can be used to power up or power down the system.

A PDU power indicator light (see Figure 3-2) turns on when ac power is applied to the PDU and the circuit breaker is in the ON (LEFT) position.

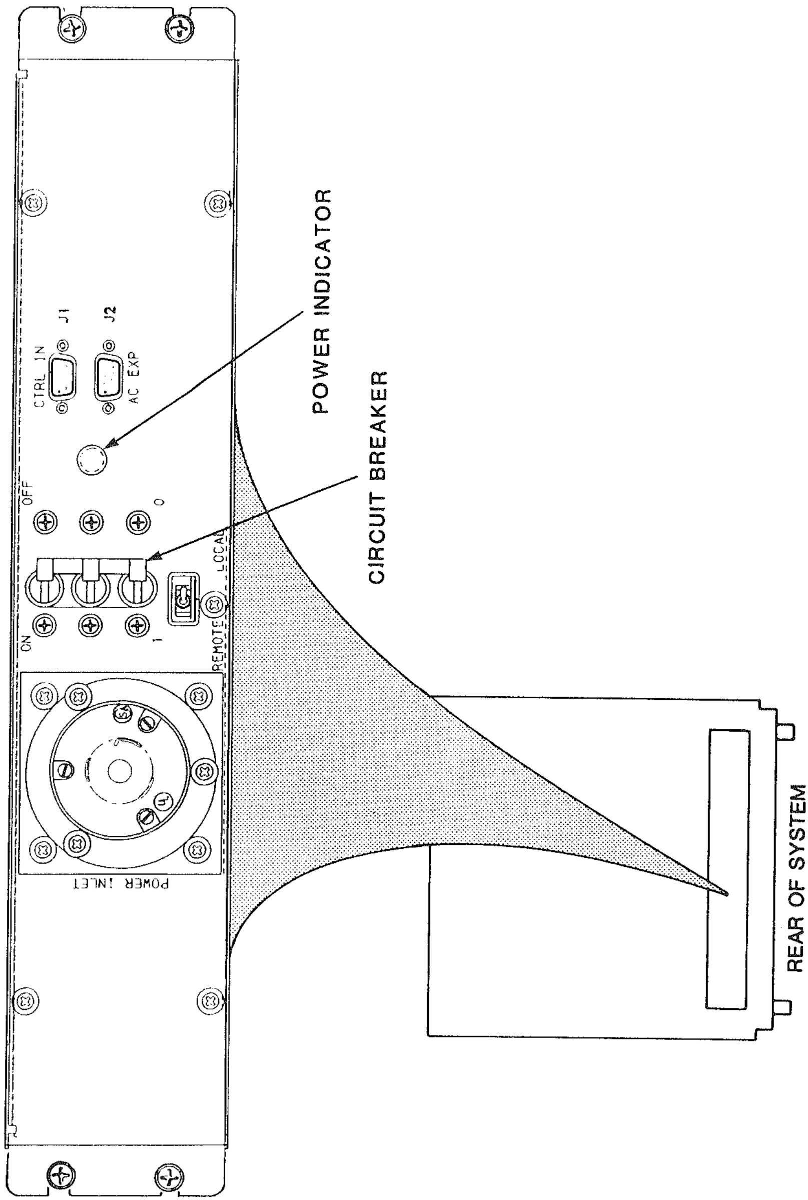


FIGURE 3-2: MAINBAY POWER DISTRIBUTION UNIT

3.1.3 TLA10113 POWER SUPPLY CONTROLS AND INDICATORS

The TLA10113 power supply has three LED indicators to provide status information. The diagnostic meanings of the three indicators, shown in Figure 3-3, are described in Table 3-3. Refer to Troubleshooting System Power Supply Failures in Chapter 6 of this manual for additional power supply status LED information.

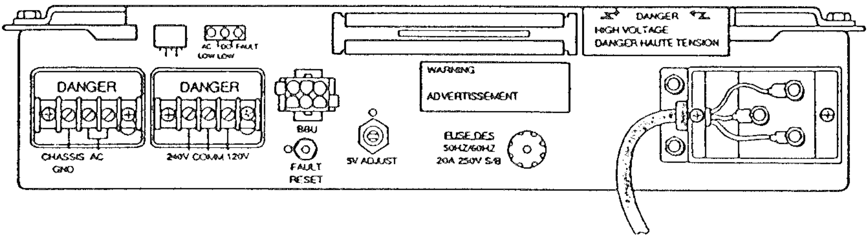


FIGURE 3-3: TLA10113 POWER SUPPLY LEDS

TABLE 3-3: TLA10113 POWER SUPPLY LEDs

LED	COLOR	STATUS	MEANING
AC Low*	Yellow	ON	Power supply is operating correctly.
		OFF	AC power has dropped or been lost.
DC Low*	Green	ON	Power supply is operating correctly.
		OFF	Power supply dc outputs have dropped or been lost.
Fault	Red	OFF	Power supply is operating correctly, or ac power has been lost for more than one minute.
		ON	AC power to the supply has been lost which has turned ON the fault LED.

* The silkscreen labels AC Low and DC Low will be changed on future power supplies to read AC OK and DC OK.

3.1.4 FLOPPY DISK DRIVE CONTROLS AND INDICATORS

The two floppy disk drives have no controls. Each has one LED indicator that lights when the drive is activated.

3.1.5 MODEL 4735 DISK DRIVE CONTROLS AND INDICATORS

Model 4735 (496Mb) disk drive controls and indicators are located on the operator's panel, shown in Figure 3-4.

The operator controls and indicators are described in the paragraphs that follow.

- LOGIC PLUG/UNIT SELECTED INDICATOR - The logic plug activates switches that determine the device's logical address (Ø-3). The unit selected indicator lights when the drive is selected.

- START SWITCH/READY INDICATOR - This switch is alternate action with a corresponding indicator. When first pressed, the switch spins up the disk drive. When pressed a second time, the switch spins down the disk drive. The indicator flashes as the drive is spinning up and lights steadily when the drive is in a ready state. The indicator flashes while the drive is spinning down and goes out when the rotation has stopped.

- FAULT CLEAR SWITCH/FAULT INDICATOR - This switch is momentary action with a corresponding indicator. When a fault is detected, the indicator lights. To clear the fault, press the fault button.

- WRITE PROTECT SWITCH/INDICATOR - This switch is alternate action with a corresponding indicator. To prevent disk write operations, press the switch. The indicator lights. To resume write operations, press the switch again. The indicator goes out.

Refer to <u>496 Megabyte Fixed Module Disk Subsystem</u> (SPM47Ø) for additional operator's information and troubleshooting procedures.

3.1.6 MODEL 4835 DISK DRIVE CONTROLS AND INDICATORS

Model 4835 (77ØMb) disk drive controls and indicators are located on the operator's panel, shown in Figure 3-5.

The following paragraphs describe operator controls and indicators.

- READY - This indicator lights when the spindle reaches full speed and on-cylinder status without faults.

- START/STOP - This switch is alternate action with a corresponding indicator. When first pressed, the switch spins up the disk drive. When pressed a second time, the switch spins down the disk drive. The indicator lights steadily as the drive is spinning up and goes out when the drive is spun down.

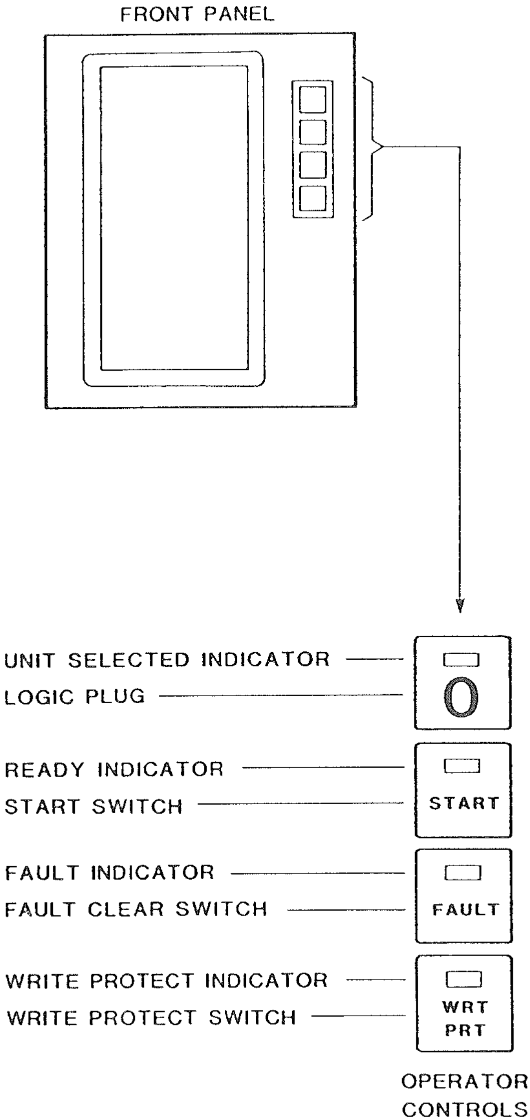


FIGURE 3-4: MODEL 4735 DISK DRIVE CONTROLS AND INDICATORS

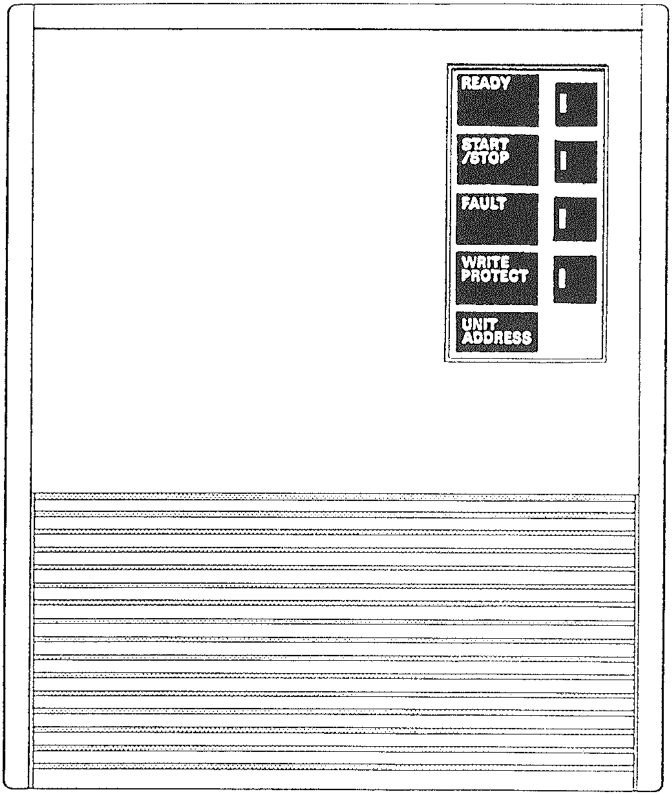


FIGURE 3-5: MODEL 4835 DISK DRIVE CONTROLS AND INDICATORS

- FAULT - This switch is momentary action with a corresponding indicator. When a fault is detected, the indicator lights. To clear the fault, press the fault button.

- WRITE-PROTECT - This switch is alternate action with a corresponding indicator. To prevent disk write operations, press the switch. The indicator lights. To resume write operations, press the switch again. The indicator goes out.

- UNIT ADDRESS - This indicator is a magnetic label that is placed to the right of the identifier. These labels are supplied with the drive.

Refer to <u>770 Megabyte Fixed Storage Disk Subsystem</u> (SPM390) for additional operator's information and troubleshooting procedures.

3.1.7 MODEL 4587 TAPE DRIVE CONTROLS AND INDICATORS

Model 4587 (quad-density) tape drive controls and indicators are located on the operator's panel, shown in Figure 3-6.

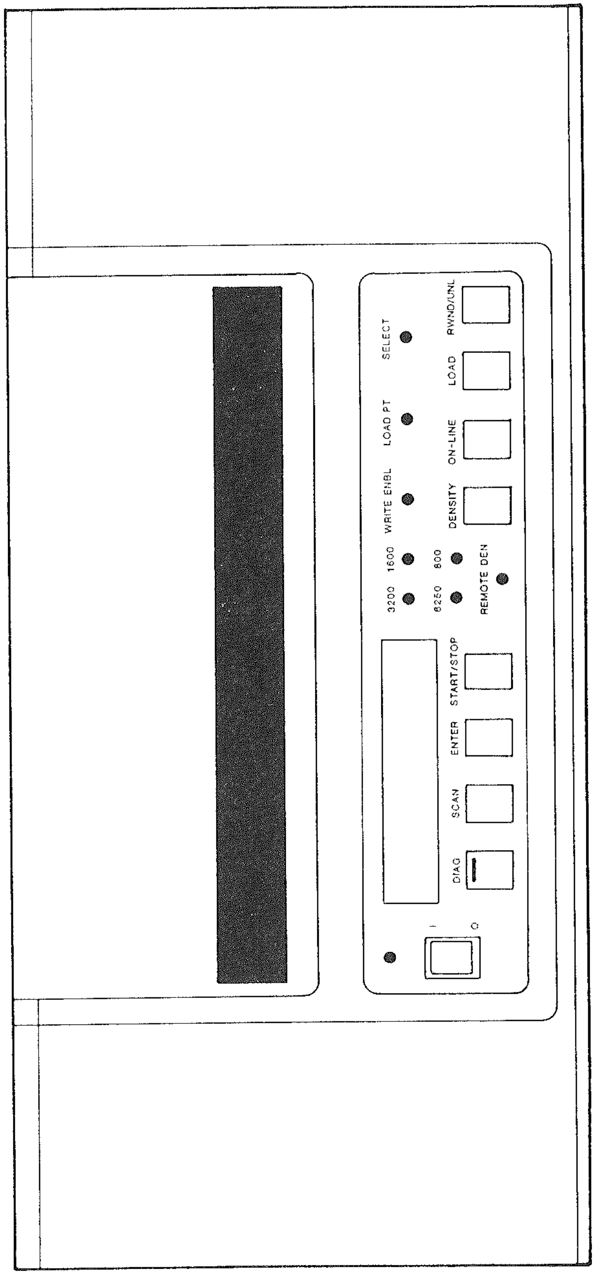


FIGURE 3-6: MODEL 4587 TAPE DRIVE CONTROLS AND INDICATORS

The following paragraphs describe operator controls and indicators.

- DISPLAY PANEL - is an eight-character display that provides the operating mode, status, errors, tape drive parameters, and diagnostic messages.

- ON/OFF - controls power to the unit. Power is ON when the switch is in the 1 position. Power is OFF when the switch is in the 0 position. The unmarked green indicator light is on when power is applied to the device.

- DIAG - turns diagnostics on and off when the unit is off-line. The green indicator light is on when the device is in diagnostics mode.

- SCAN - scrolls through the diagnostic and calibrate menus.

- ENTER - executes selected commands while in diagnostic or calibrate mode.

- START/STOP - starts and stops selected commands when in diagnostic or calibrate mode.

- REMODE DEN - is a green LED that indicates the ability to select tape density from a terminal via the ASSIGN command.

- 800/1600/3200/6250 - are green LEDs that indicate the selected tape density in bits per inch (BPI). The default is 1600 BPI.

- DENSITY - selects tape density and enables REMOTE DEN. One density indicator and the REMOTE DEN indicator must be lit before density can be assigned from a terminal.

- ONLINE - places the drive on and off line. The online indicator lights when the button is pressed. Pressing the button again takes the device off line.

- LOAD - initiates the load sequence. The indicator blinks once at the start of the sequence and remains on when tape load is complete.

- RWND/UNL - rewinds or unloads the tape when the drive is off-line.

- WRITE ENBL - is an indicator that lights when the tape reel write-enable ring is in place.

- LOAD PT - is an indicator that blinks once during load and unload. The indicator remains on when the tape reaches its load point.

- SELECT - is an indicator that blinks constantly indicating that the tape drive is on-line and operating correctly. The light remains on while the CPU is communicating with the drive.

Refer to <u>Model 4587 Tape Drive Service Procedures Manual</u> (SPM920) for additional operator's information and troubleshooting procedures.

3.1.8 PNC & MODULAR JUNCTION BOX CONTROLS AND INDICATORS

This section provides control and indicator information for the following PRIMENET components:

- PNC-II Controller
- Modular Junction Box

Operating procedures for the PNC-II controller (2384-001) and modular junction box are described under PRIMENET Node Controller Operations in this chapter.

3.1.8.1 PNC-II Controller

The PNC-II has six LEDs on the right-hand edge of the board as seen from the back of the cabinet (refer to Figure 3-7).

```
Controller Status                          Network Status
    1       2                           3      4      5      6
  Green    Red                       Yellow Yellow   Red    Red
 --(O)----(O)-------------------------(O)----(O)-----(O)----(O)--

                                      Ring   Node    Ring   J-Box
  Good    Error                       Up     Active  Down   Fault
                                    +----------------------+
                                          Duplicated on
                                        Bulkhead interface
```

FIGURE 3-7: PNC-II BOARD LEDS

During normal operation of PRIMENET, the green Controller Status light is on. The yellow Network Status lights also are on, with some flickering of the Node Active light, according to the amount of activity on the network.

The LEDs also serve as indicators for self-verify routines (refer to Table 3-4). See Chapter 6 for the use of LEDs in error detection.

TABLE 3-4: PNC-II BOARD LEDS

LED	COLOR	MEANING WHEN LIT
1	green	Controller status good
2	red	Controller status bad
3	yellow	Ring is up
4	yellow	This node active
5	red	Ring is down
6	red	Junction Box disconnected

3.1.8.2 Modular Junction Box

The modular junction box has a toggle switch to allow manual disconnect of the node from the network. Toggling the switch to the NORMAL position allows the node to be active.

NOTE

> Pull the toggle switch towards you to unlock it before throwing the switch left or right.

Either in the NORMAL or DISCONNECT positions, a power-off condition disconnects the node from the network. It is not necessary to toggle this switch before installing or replacing PNC components.

The MJ-BOX has three LEDs indicating network status and activity (refer to Table 3-5).

Normal indications are a steady green UP light, (Ring up, node not active), or a steady green UP and a blinking green ACTIVE light (Ring up, Activity).

- UP LED steady green: Network Active, Token Circulating
- ACTIVE LED blinking green: Node Active, Packets In/Out
- DOWN LED red: Network Down, Token Not Circulating

NOTE

> When the modular junction box is configured with the old PNC controller (2257-902), the UP, ACTIVE, and DOWN LEDs are invalid.

Refer to Figure 3-8 for an illustration of the MJ-Box.

TABLE 3-5: MJ-BOX LEDS

STATE	LED NAME			MEANING
	UP	ACTIVE	DOWN	
1	GREEN	BLINK	off	Ring Net UP, Normal Activity
2	GREEN	off	off	Ring Net UP, Node not active
3	off	GREEN	RED	Ring DOWN, Token not circulating, Carrier Detect from upstream PNC

TABLE 3-5: MJ-BOX LEDS (CONT.)

STATE	LED NAME			MEANING
	UP	ACTIVE	DOWN	
4	off	off	RED	Ring DOWN, Token not circulating, NO Carrier Detect from upstream PNC
5	off	off	off	System Powered Off or Power-up Sequence of CPU failed. RING disconnected.
6	GREEN	GREEN	RED	Normal during Power-Up sequence. After Power Up: PNC self-verify failed.

NOTE

During the system power-up sequence State 6 is normal. After the power-up is completed, State 1 or 2 is normal.

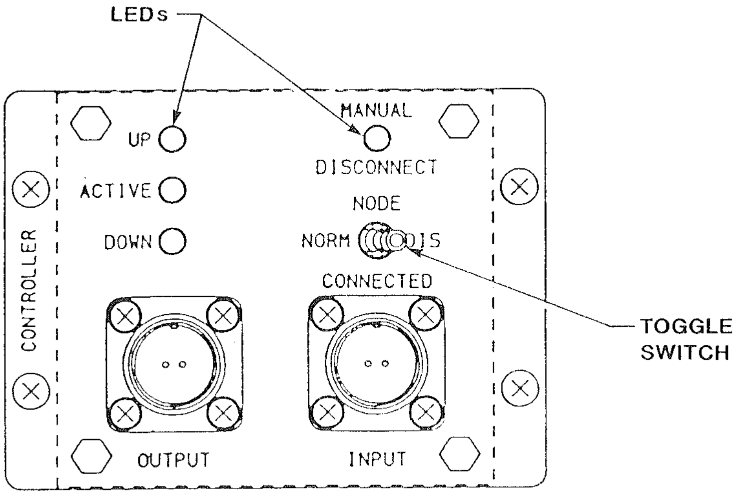


FIGURE 3-8: PNC MJ-BOX CONTROLS AND INDICATORS

3.1.9 ICS3 CONTROLS AND INDICATORS

The ICS3 controls and indicators are on the following subsystem components:

- Controller Board
- Buffer Card
- Power Supply

3.1.9.1 ICS3 Controller Board Indicators

The ICS3's printed circuit controller board (see Figure 3-9) has four red board-edge mounted LEDs.

Each LED monitors a separate system operation and either blinks or remains lighted to indicate specific conditions. If the ICS3 LEDs indicate a hardware error(s), refer to Chapter 6 of this manual. See Figure 3-9 and Table 3-6 for a description of ICS3 LEDs.

TABLE 3-6: ICS3 CONTROLLER BOARD LEDS

FUNCTION	DESCRIPTION
LAC card cage power	Steady ON = Power level normal Flashing = Power failure
Memory parity	Steady ON = Parity normal Flashing = Single bit parity error
Writeable Control Store (WCS)	Steady ON = Fatal WCS parity error OFF = Parity normal
RUN indication	Steady ON = Operating System halted Flashing = Operating System running

NOTE

All LEDs flash when multiple bit errors are detected.

3.1.9.2 ICS3 Buffer Card Indicators

The ICS3's buffer card (see Figure 3-10) has one green board-edge mounted LED.

The LED lights when dc LAC backplane power is present.

3.1.9.3 ICS3 Power Supply Controls and Indicators

The push button on the 16-slot card cage's power supply (see Figure 3-10) controls power to the buffer cards and LAC bus backplane. A green light inside the control button indicates the power supply is on.

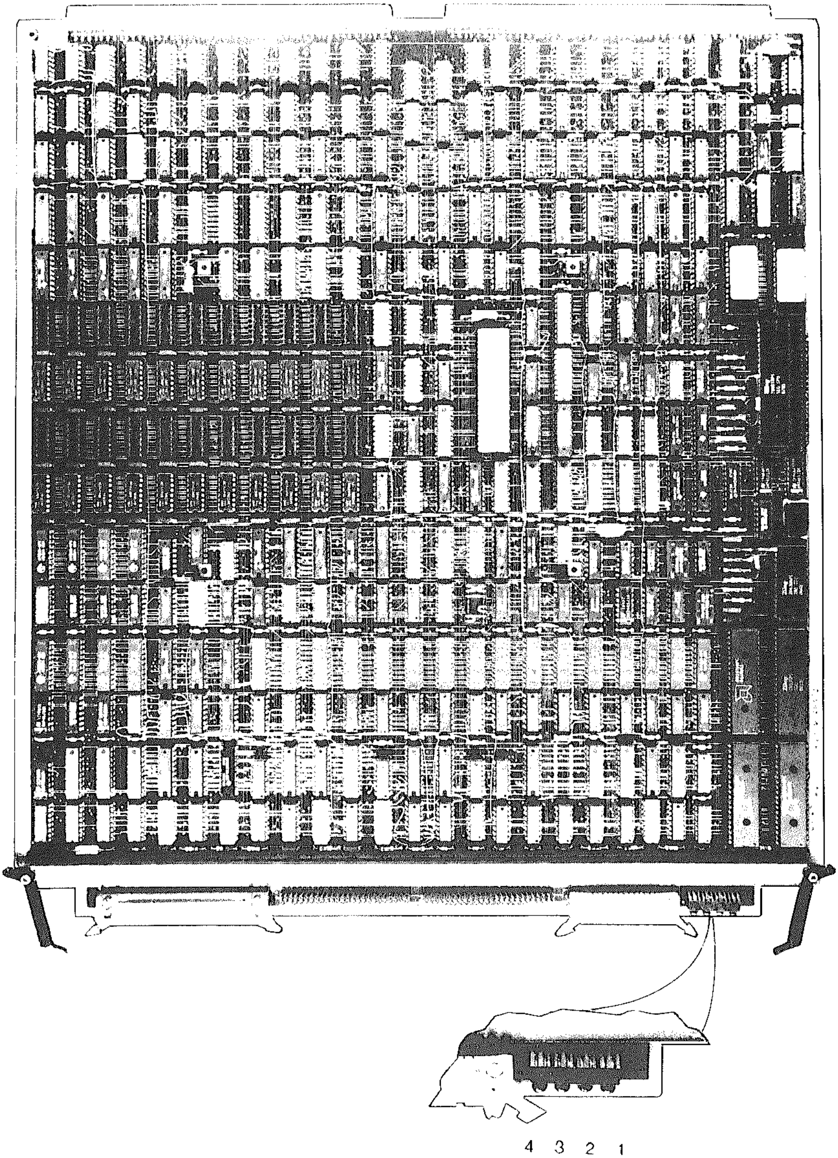


FIGURE 3-9: ICS3 CONTROLLER LEDS

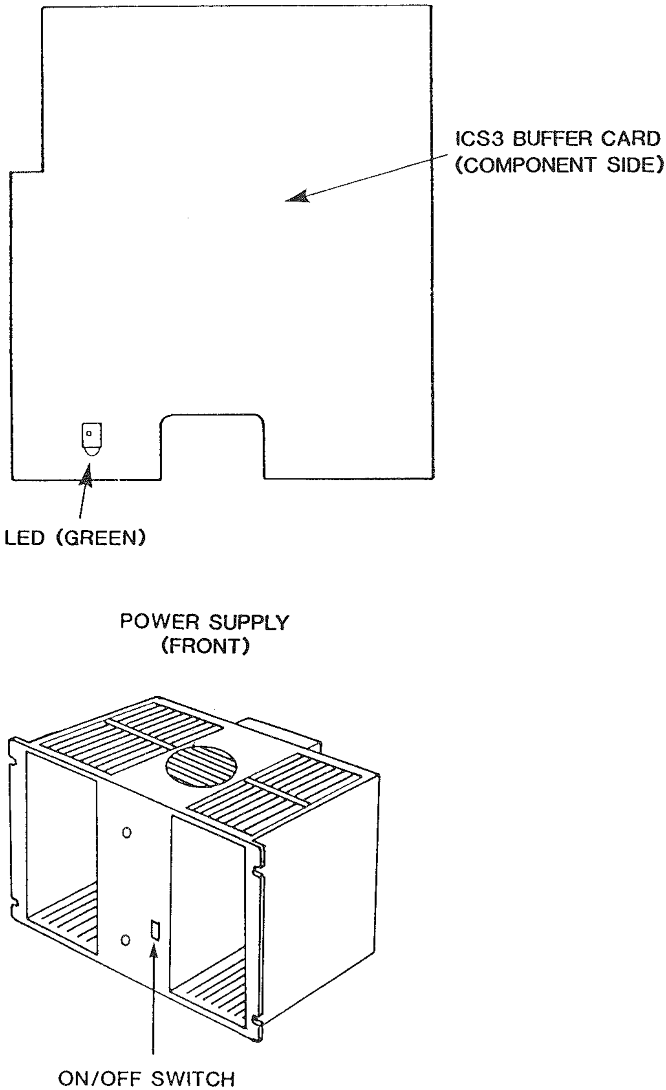


FIGURE 3-10: ICS3 LEDS

3.1.10 OTHER SYSTEM AND BOARD INDICATORS

Table 3-7 describes other indicators in the Model 4050/4150 system.

TABLE 3-7: OTHER SYSTEM AND BOARD INDICATORS

LOCATION	DESCRIPTION
Diagnostic Processor (VCP-V)	Four LEDs located on the VCP board. Diagnostic meanings of the LEDs are detailed in Chapter 6 of this manual. Only the green LED is lit when the Diagnostic Processor is functioning properly.
MBBU	Three LEDs on the front panel of the optional MBBU indicate the status of the MBBU. Refer to Chapter 6 of this manual for LED patterns.
Model 6380 Intelligent Disk Controller	Six LEDs on the controller board report on status. There are one red, one green and four yellow indicators. Refer to Chapter 6 of this manual and SMN501 to interpret the LED patterns.

3.2 FLOPPY DISK DRIVE OPERATION

Two floppy disk drives, located behind the floppy disk drive access door (see Figure 3-11), store VCP-V microcode and system history data. The top diskette drive is used for microcode and microdiagnostic operations. The bottom drive records system events on a history disk.

The subsections that follow describe diskette insertion, removal, and diskette handling precautions.

3.2.1 INSERTING THE FLOPPY DISK

To insert a floppy disk into a floppy drive, follow these steps:

1. Remove the diskette from the storage envelope.

2. Make sure the drive's locking lever is in the full counter-clockwise position (see Figure 3-11).

3. Insert the diskette into the drive access opening with the label face up and the write protect notch on your left.

4. Push in the floppy disk until it meets firm resistance.

5. Lock the diskette into the disk drive unit by turning the media locking lever clockwise.

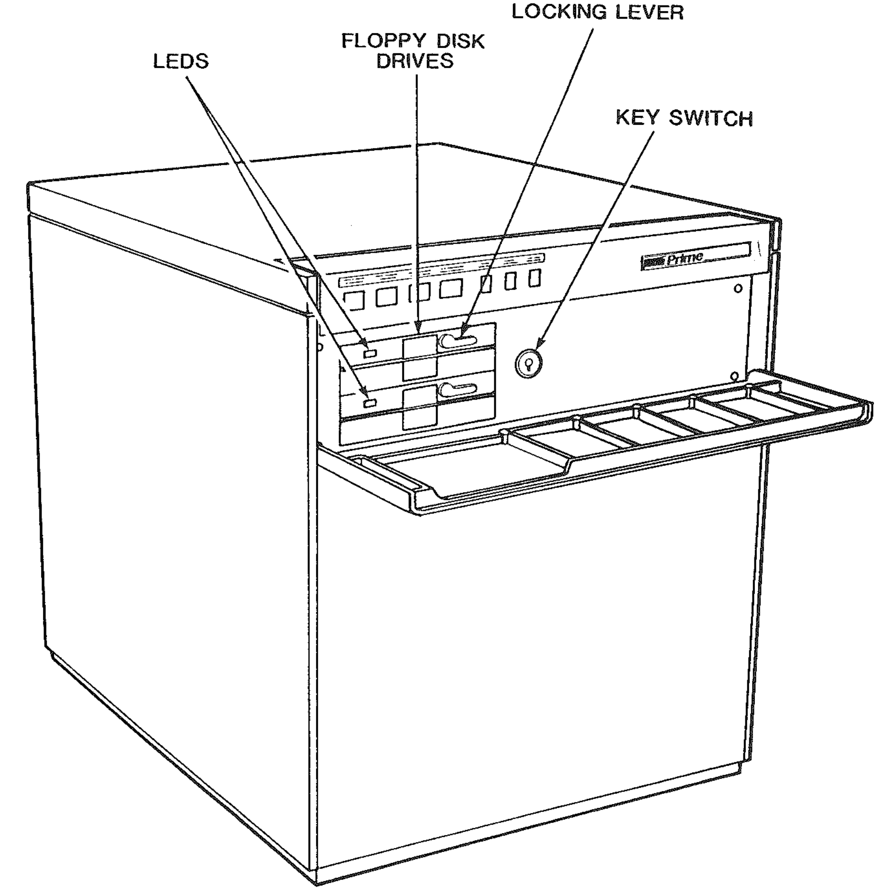


FIGURE 3-11: FLOPPY DISK DRIVES

3.2.2 REMOVING THE FLOPPY DISK

To remove the floppy disk, follow these steps:

1. Turn the media locking lever counterclockwise. The floppy disk can be removed.

2. Store the floppy disk in its envelope to protect the data.

CAUTION

To avoid damage to the floppy disk, never unlock the media locking lever while the LED is lit or blinking.

3.2.3 FLOPPY DISK CARE, HANDLING, AND STORAGE

It is important to handle and store the floppy disk properly to maintain the integrity of the recorded data. A damaged or contaminated floppy can impair or prevent recovery of data and can damage the read/write heads of the disk drive.

When handling disk media, follow these rules:

- Keep the floppy away from magnetic fields.
- Do not touch the precision surface of the floppy with your fingers.
- Carefully insert the floppy into the drive until the floppy meets the backstop.
- Do not bend or fold the floppy.
- Put the floppy into its jacket when it is not being used.
- Store the floppy at temperatures between 10 degrees C and 52 degrees C (50 degrees F and 125 degrees F).

3.3 PRIMENET NODE CONTROLLER OPERATIONS

There are no operating procedures for the PNC. The PNC is operating when the system is powered up. If any problems occur, refer to Chapter 6 for troubleshooting procedures.

PRIMENET software must be installed for the PNC to function under PRIMOS. For full PNC-II functionality, PRIMOS 20.1 or later is required.

NOTE

On pre-20.1 revisions of PRIMOS, the PNC-II emulates the old PNC.

For the system to become an active node in the ring it must be configured and initialized. See the Network Planning and Administration Guide (DOC7532-2PA) for information on the following utilities:

- CONFIG_NET
- START_NET

3.4 INTELLIGENT COMMUNICATIONS SUBSYSTEM 3 (ICS3) OPERATIONS

The available protocols and subsystem responses of ICS3 operation under PRIMOS depend on the PRIMOS revision level used.

The communication software packages supported and the configuration procedures for the ICS3 subsystem are provided in Intelligent Communications Subsystems (ICS) Service Manual (SMN250).

3.5 SYSTEM POWER-UP AND AUTOBOOT TO PRIMOS

To power up the system and perform an autoboot to PRIMOS, follow these steps:

1. Verify that the ac cable is connected from the system PDU connector to the external ac power source (see Figure 3-2).

2. Flip the PDU circuit breaker to the ON (LEFT) position. Verify that the PDU power indicator light is ON.

3. Check for the proper installation of the system terminal to the bulkhead panel (refer to Chapter 2, System Terminal Installation). Check that the system terminal baud rate matches the baud rate of the VCP-V LOCAL1 port.

4. Press the ON/INITIATE SHUTDOWN control on the control panel (see Figure 3-1). The ON and MASTER CLEAR indicators illuminate. After the VCP-V software is loaded, the REMOTE ENABLE and REMOTE PRIVILEGE indicators also illuminate. When the VCP-V and CPU verification is complete only the ON and MASTER CLEAR indicators remain illuminated. When the system successfully loads and begins running the boot routine, the PROC RUNNING indicator illuminates.

   If no errors occur, the message sequence shown in Figure 3-12 is displayed on the system terminal:

```
DPM000: Diagnostic Processor beginning self verification.
DPM020: Sequencing PDU.  Please wait.
DPM001: Diagnostic Processor self verification completed.
        16 Dec 87 14:51:16 Wednesday

DPM350: Loading Configuration Table <n>
DPM021: System power supplies and PDU being tested, please wait.


        Microdiagnostics and Control Program,
        Copyright Prime Computer, 1987.
        All Rights Reserved.

        Proprietary software of Prime Computer Inc.,
        provided under license for use only on a single CPU.
        Except as provided under such license this software
        may not be transferred, disclosed to third parties
        or copied in whole or in part.

DPM800: Sizing Control Store RAM
DPM803: 16K Control Store available
DPM807: Beginning control store address verification
DPM808: Verification completed.
DPM002: Beginning Central Processor verification, please wait.
DPM003: 'SYSV1' successfully completed.
DPM003: 'SYSV2' successfully completed.
DPM003: 'SYSV3' successfully completed.
DPM003: 'SYSV4' successfully completed.
DPM003: 'SYSV5' successfully completed.
DPM003: 'SYSV6' successfully completed.
DPM004: Central Processor system verified
        16 Dec 87 14:56:20 Wednesday

DPM005: Beginning Central Processor system
         Initialization, please wait
DPM006: Central Processor system initialization completed
        16 DEC 87 14:57:23 Wednesday

DMP007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) 1987, Prime Computer, Inc.]

BOOTING FROM 001060 PRIRUN>PRIRUN.SAVE

CONFIG -DATA CONFIG

Coldstarting PRIMOS, Please wait.

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987
...
...
...
```

FIGURE 3-12: POWER-UP MESSAGE SEQUENCE

NOTE

When an error occurs during an AUTOBOOT sequence, the VCP-V processor immediately enters CP mode after it displays the error code. If an error occurs refer to Troubleshooting System Verification and Initialization Failures or to Troubleshooting Boot and Coldstart Failures in Chapter 6 of this manual.

3.6 SYSTEM POWER-DOWN

To power down the system, follow these steps:

1. Notify all users that the system is being shut-down. Set MAXUSR to 0 to prevent additional users from logging in.

2. Press the write protect button on all disk drives and power down all peripheral devices.

3. Use the STATUS USERS command to verify that all terminal users are logged out and all subsystems are shut down.

4. Shut down PRIMOS with the SHUTDN ALL command.

5. Press the ON/INITIATE SHUTDOWN switch.

6. When the VCP-V detects that ON/INITIATE SHUTDOWN has been pressed, it flashes the ON LED, sends a sensor check to the CPU and PRIMOS, and displays the following message on the system console:

   WRN401: Diagnostic Processor detects Soft Shutdown request.

   23 Jan 86 14:01:58 Thursday

7. The PDU shuts down power to the system power supply as directed by the VCP-V.

8. Throw the PDU circuit breaker to the OFF (RIGHT) position, then disconnect the ac power cord from the PDU and the power source.

3.7 TERMINAL PORTS OPERATION

Four RS-232 serial ports are provided on the VCP-V:

- Local 1 Terminal Port (J2) - supports the System Console function.

- Local 2 Terminal Port (J3)- supports the System Console function.

- Spare Terminal Port (J7) - provides an extra port for various system functions and diagnostics.

- Remote Terminal Port (J4) - provides remote access to the system console through a modem.

The operation of each port is presented in the following subsections.

3.7.1 LOCAL 1 TERMINAL PORT

The Local 1 terminal port is connected to the system console. The system console is used to bring the operating system up and down, to modify system configurations, and to provide the operator interface to the VCP-V. When the VCP-V is powered on or reset, the Local 1 terminal is automatically privileged.

3.7.2 LOCAL 2 TERMINAL PORT

The Local 2 terminal port is used as a system console, with a terminal located away from the system.

3.7.3 SPARE TERMINAL PORT

The Spare Terminal Port is for Engineering use.

3.7.4 REMOTE TERMINAL PORT

The remote port is a full Post, Telegraph and Telephone (PTT) compliant RS-232 port, and supports almost any type of modem. To use the remote port, depress the status panel switch, REMOTE ENABLE. When the VCP-V detects the remote terminal connection, it prompts the remote user for the remote password. The prompt appears as follows:

    DPM202: Please enter remote password:

This password is set by using the PASSWORD command from the Local 1 terminal (refer to PASSWORD command in CP Mode Commands in this chapter). The password is retained by the VCP-V when the system is powered down. The default password is a null (or carriage return). If the incorrect password is entered the VCP-V displays:

    ERR205: Incorrect password entered.

If the correct password is not entered after three tries or 40 seconds, the VCP-V drops the Data Terminal Ready (DTR) line to disconnect the remote terminal, and prints the following message:

    DPM908: No response for password from requested port.

When the correct password is entered, the operator is able to monitor VCP-V commands from the remote terminal connected to the remote port.

The status panel switch REMOTE PRIVILEGE must be pressed in order for the remote operator to have the ability to execute commands that would change the state of the system. The prompt CP*> indicates that the remote port is privileged. Any commands typed on the system console terminal once the remote port is privileged, are bracketed by angle brackets and are not executed.

NOTE

> If commands are typed from a non-privileged remote terminal, the commands are echoed back in angled brackets and are not executed.

3.8 VCP-V OPERATION

The VCP-V controls basic system operations, such as AUTOBOOT and power sequencing, and monitors system power supplies and optional Memory Battery Backup Unit.

The following operating modes are available on the VCP-V processor:

- Control Panel (CP)
- System Terminal (ST)
- User (USER)
- Processor Diagnostic Aid (PDA)

Each mode is explained in the following sections.

3.8.1 CONTROL PANEL MODE

In Control Panel (CP) mode, the VCP-V Processor acts as the system control panel and provides the following control panel functions:

- Bootstraps PRIMOS and Standalone Programs
- Displays or modifies CPU Registers and Memory Locations
- Displays system status information
- Enables or disables system terminal ports
- Loads and executes CPU control store

The following subsections explain:

- Entering CP Mode
- Exiting CP Mode
- Control Panel Mode Commands

3.8.1.1 Entering CP Mode

Enter CP mode in one of the following ways:

- Enter a CONTROL-P at the system console to interrupt the AUTOBOOT to PRIMOS sequence at any point after LOAD THE SYSVERIFY MICROCODE FILE.

or

- Press the ESCAPE key twice after the AUTOBOOT to PRIMOS sequence has completed or during System Terminal mode.

CP mode displays one of the following prompts:

- A CP1> prompt is displayed if the LOCAL1 system terminal port is privileged.

NOTE

During Power-up or Reset, the LOCAL1 system terminal port is privileged.

- A CP2> prompt is displayed if the LOCAL2 system terminal port is privileged.

- A CP*> prompt is displayed if the REMOTE system terminal port is privileged.

The prompt indicates that CP mode is entered and the VCP-V Processor is ready to accept CP input commands.

3.8.1.2 Exiting CP Mode

To exit CP mode, enter any of the following commands at the system console:

- MO ST - Enters System Terminal (ST) mode from CP mode.

- MO USER - Enters User (USER) mode from CP mode.

3.8.1.3 Control Panel Mode Commands

The VCP-V uses most CP mode operator commands available under previous VCP processors, as well as a number of new commands.

The CP mode command format may or may not include one or more arguments (specifiers). Arguments are used to specify display mode, device selection and CPU direction.

The display mode arguments are:

- :O (octal)

- :H (hexadecimal)

- :B (binary)

- :D (decimal)

- :A (ASCII)

New specifiers for device selection are:

- :0, :1, :2, :3, :4 (Device Selection --select Floppy 0 or 1)

Up to four arguments can be grouped together at a time in any order, except for display mode specifiers. If two display mode specifiers are used, as in <:B, :H>, the first specifier refers to data display and the second specifier refers to the address display. The default display mode for both address and data is octal. These indicators are also valid to use with DUMP and ACCESS commands. Note, however, that the address mode indication does not take effect until the next command.

For example, the following command is given to perform an ASCII dump from the locations '1000 to '1010 in the current address mode:

D 1000 1010 :A :O

NOTE

The address can be designated in octal, hexadecimal, decimal, or binary. ASCII format is invalid for address displays. The default is :O :O.

VCP-V commands are used for the following purposes:

- CP Operations
- Microdiagnostic File Operations
- Memory Display
- Memory Access

These commands are listed and defined in the following subsections.

3.8.1.3.1 CP Operations Commands

New control panel mode commands have been added to the VCP-V to take advantage of new hardware features. The following section describes new and existing CP mode commands and their functions.

- BOOT - Loads PRE-BOOT and LOADER routines into the CPU. Places the VCP-V Processor in AUTO-WARMSTART mode. Is used with UPS system after main ac power is resumed.

- BOOT <number> - Boots from the drive and controller indicated by the octal sense switch <number>. Refer to Sense Switch Settings in this chapter for BOOT sense switch settings.

- BOOTP - Initiates a BOOT to PRIMOS sequence from disk. BOOTP assumes the physical device and sets the 'RUN FILE TREENAME' to that of the PRIMOS coldstart image.

- BOOTT - Initiates a BOOT sequence from tape. BOOTT assumes the physical device to be MT0 and prompts for the 'RUN FILE TREENAME'.

- BREAKON/BREAKOFF - Controls the system console break option that prevents unauthorized users from accessing the system console. If BREAKON is active, the user must enter a password if console power is removed and re-applied while the system is running. If BREAKOFF is active, no password is required. Refer to the PASSWORD and OVERRIDE commands in this subsection for additional information.

- CONFIG <table> - Loads the specified configuration table from the logical device into the VCP-V memory. Information contained in the table indicates to the VCP-V software which sensors and power supplies to monitor and support. The configuration file stored on the logical device can contain up to 16 possible configuration tables. Valid parameters for <table> are 0 to 15. Configuration table 0 is the base configuration table containing support for the base system. The current configuration table loaded in the system is indicated in the STAT command. The tables are listed in Chapter 2.

- DATE - Displays the time and date in the form of the following example:

  16 JAN 87 17:32:15 Friday

  If the time or date is invalid, the following error message is logged on the history disk and terminal

  ERR800: Diagnostic Processor time of day clock not valid.
  Time and date initialized to: 01:01:00 Sunday

- DISABLE :<port #> - Disables the VCP-V system terminal port designated by <port #>. Port numbers 1, 2, and 3 designate the LOCAL1, LOCAL2, and REMOTE ports respectively.

- DISPLAY <address> - Displays contents of <address> when multi-user PRIMOS is running.

- DIR :<:0 - :4> - Displays the directory of the floppy drive or EPROM cartridge designated by the specifier. The VCP-V Processor stores the specified device number. Subsequent commands use the stored device number, unless a new load device is specified. Specifiers are as follows:

  Device 0 = Floppy Drive 0

  Device 1 = Floppy Drive 1

- DISPLAYC <address> - Displays the contents of <address> each time <address> changes. Operates only with multiuser PRIMOS. To end display, enter CONTROL-P.

- ENABLE :<port> [-NOPASS] - Enables the VCP-V system terminal port that is designated by <port #>. Port numbers 1, 2, and 3 designate the LOCAL1, LOCAL2, and REMOTE ports respectively. Once a port is enabled, an operator at a terminal connected to that port can monitor system console activity. When a port is enabled the operator is prompted for a password. If the -NOPASS option is included the password prompt does not display.

- FETCH - Fetches data from the currently set sense and data switches.

- FREQHIGH - Selects the high speed clock crystal in the CPU. The command is intended for internal Prime use only. The command can only be issued from the Local 1 terminal. A special password encoded directly into the VCP-V software is required to select the high speed clock crystal. If the correct password is entered, the VCP-V checks for SYSCLR active (low). The VCP-V can only change the crystal selection while SYSCLR is asserted. Each time a RUN command is issued with the frequency set high, the following message is displayed at the system console and logged in the History Disk:

WRN200: A Run command was issued with the frequency set high.

- FREQNORM - Cancels the FREQHIGH command by setting the clock crystal selection to normal.

- HALT - Same as STOP command. Halts the CPU and enters the CPU microcode in the CP idle loop. When the CPU is halted, the VCP-V displays the following message:

  DPM400: MASTER CPU HALTED AT <address>

  where <address> is the last address in main memory executed. If the CPU does not enter the CP idle loop, use Control-P to return to command level.

- HELP - Displays a list of CP mode commands available on the VCP-V.

- HISTORY - Places the user into the history environment to review and add comments to the history disk (always logical device 1).

  When the HISTORY command is entered, the following prompt displays:

  HST>

  Valid history disk commands are as follows:

E	Go to end of error list and read the last entry
P <n>	Print the next <n> entries (if n is null, print 1)
UP ARROW	Read the previous entry
N (+/-)	Read the entry plus or minus n from the current entry
W	Write into the current entry's comment
F	Format a history disk
Q	Quit from history environment

  Format the history disk with the F subcommand to enable error logging.

  CAUTION

  Formatting a history disk destroys any data previously on the disk.

  The VCP-V logs error messages sequentially. Each error message is stored in a 256-byte sector of the disk. The next available sector is reserved for comments. You must point to the error message before using the W subcommand to enter comments. Comments can be up to 256 characters. To end a comment, enter $ CARRIAGE RETURN (or enter the 257th character).

The history disk can store about 1,200 messages and comments. When the disk becomes full, the VCP-V overwrites the oldest entry.

The following is an example of the HISTORY command:

```
CP1> HISTORY
HST> E
Date written: 01-11-88 12:45:31

ERR350: Diagnostic Processor detects power supply failure.

Comment: 7778 power supply out to lunch.  Replaced
         by customer service 1/11/88.

HST> Q
CP1>
```

If the HISTORY command is entered and the VCP-V fails to detect a valid history disk at logical device 2, the following error message is displayed:

ERR502: Invalid History Disk detected.

If the VCP-V tries to log an error on the history disk and fails, the following message is displayed:

ERR503: History Disk not responding.

- IOSYSOFF - Releases the IOSYSCLR line to the IO regardless of its current state. This command is intended for internal Prime use.

- IOSYSON - Asserts the IOSYSCLR line to the IO regardless of its current state. This command is intended for internal Prime use.

- LDNET [filename] - Searches the logical device for a Decode Net (type D) file of a given name and loads it into the CPU decode net RAM. If a filename is not specified with the command, the VCP-V defaults to the first type D file on the logical device. If the VCP-V fails to find a decode net file during AUTOBOOT or when a LDNET command is executed without specifying a filename, the following message is displayed and logged on the history disk:

  ERR115: Decode Net file not found.

  If the VCP-V cannot find a specified file, the following message is displayed and logged on the history disk:

  ERR118: Decode Net file <filename> not found.

  When the VCP-V finds the file, it checks the type. If the type is not type D, the following message is displayed and logged on the history disk:

ERR119: File <filename> is not a valid Decode Net file.

- LIGHTS - Displays the current octal contents of the data register.

- LIGHTSC - Displays the current octal contents of the data register each time they change. To end display, enter CONTROL-P.

- LISTREV - Lists the processor types, all processor board part numbers, and their minimum revision level. The output is in the following format:

```
Code inserted for processor: <type>
  Part number: xxxx-xxx - Rev <a>
  Part number: xxxx-xxx - Rev <a>
                    o
                    o
                    o
  Part number: xxxx-xxx - Rev <a>
```

- LMEMTST - Performs a control store address test on the system CPU.

  The VCP-V automatically performs the control store address test at system power-up. The test writes a known image into the control store, then reads the image back. The image is based on the address being tested. If a verification error occurs, the following message is displayed, but <u>not</u> logged on the history disk:

```
ERR704: Control store verification error at location.
        Data received:  aaaa bbbb cccc dddd
        Data expected:  eeee ffff gggg hhhh
```

  If no verification errors occur, the following message is displayed:

  DPM808: Verification completed.

  Before executing the test, the VCP-V tries to determine the size of the control store by writing and reading known data to boundary addresses, then correlating correct and faulty data. If no correct data is read, the following message is displayed and logged on the history disk:

  ERR701: Can't determine Control Store size.

- LOADTM <filename> [SS] - Loads a PMA file from the current logical device into main memory after finding the file and checking the file type. The VCP-V then loads the sense switches specified in [SS]. If none are specified, current settings are used. The data mode specifier must be set to octal. The following registers are loaded into the primary CPU: A, B, X, KEYS, and PB. The registers are specified in the nine-byte R-mode vector at the beginning of the PMA file. Following the load, the VCP-V compares the checksum of the PMA file read from the logical device with the expected result stored in the file pointer. If the checksum is incorrect, the following message is displayed and logged in the history disk:

ERR043: Checksum error on file "<filename>".

- MARGIN <:L :H :O :N> [1 - 8] - The margin command alters the output of the 7778 power supplies according to the value of its specifier. The processor can control up to eight power supplies. If no power supply number is specified, the processor assumes that all power supplies are requested. The :H option increases the voltage output by 5% and :L decreases the voltage output by 5%. The :N option returns the output to normal. The :O option shuts the power supply off.

- MO BRIEF - Enters the VCP-V processor into a limited diagnostic message mode. Power-up defaults to this mode.

- MO FULL - Enters the VCP-V Processor into full diagnostic message mode.

- MO PDA [:0 or :1] - Allows the VCP-V to communicate with either the primary CPU's PDA or the secondary CPU's PDA. This command places the VCP-V processor into User Terminal Mode, and connects the system console to the PDA via the spare port. All characters from LOCAL1, LOCAL2 and REMOTE ports are ignored. To return to CP mode, press the ESCAPE key twice.

- MO USER - Places the VCP-V Processor into User Terminal mode. Refer to User Mode in this chapter for operating procedures.

- MO ST - Places the VCP-V Processor into System Terminal mode. Refer to System Mode in this chapter for operating procedures.

- MO TEST - Places the VCP-V into Test mode. Test mode is similar to User Mode. It communicates down the same asynchronous line, but ignores characters received from the CPU. This mode is intended for internal use only. To return to CP mode, press the Escape key twice.

- OVERRIDE [:0 or :1] - Overides internal flags. This command is intended for internal Prime use only. The command is useful with the PASSWORD command to set a new system console password without entering the existing console password (refer to PASSWORD in this subsection). A password is required whenever power is removed from the system console if the BREAKON option is set (refer to BREAKON/BREAKOFF in this subsection). OVERRIDE bypasses the "Enter old password" prompt in the PASSWORD command by setting an internal flag sought by PASSWORD. Use of the OVERRIDE command with the PASSWORD command is illustrated in the following example:

```
CP1> OVERRIDE
CP1> PASSWORD
DPM203: Please enter password: PRIME
CP1>
```

The OVERRIDE command also sets the microcode loaded, microcode running, and decode net loaded flags, regardless of the system's current state. This allows use of the Processor Diagnostic Aid (PDA) to load and unload microcode without interruption by the VCP.

The command also bypasses the Force BCY error handling capabilities of the VCP. An FBCY by the VCP in response to an error destroys information that could be of value during degbug.

- PARTIAL_TAPEDUMP <drive> - (Primos Rev.21 dependent) Instructs the primary CPU to perform a memory dump to magnetic tape. The sense switch setting is changed to reflect the requested tape drive number. Valid entries are drives 0 through 9. The command then executes a SYSCLR, RUN '777, and SYSOUT INT.

NOTE

Do not use Partial Tapedump for troubleshooting. Customer Service requires full tape dumps for problem analysis.

- PRIVILEGE :<port #> - Allows the system terminal connected to the VCP-V port specified by <port #> to have all system terminal privileges. A port must be ENABLED before it can be PRIVILEGED. Only one port can be privileged at any given time.

- PASSWORD - Changes the current password to protect the system from access from other terminals, such as the remote terminal. This password is required whenever a terminal becomes active or breaks. There is no default password.

  This command can only be issued from the LOCAL1 system terminal. When PASSWORD is typed at the terminal and barring an OVERRIDE command (refer to OVERRIDE in this subsection), the VCP-V Diagnostic Processor displays the following message:

  DPM202: Please enter old password:

  If a user enters an incorrect password, the VCP-V returns the following error message and returns to control panel mode:

  DPM205: Incorrect password entered

  If the old password is correct, the VCP-V prompts for a new password:

  DPM203: Please enter password

  It then asks the user to verify the new password:

  DPM204: Verify password entered

  If the password is verified, the VCP-V changes the old password to the new password and stores the new password in non-volatile memory. The password can have a maximum of eight characters. The initial character can not be a number.

- RCP <location> [:0 or :1] - Is identical to the RUN command except the VCP-V processor remains in CP mode. The <location> is a virtual address when the CPU is in segmented mode.

- RUN <address> [:0 or :1] - Deposits <address> into PB and starts the CPU. If the <address> is not supplied, the current value in PB is used. This command automatically puts the VCP-V in ST Mode. The VCP-V keeps track of the last SYSOUT command entered and implicitly issues a SYSOUT (BUFF, INT or IGN) after every RUN command. The default mode is SYSOUT INT. When the RUN is sent to the CPU, the VCP-V checks if the FREQHIGH command has been entered. If the command was entered, the VCP-V logs a warning on the history disk and displays the following message:

  WRN200: A Run command was issued with frequency set high.

- SD <data> - Sets the data switch register to the value of <data>.

- SE -<mmddyy> -<hhnnw> -<D> - Sets and displays the contents of the VCP-V time-of-day clock. The time is retained when system power is disabled. The command's parameters are described below:

  mm = month of year (01 - 12)

  dd = day of month (01 - 31)

  yy = year 19yy (00 - 99)

  hh = hour of day (00 - 23)

  nn = minute of hour (00 - 59)

  w = day of week (1 - 7, 1 = Sunday)

  D = If present, specifies daylight savings time option.

  The automatic daylight savings time option is designed for domestic use only. To update international systems, refer to the daylight savings time procedure specific to that area.

- SS <sense_switch_setting> - Sets the sense switch register to the value of <sense_switch_setting>.

- SSTEP <n> - Single steps the primary CPU <n> locations. The value of <n> is dependent on the data representation. For example, if the data specification is octal, SSTEP 10 steps the primary CPU eight locations.

- STEPU <address> - Steps the primary CPU until the instruction at location <address> is executed.

- STATus <-CLEAR> - The STATus command displays diagnostic processor status information at the system console. The STATus command has a -CLEAR option which is used to reset the Power

Fail Status field values to zero and then print the most current status of the diagnostic process. Figure 3-13 illustrates a sample status display.

```
Diagnostic Processor Status Information

Power Fails
Recoverable: 000     NonRecoverable: 000     Faults: 000

UPS Activity: 000
MBBU Power Supply is in trickle charge.

Terminals
Local 1:  Active     Enabled    Master
Local 2:  Active     Disabled   Slave
Remote:   Inactive   Disabled   Slave

Password Prompt on Terminal break option off

--- More ---

Configuration Table Selection: 002
Device Selected: 0
Data Mode: Octal
Address Mode: Octal

Microcode Loaded: No
Microcode Running: No
Decode Net Loaded: No

System Running: No
```

FIGURE 3-13: SAMPLE STATUS DISPLAY

Status display fields, shown in Figure 3-13, are defined as follows:

- POWER FAIL displays the number of RECOVERABLE power failures (ac glitches or failures that did not affect system operation because an MBBU was used), UNRECOVERABLE power failures (ac failures), and FAULTS (power supply failures). These values are stored in non-volatile memory and are not reset at power-up.

- TERMINAL STATUS displays the current status of the LOCAL1, LOCAL2, and REMOTE system consoles. The Terminal status is modified by using the ENABLE, DISABLE, and PRIVILEGE commands. The REMOTE port is active only after a remote terminal is successfully connected to the system. Ports are ENABLED/DISABLED through the ENABLE and DISABLE commands. Ports are given MASTER/SLAVE status through the PRIVILEGE command.

The next line indicates whether the VCP-V acts on terminal breaks (see BREAKON/BREAKOFF commands).

The --- More --- prompt displays at the end of one screen of information. Type any character to print the second screen of information.

- CONFIGURATION TABLE SELECTION displays the currently loaded configuration table (see CONFIG command).

- DEVICE SELECTED displays the current logical device. Devices 0-3 are floppy disk drives, while device 4 is an EPROM cartridge.

- DATA MODE and ADDRESS MODE provide the current mode specifiers.

The last section indicates CPU status, including the state of the CPU (running or halted), and whether microcode is loaded and running, and whether or not decode net is loaded.

- STOP - Halts the CPU and enters the primary CPU microcode in the CP idle loop. When the CPU is halted, the VCP-V displays the following message:

DPM400: CPU HALTED AT <address>

where <address> is the last address in main memory executed. If the CPU does not enter the CP idle loop, a Control-P returns the operator to command level.

- STORE <data> - Stores the value of <data> at the location specified by the previously set sense and data switches.

- SYSCLR - Performs the same function in the CPU as the MASTER CLEAR switch on the front panel. The CPU hardware is cleared and the microcode begins execution at location 0.

When the SYSCLR command is issued after a system halt, the VCP-V prompts the user with the following:

Really?

To complete the operation, enter YES. To abort the command, type any other characters. The VCP-V displays the following message:

DPM311: Sysclr was not performed.

CAUTION

The SYSCLR command destroys information stored in controllers that may be useful in analyzing a PRIMOS crash. To preserve this information after a system halt, perform a tape dump before issuing a SYSCLR.

The functions that occur following a SYSCLR command depend upon the microcode loaded in the CPU control store at that time. If no microcode is loaded, the VCP-V processor does not SYSCLR and the following message is displayed:

DPM305: Can't SYSCLR unless CPU microcode loaded

Following a SYSCLR, the VCP-V processor expects a response character from the CPU. A valid response includes:

- A response returned from a microdiagnostic routine.
- A response following the system initialization portion of the base instruction set microcode.

If either of these are received, the VCP-V processor completes the operation and returns to CP Mode. If no response or any other character is received, the VCP-V displays the following message and returns to CP Mode:

ERR303: CPU not responding

If an invalid character is received, the VCP-V processor displays the following:

ERR901: Unexpected character received from CPU <char>

The unexpected character <char> is displayed in Hexadecimal.

- SYSOFF [address] [:0 or :1] - Loads the specified address into the selected (0 or 1) CPU microsequencer, then releases the SYSCLR line to the CPU. The default address is '200. The command is intended for internal Prime use.
- SYSON [:0 or :1] - Asserts the SYSCLR line to the selected CPU (0 or 1). The VCP-V ignores any characters received from the CPU. This command is intended for internal Prime use.
- SYSOUT BUFF - Instructs the CPU to buffer the system terminal output while the VCP-V processor is in CP mode. The VCP-V processor remains in CP mode until another SYSCLR or MO ST command is entered, at which point the buffered output is displayed to the terminal. SYSOUT BUFF is also the default mode whenever the MO ST command is used.
- SYSOUT IGN - Instructs the CPU to ignore all system terminal output while the VCP-V processor is in CP mode.
- SYSOUT INT - This command instructs the CPU to interleave the system terminal output with CP mode output at the system console. The VCP-V processor remains in this mode until another SYSOUT is entered.
- TAPEDUMP <unit #> - Instructs the CPU to perform a memory dump to the magnetic tape unit indicated by <unit #>. It does an implied SYSCLR and RUN '776 from tape drive 0 and a RUN '775 for tape drive 1.
- TRACE - Same as SSTEP, but prints each step rather than only the last step.
- TSENS [1...9] [C] - Displays the ambient temperature readings from all or selected environmental sensors. The default is

readings from all sensors listed in the configuration table. Values are in Celsius. If the sensor number is specified in the command line, the VCP-V attempts to display the temperature from that sensor even if the sensor is not listed in the configuration table. To continuously display temperatures from all or selected sensors, include the C parameter. The VCP-V displays a new temperature reading each time a temperature change is detected. To terminate the display, enter CONTROL P.

NOTE

TSENS 3 command, for the analog sensor in the CPU blower, is the only sensor available at this time. It measures the temperature of the incoming air.

CAUTION

Using the C parameter to continuously display sensor temperatures disables the VCP-V's automatic power supply temperature and voltage monitoring safety feature.

Sample TSENS command output follows:

Temperature degrees in Celsius from Sensor n: xxx

- VIRY - Initiates the VCP-V Processor self-test, performs a SYSCLR, and sets the default load device to 0.

- VFNET [filename] - Verifies the decode net. This command searches the logical device for a Decode Net (type D) file of a given name and verifies it against the copy in the CPU. If no filename is specified, the VCP-V defaults to the first type D file on the logical device. If the VCP-V fails to find a decode net file when a LDNET command is executed without specifying a filename, the following message is displayed and logged on the history disk:

  ERR115: Decode Net file not found.

  If the VCP-V cannot find a specified file, the following message is displayed and logged on the history disk:

  ERR118: Decode Net file <filename> not found.

  When the VCP-V finds the file, it checks the type. If the type is not type D, the following message is displayed and logged on the history disk:

  ERR119: File <filename> is not a valid Decode Net file.

  If a discrepancy is found during the comparison, one of the following messages is displayed:

  ERR308: CPU Verification error on Decode Net file "<filename>".

  or

ERR308: CPU Decode Net verification error.

- VPSD - Starts the resident Virtual Prime Symbolic Debugger (VPSD) if one is loaded. It does an implied SYSCLR and RUN '600.

- VSENS [1...8] [C] - Displays the power supply voltages from all or selected power supplies. The default reads all power supplies listed in the configuration table. If the power supply number is specified in the command line, the VCP-V attempts to display the voltage from that power supply even if the supply is not listed in the configuration table. To continuously display voltages from all or selected power supplies, use the C parameter. The VCP-V displays a new voltage reading each time a change is detected. To terminate the display, enter CONTROL P.

CAUTION

Using the C parameter to continuously display power supply voltages disables the VCP-V's automatic power supply temperature and voltage monitoring safety feature.

Sample VSENS command output follows:

Voltage from power supply n: xx.xxxx

- WARMSTART - Does an implicit warmstart sequence of SYSCLR, RUN, RUN.

3.8.1.3.2 Microdiagnostic File Operations Commands

The following commands load and execute microcode files from the floppy disk drive:

- LOADM <filename>[:0 or :1] - Asserts the SYSCLR- line to the CPU, loads the microcode file from the designated load device, verifies the file if the verify flag is set, and returns to CP mode.

  The SYSCLR command must be issued to execute the microcode since LOADM leaves the SYSCLR- line TRUE (LOW). When the microcode successfully loads, the following message displays:

  DPM008: Microdiagnostic file <filename> successfully loaded.

- RUND<filename> - Asserts SYSCLR-, loads the microdiagnostic specified by <filename> from the disk device into Control Store, and releases the SYSCLR- line to execute microdiagnostics. The following message displays:

  DPM009: Diagnostic <filename> beginning execution.

- RUNDC <filename> - Performs the RUND command continuously. The VCP-V restarts the diagnostic execution regardless whether it passed or failed on the previous execution. To interrupt the sequence, enter a CONTROL-P.

- RUNTM <filename> <ss-setting> - Loads the PMA program file into CPU main memory. If the PMA file load is unsuccessful, the command displays the error message and places the VCP-V in CPU mode. If the load is successful, it sets the sense switches with the <SS-Setting> value.

  If the <data-mode-specifier> is not octal, the following message displays before the sense switch registers are set to the <SS-Setting> value:

  WRN004: Mode specifier is not set to Octal.

  After the sense switches are set, it loads the A, B, X, KEYS and PB registers with the values specified in the 9-byte R-mode vector.

- SCOPE - Places a running microdiagnostic into its scope loop. When a microdiagnostic detects a failing test, it sends the test number and possible failing units to the VCP-V, then enters its console code. This allows the VCP-V to communicate with the microcode to perform certain CP commands, such as ACCESS. When the SCOPE command is invoked, the VCP-V sends the microcode the Scope function byte. The microcode exits the console code, and enters its scope loop. The VCP-V then clears the microdiagnostic running flag. SYSCLR to exit the loop.

- VERIFYM <filename>[:0 or:1] - Verifies the contents of the VCP-V processor's microcode memory against the load device copy named in the command.

3.8.1.3.3 Memory Display Commands

Memory display commands display and modify the CPU registers and memory locations. These commands are as follows:

- MO ABS - Sets the VCP-V Processor to reference absolute (physical) memory locations.

- MO MAP - References mapped memory (default) locations.

- MO RFABS - References register file absolute locations.

- MO RFCRS - References register file Current Register Set (CRS) locations.

- MO RFH - Displays or modifies only the high side of a register file.

- MO RFL - Displays or modifies only the low side of a register file.

NOTE

When register file mnemonics are used, both high and low sides display. The high-low mode determines which side is modified by the Access command.

3.8.1.3.4 Memory Access Commands

System memory access commands are as follows:

- A <n>[:0 or :1] - Accesses address <n>. The access memory command displays the contents of the selected CPU's memory location specified by <address>. The address may be followed by data mode specifiers.

- A <registername>[:0 or :1] - The access register command displays the contents of the selected CPU's specific register. The current high/low mode determines which side of the register is modified. The name may be followed by data mode specifiers. The access command may be followed by:

  <CR> - (Carriage Return) Access next location.

  ^ - (Up-arrow) Access previous location.

  <number> - Modify location to value of <number>.

  / - (Slash) Exit and return to CP mode.

- C <start> <end> <to> - Copies the block, beginning at address <start> and ending at address <end>, to the block beginning at address <to>. Overlapping blocks are not allowed.

- D <start> <end>[:0 or :1] - Dumps from address <start> to address <end>. Display specifiers may follow the command. To end long or runaway display, enter CONTROL-P.

- D <registername>[:0 or :1] - Dumps both high and low sides of the specified <registername>. Data specifier may follow the command. To terminate a dump, enter a CONTROL-P.

- F <start> <end> <number> - Fills the block from address <start> to address <end> with the data specified by <number>.

3.8.2 SYSTEM TERMINAL MODE

System Terminal (ST) mode provides the user with standard system console operation and performs all system console functions i.e. brings up PRIMOS, sends messages, logs out users. After the system clears and a BOOT command is issued through the system console, the VCP-V processor enters ST mode and awaits the standard PRIMOS commands. Press ESCAPE ESCAPE to exit ST Mode and enter Control Panel mode.

3.8.3 USER MODE

USER mode allows the system supervisor to use the system console as a normal user terminal. USER mode is available only if Local 1 port is privileged and if a terminal line is connected to the VCP-V spare port.

To enter USER mode from ST mode, press ESCAPE ESCAPE. The CP1> prompt display. Enter the MO USER command, then use the LOGIN command to log in as a regular user.

To exit USER mode, press ESCAPE ESCAPE. The CP1> prompt displays.

3.8.4 PROCESSOR DIAGNOSTIC AID MODE

Processor Diagnostic Aid (PDA) mode is intended for use ONLY by Prime hardware and software specialists or trained personnel.

To enter Processor Diagnostic Aid (PDA) mode from the Control Panel mode, enter the following command:

CP1> MO PDA

To return to CP mode, press ESCAPE ESCAPE.

3.9 INFORMATIONAL MESSAGE SUMMARY

Diagnostic Processor Messages (DPMs) provide information on the current status of the system. They display as part of normal system operation and are self-explanatory. These messages cannot be inhibited by the MO BRIEF command. Table 3-8 lists the DP messages available on the 4050/4150 System.

TABLE 3-8: DIAGNOSTIC PROCESSOR MESSAGE (DPM) SUMMARY

NUMBER	MEANING
DPM000	Diagnostic Processor beginning self verification.
DPM001	Diagnostic Processor self verification completed.
DPM002	Beginning Central Processor system verification, please wait.
DPM003	Diagnostic "<filename>" successfully completed.
DPM004	Central Processor system verified.
DPM005	Beginning Central Processor system initialization, please wait.
DPM006	Central Processor system initialization completed.
DPM007	System booting, please wait.
DPM008	Microcode file "<filename>" successfully loaded.
DPM009	Diagnostic "<filename>" beginning execution.
DPM010	Test # <nnnn> successfully completed.
DPM011	Microcode file "<filename>" successfully verified.
DPM020	Sequencing PDU, please wait.
DPM021	System power supplies and PDU being tested, please wait.
*DPM100	Diagnostic Processor has recovered from a Power Fail.
*DPM101	UPS no longer active. Main Power has resumed.
*DPM102	Diagnostic Processor recovering from a power fail.
DPM200	Local 1 terminal connected.
DPM200	Local 2 terminal connected.
DPM200	Remote terminal connected.
DPM201	Remote terminal disconnected.
DPM202	Please enter old password:
DPM203	Please enter password:
DPM204	Verify new password:

*Logged onto History Disk.

TABLE 3-8: DIAGNOSTIC PROCESSOR MESSAGE (DPM) SUMMARY (CONT.)

NUMBER	MEANING
DPM205	Can only do from the local 1 terminal!
DPM206	No help available.
DPM207	Can't from remote terminal
DPM300	Can't while CPU is running.
DPM301	Can't while the system is locked.
DPM302	Can't unless CPU's microcode is running.
DPM303	Can't unless CPU's Instruction Set microcode is running. running.
DPM304	Can't unless CPU's Decode Net is loaded.
DPM305	Can't SYSCLR unless CPU's microcode loaded.
DPM306	CPU interface verification completed.
DPM307	Can't unless CPU is running.
DPM308	Can't stop secondary CPU.
DPM311	Sysclr was not performed.
DPM312	Can't while Sysclr is active.
DPM350	Loading Configuration Table <n>.
DPM351	Ignoring power supply <n>.
*DPM400	CPU halted at <address> <data>.
DPM500	Battery Backup Unit is in high charge.
DPM501	Battery Backup Unit is in trickle charge.
DPM502	MBBU power supply is in high charge.
DPM503	MBBU power supply is in trickle charge.
DPM510	Voltage in range for power supply <n>.
DPM520	Ambient Temperature in range for Sensor <n>.
*DPM701	Machine Check. DWSTAT = <data> DSWPARITY = <data> DWPPARITY2 = <data> DSWRMA = <data> DWSPB = <data>
*DPM702	Missing Memory Module.
*DPM703	Memory Parity (ECCU).
DPM800	Sizing Control store RAM.
DPM801	4K Control store available.
DPM802	8K Control store available.
DPM803	16K Control store available.
DPM807	Beginning control store address verification.
DPM808	Verification completed.
DPM900	Terminal is already enabled.
DPM901	Terminal is being enabled.
DPM902	Local 1 port is being disabled.
DPM902	Terminal is being disabled.
DPM903	Terminal is already disabled.
DPM904	Not allowed to disable privileged terminal.
DPM905	Terminal is being privileged.
DPM906	Terminal is being privileged.
DPM907	Terminal is not active.
DPM908	No response for password from requested terminal.
DPM909	Terminal is not active.
DPM910	Another terminal must be enabled to disable remote terminal.
DPM911	Terminal is being slaved.

*Logged onto History Disk

3.10 BASIC PRIMOS OPERATIONS

This section describes operating system functions frequently used by Customer Service. Refer to the following subsections for basic PRIMOS operating procedures:

- Sense Switch Settings
- Booting PRIMOS
- PRIMOS Utilities
- Changes to PRIMOS Since Rev. 20
- Changes to PRIMOS at Rev. 21

NOTE

The Model 4050 Computer System requires PRIMOS Revision 20.2.6 or 21.0.2 or greater. The Model 4150 Computer System requires PRIMOS Revision 20.2.5 or 21.0.1 or greater.

3.10.1 SENSE SWITCH SETTINGS

When booting PRIMOS, the operator can customize the boot sequence by setting a series of sense switches following the BOOT command.

The syntax for the BOOT command and switch settings is as follows.

CP1> BOOT XXXYYY ZZZZZZ

In the above example, the value of XXX is used to select options that alter the execution of CPBOOT. See Sense Switch Boot Options in this chapter for more information.

The value of YYY tells CPBOOT what type of device to boot from, disk or tape, the address of the controller it is connected to, and its unit number on that controller. See Boot Device Options in this chapter for more information.

Lastly, the value of ZZZZZZ represents the contents of the Data Switches. This field is optional, and is used primarily to control CPBOOT's built-in diagnostics.

Refer to the following subsections for specific sense switch information:

- Sense Switch Boot Options
- Boot Devices
- Data Switch Boot Options
- Sample Boot Option Words

3.10.1.1 Sense Switch Boot Options

The following boot options are defined at Rev. 20.2.3 and 21.0.2 of PRIMOS. Note that the value YYY represents the Boot Device Option, defined in detail in the next subsection.

'100YYY - Prompts the user for the values of COMDEV, PAGDEV, and NTUSR. Do not initialize the communications controllers (QAMLC, ICS1, ICS2, ICS3, SMLC, or PNC). Do not read the user's PRIMOS.COMI or CONFIG file. If this switch is not set, PRIMOS assumes that it is to use PRIMOS.COMI and CONFIG, and proceeds as usual.

'010YYY - Assumes that the program being booted is on the same device that BOOT was read from. If not set, BOOT prompts for 'Physical DEVICE=' for entry of a valid disk partition's Physical DEVice (PDEV) number, or a magtape unit in the form of MT0, MT1, MT2, ... or MT7.

'004YYY - AutoBoots PRIMOS. Assumes the pathname of the PRIMOS runfile is the same as used in the last successful boot of PRIMOS from this device. If the UFD MFD>BOOT_RUN_FILE_TREENAME does not exist, or does not contain a valid treename, it assumes PRIRUN>PRIMOS.SAVE. If PRIRUN>PRIMOS.SAVE does not exist, or if this switch is not set, BOOT prompts for 'RUN FILE TREENAME= '.

If this sense switch is not set, the user is prompted for the pathname of the file to be booted. Examples are DOS>DOS.SAVE, CMDNC0>MAKE.SAVE, CMDNC0>COPY_DISK.SAVE, and PRIRUN_19>PRIMOS. Entering a carriage return in response to the prompt instructs BOOT to use the default treename, PRIRUN>PRIMOS.SAVE.

'002YYY - Halts immediately after loading the program to be booted, but before starting program execution, to allow the user to patch locations in memory or set sense switches. To execute the program depress the START switch (for Control Panel systems) or enter RUN from VCP mode. Do not SYSCLR before executing the program! This option is useful when running T&Ms. If this option is not set, the program is loaded then executed immediately.

'001YYY - Indicates do not run CPBOOT, or this machine, in Machine Check Mode. This option is useful when troubleshooting a system that is halting due to machine checks. If not set, the system runs with Machine Check Mode turned on.

'000040 - Halts immediately to allow the user to patch the system console baud rate to something other than the default of 300 baud. This option is valid only when booting from Magtape! Other baud rates are selected by patching locations '1004 through '1006.

To continue the boot, press the START switch (on Control Panel system), or enter RUN from VCP mode. Before continuing with the boot, you must set the sense switches back to their original values at the start of the boot.

3.10.1.2 Boot Devices

The Rev. 20.2.3 and 21.0.2 BOOT program allows PRIMOS and standalone programs (MAKE.SAVE, COPY_DISK.SAVE, etc.) to boot from disk drives attached to controller addresses '22 and '23, and from Magtape units other than MT0. Table 3-9 lists the boot devices supported at Rev. 20.2.3 and 21.0.2 of PRIMOS. The value XXX represents the Sense Switch Boot Options described in the previous section.

TABLE 3-9: SENSE SWITCH BOOT DEVICE OPTIONS

OPTION	DEVICE
XXX114	Disk drive 0, disk controller 0 (dev addr '26)
XXX314	Disk drive 1, disk controller 0 (dev addr '26)
XXX514	Disk drive 2, disk controller 0 (dev addr '26)
XXX714	Disk drive 3, disk controller 0 (dev addr '26)
XXX134	Disk drive 0, disk controller 1 (dev addr '27)
XXX334	Disk drive 1, disk controller 1 (dev addr '27)
XXX534	Disk drive 2, disk controller 1 (dev addr '27)
XXX734	Disk drive 3, disk controller 1 (dev addr '27)
XXX154	Disk drive 0, disk controller 2 (dev addr '22)
XXX354	Disk drive 1, disk controller 2 (dev addr '22)
XXX554	Disk drive 2, disk controller 2 (dev addr '22)
XXX754	Disk drive 3, disk controller 2 (dev addr '22)
XXX174	Disk drive 0, disk controller 3 (dev addr '23)
XXX374	Disk drive 1, disk controller 3 (dev addr '23)
XXX574	Disk drive 2, disk controller 3 (dev addr '23)
XXX774	Disk drive 3, disk controller 3 (dev addr '23)
XXX005	Tape drive 0, tape controller 0 (dev addr '14)
XXX205	Tape drive 1, tape controller 0 (dev addr '14)
XXX405	Tape drive 2, tape controller 0 (dev addr '14)
XXX605	Tape drive 3, tape controller 0 (dev addr '14)
XXX025	Tape drive 0, tape controller 1 (dev addr '13)
XXX225	Tape drive 1, tape controller 1 (dev addr '13)
XXX425	Tape drive 2, tape controller 1 (dev addr '13)
XXX625	Tape drive 3, tape controller 1 (dev addr '13)

3.10.1.3 Data Switch Boot Options

The following data switch options are available at PRIMOS Revisions 20.2.3 and 21.0.2 or greater.

'040000 - Forces the system to halt after an error displays with Force Error Display set (Data Switch '004000).

'020000 - Inhibits PIO time outs.

'010000 - Bypasses the CPBOOT diagnostic routines.

'004000 - Forces error display.

'002000 - Displays messages while executing CPBOOT.

'000002 - Boots from a Pre-REV20 tape.

3.10.1.4 Sample Boot Option Words

Table 3-10 lists commonly used boot options.

TABLE 3-10: COMMON BOOT OPTION WORDS

BOOT VALUE	CONTROLLER ADDRESS	DRIVE UNIT	PARTITION WITH BOOT FILE	PRIMOS RUNFILE
14114	'26	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
10114	'26	0	First	Prompts for filename
114	'26	0	Prompts for pdev	Prompts for filename
114114	'26	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE Do not use configuration and startup files.
100114	'26	0	Prompts for pdev	Prompts for filename. Do not use configuration and startup files.
14314	'26	1	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14514	'26	2	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14134	'27	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14154	'22	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14174	'23	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
10005	'14	MT0	-	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE

3.10.2 BOOTING PRIMOS

The following subsections contain examples of booting PRIMOS from disk and tape.

3.10.2.1 Booting PRIMOS from Disk

Refer to the following examples when booting PRIMOS from disk:

NOTE

The PRIMOS revision listed in the following procedures may vary depending on what revision of PRIMOS the system is using.

EXAMPLE 1: Execute the following sequence of commands to boot PRIMOS from physical device 1460:

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88 09:30:00 Wednesday
```

2. Boot to multi-user PRIMOS:

```
CP1> BOOT 114
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]
```

3. Enter the physical device:

```
PHYSICAL DEVICE=1460
```

4. Enter the run file treename:

```
RUN FILE TREENAME=PRIRUN>PRIMOS.SAVE

BOOTING FROM 001460 PRIRUN>PRIMOS.SAVE

CONFIG -DATA CONFIG          /* Specify CONFIG file after -DATA

Coldstarting PRIMOS, Please Wait...

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987
..
..
```

EXAMPLE 2: Set the sense switch boot option to '010 to assume that the program being booted is on the same device that BOOT was read from. Execute the following sequence of commands to boot PRIMOS:

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88 09:30:00 Wednesday
```

2. Boot to multi-user PRIMOS:

```
CP1> BOOT 10114
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]
```

3. Enter the run file treename:

```
RUN FILE TREENAME=PRIRUN>PRIMOS.SAVE

BOOTING FROM 001460 PRIRUN>PRIMOS.SAVE

CONFIG -DATA CONFIG          /* Specify CONFIG file after -DATA

Coldstarting PRIMOS, Please Wait...

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987
..
..
```

EXAMPLE 3: Execute the following sequence of commands to AutoBoot to PRIMOS:

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88 09:30:00 Wednesday
```

2. AutoBoot to multi-user PRIMOS:

```
CP1> BOOT 14114
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]

BOOTING FROM 001460          PRIRUN>PRIMOS.SAVE

CONFIG -DATA CONFIG          /* Specify CONFIG file after -DATA

Coldstarting PRIMOS, Please Wait...

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987
..
..
```

3.10.2.2 Booting PRIMOS from Tape

Refer to the following example when booting PRIMOS from tape mounted at MT0:

NOTE

The PRIMOS revision listed in the following procedure may vary depending on what revision of PRIMOS the system is using.

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88 09:30:00 Wednesday
```

2. Boot from MT0:

```
CP1> BOOT 14005
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]

BOOTING FROM MT0            PRIRUN>PRIMOS.SAVE
```

3. Enter the COMDEV, PAGDEV, and NTUSR:

```
Enter COMmand DEVice: 1460
Enter PAG DEVice: 130460
Enter Number Terminal USeRs: 1

Coldstarting PRIMOS, Please Wait...

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987
..
..
```

3.10.3 PRIMOS UTILITIES

This section summarizes and provides examples for some of the PRIMOS utilities commonly used by Customer Service. These utilities include the following:

- MTRESUME
- BOOT_CREATE
- MAKE.SAVE
- FIX_DISK.SAVE
- COPY_DISK.SAVE
- MAGSAV/MAGRST

NOTE

For a more complete description of these utilities, refer to PRIMOS and Utilities (SSG080).

3.10.3.1 MTRESUME

MTRESUME is a PRIMOS command that runs a .SAVE file from any MAGSAV format magtape. MTRESUME does not run Executable Program Format (EPF) files, which end in .RUN. The utility helps build or recover systems when the necessary software is not present, or when the software cannot be accessed on disk. The following describes the syntax and a list of command options for the MTRESUME command.

MTRESUME MT*n* pathname [-option1] [-optionN]

The unit number for the magnetic tape drive being used for this operation is placed in the *n* position. Command line options for MTRESUME are listed in Table 3-11.

TABLE 3-11: MTRESUME COMMAND LINE OPTIONS

OPTION	DEFINITION
-HELP	Displays help information for the MTRESUME command.
-INDEX	Displays an index of the specified MAGSAV format tape.
-NO_WAIT (-NW)	Does not pause after every page when printing a tape index. A page is defined as 23 lines, unless modified by the -PAGE_LENGTH option.
-PAGE_LENGTH <n> (-PL <n>)	Redefines the page length to <n>, where <n> is a number representing the number of lines in the page. MTRESUME will pause after printing a page of treenames, when indexing a tape. The default is 23 lines.
-LOGICAL_TAPE <n> (-LT <n>)	Specifies the logical tape to search, where <n> is a number representing the logical tape number. The default is 1.
-COMMAND_OPTIONS <options>	Must be the last option on the command line. The option specified are arguments which are passed to the program being invoked by MTRESUME. This option can be abbreviated to -CMDOPT.

3.10.3.2 BOOT CREATE

The BOOT_CREATE utility is used to create boot tapes. Under the system boot sequence implemented at Rev. 20 and greater, the following files and UFDs are required on the boot tape:

- CMDNC0>MAKE.SAVE
- CMDNC0>FIX_DISK.SAVE
- CMDNC0>COPY_DISK.SAVE
- CMDNC0>MAGRST
- CMDNC0>MAGSAV

- DOS>DOS.SAVE
- PRIRUN

The following utilities and directories are recommended on the boot tape:

- SAM.SAVE
- DIAG
- T&MRUN

For more information, refer to the BOOT_CREATE INFO File in the PRIMOS Rev. 20 or 21 Information File.

3.10.3.3 MAKE.SAVE

MAKE.SAVE (formerly MAKE) can be executed in two modes:

- Standalone (booted from disk or tape)
- Under multi-user PRIMOS (command line)

If you run MAKE.SAVE under multi-user PRIMOS, you must first assign the disk partition to be created, then enter any desired options following the MAKE command on the same line.

Disks do not have to be assigned when executing MAKE.SAVE in standalone mode. Enter command options on one line after the "Enter command line options:" prompt.

To run MAKE.SAVE in standalone mode, refer to the following example.

NOTE

The PRIMOS revision listed in the following procedure may vary depending on what revision of PRIMOS the system is running.

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88 09:30:00 Wednesday
```

2. Boot from tape drive MT0:

```
CP1> BOOT 10005
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]
```

3. Enter the run file treename:

```
RUN FILE TREENAME=CMDNC0>MAKE.SAVE

BOOTING FROM MT0      CMDNC0>MAKE.SAVE
```

```
*** MAKE <Rev. 21> ***  Copyright (c) 1986, Prime Computer, Inc.
```

4. Enter the command line options:

```
Enter command line options: -DISK 1460 -PART COMDEV -DT MODEL 4735
-BADLEV 4 -NO INIT -AC

Which file sectoring scheme would you like?
Type "0" (Reverse Sector)
 or  "1" (Forward Sector)
> 0

Making     6 head partition COMDEV
Tracks:               ####
Sectors per track:       #
Partition is using Reverse Sectoring
Partition is in All_Controller Mode
Partition size in decimal records:    #####
Checking for badspots.
Disk Created.

DPM400: CPU halted at 025175: 103775
        10 Feb 88 10:20:00 Wednesday

CP1>
```

For detailed information on the MAKE utility, refer to PRIMOS and Utilities (SSG080).

3.10.3.4 FIX_DISK.SAVE

FIX_DISK.SAVE (formerly FIX_DISK) automatically repairs disk partitions, including hashed directories, and disk partitions in lower revision formats.

A new command line option, -CONVERT_XX, has been added to function under FIX_DISK.SAVE. -CONVERT_20 converts existing disk partitions (Rev. 18 or 19) to Rev. 20 disk partitions. -CONVERT_21 converts existing disk partitions (Rev. 18, 19 or 20) to Rev. 21.

NOTE

FIX_DISK.SAVE cannot be used to install the Rev. 20 or 21 CPBOOT.

The following example shows how to boot PRIMOS from tape and fix the command partition with FIX_DISK.SAVE. The command device was specified as 100000 in this example. This indicates that the command device is null, or empty. Refer to Sense Switch Settings and to MTRESUME in this chapter for additional information.

To use FIX_DISK.SAVE, follow these steps:

NOTE

The PRIMOS revision listed in the following procedure may vary depending on what revision of PRIMOS the system is running.

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88 09:30:00 Wednesday
```

2. Boot:

```
CP1> BOOT 14005
DPM007: System booting, please wait.

BOOTING FROM MT0     PRIRUN>PRIMOS.SAVE
```

3. Enter the COMDEV, PAGDEV, AND NTUSR:

```
Enter COMmand DEVice: 100000
Enter PAGing DEVice:  1460
Enter Number Terminal USeRs: 5

Coldstarting PRIMOS, Please Wait...

PRIMOS 21.0.2 Copyright (c) Prime Computer, Inc. 1987

2048K BYTES MEMORY IN USE

Please enter date and time.
```

4. Enter the date and time:

```
OK, SE -012786 -0930
LOGREC* ufd does not exist. Can't start system event logging.
 (SETIME)
ER!
```

5. Assign the drive:

```
AS MT0
Device MT0 assigned.
```

6. Resume FIX_DISK.SAVE:

```
OK, MTRESUME MT0 FIX_DISK.SAVE -DISK 1460 -COMDEV -FIX
This is a revision 20 MAGSAV tape.
Date:     02-11-87
Revision: 20
Reel:     1
Name:     BOOT
[FIX_DISK Rev. 20.0 Copyright (c) Prime Computer, Inc. 1985]
  02/11/87 09:35
Partition name is COMDEV

The quota system may be incorrect.
This is a revision 20 partition.
BEGIN MFD
..
..
..
```

```
DISKRAT UPDATED!
FIX_DISK finished
OK,
```

For further information on FIX_DISK.SAVE, refer to the FIX_DISK INFO file in the PRIMOS Rev. 20 or 21 Information File.

3.10.3.5 COPY_DISK.SAVE

COPY_DISK.SAVE (formerly COPY_DISK) can run under PRIMOS or standalone. COPY_DISK.SAVE can copy either Rev. 21,20, 19, or 18 format disk partitions. COPY_DISK at Rev. 20.2.3 and 21 functions the same as other versions of PRIMOS.

To run COPY_DISK.SAVE standalone, the new CPBOOT must be given the treename, COPY_DISK, when the run file treename is requested. In standalone mode:

- Disk assignments are not possible
- COPY_DISK asks the operator to enter the command line options
- COPY_DISK halts when it finishes its task

When running COPY_DISK under PRIMOS, assign the disks involved in the copy operation, and enter the command line options on the same line following the COPY_DISK command.

To run COPY_DISK.SAVE, follow these steps:

NOTE

> The PRIMOS revision level listed in the following procedure may vary depending on what revision level of PRIMOS the system is using.

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        10 Feb 88  09:10:40 Wednesday
```

2. Boot:

```
CP1> BOOT 10114
DPM007: System booting, please wait.
```

3. Enter the run file treename:

```
RUN FILE TREENAME=CMDNC0>COPY_DISK.SAVE

BOOTING FROM 001460 CMDNC0>COPY_DISK.SAVE

[COPY_DISK Rev. 20.0 Copyright (c) Prime Computer, Inc. 1985]
Enter command line options:
```

4. Enter the desired options:

```
From phys disk=1460
To phys disk=1462
From, To, Records =  001460, 001462   29628
Parameters OK (yes/no)? YES
Copy started
Badspots handled on partition 001462, please run FIX_DISK

DPM400:  CPU halted at 024147: 103775
         11 Feb 88  09:30:30 Wednesday

CP1>
```

For further information, refer to the COPY_DISK INFO File in the PRIMOS Rev. 20 or 21 Information file.

3.10.3.6 MAGSAV/MAGRST

At Rev. 20 and greater of PRIMOS, MAGSAV has changed in the following ways:

- Prompts for Overwrite or Append.
- Writes a Rev. 20 or greater boot record (MTBOOT) on tape if the -REV19 option is omitted.
- The -CAM_TO_DAM (-CTD) option has been added to convert the type of all contiguous files on tape to DAM files, without affecting the copy on the disk.

At Rev. 20 and greater of PRIMOS, the MAGRST utility has changed as follows:

- Creates a hashed directory for a non-hashed ACL directory saved to tape.
- The -CAM_RBF (-CRBF) option has been added to allow all RBF files to be restored as CAM files.
- The -DAM_RBF (-DRBF) option has been added to allow all RBF files to be restored as DAM files.

Attempting to read a tape created with Rev. 20 (or greater) MAGSAV with Rev. 19 or Rev. 18 MAGRST, generates read errors when reading the first record of the tape if the -REV19 command was not used when the tape was created. The Rev. 19.2.18, 19.3.11. and 19.4.4 patch releases contain versions of MAGRST modified to read tapes written by Rev. 20 MAGSAV (or greater) without the -REV19 option.

The Rev. 20 (or greater) new system boot allows PRIMOS Rev. 20 (or greater), PRIMOS II (DOS) MAKE.SAVE, and COPY_DISK.SAVE to be booted from magtape.

For additional information and MAGSAV/MAGRST examples, refer to <u>PRIMOS and Utilities</u> (SSG080).

3.10.4 CHANGES TO PRIMOS SINCE REVISION 20

The following sections describe the new changes to all levels of PRIMOS since Rev. 20. Included are:

- Startup Messages
- Two halt address messages
- STATUS command line numbers also in decimal
- The -FORCE option of the SHUTDN command.

3.10.4.1 Startup Messages

At Rev. 20.2, one or more new system startup messages will appear on the screen at system startup. The new startup message, which always appears after the CONFIG command is processed as follows:

```
Coldstarting PRIMOS, Please wait ...
```

Other new messages concern the initialization of the attributes of User 1 (SYSTEM). At coldstart, PRIMOS reads profile information in the SAD and uses it to initialize attributes for the user SYSTEM. If you do not make an entry in the SAD for USER1, PRIMOS uses the system defaults for the profile. If the SAD does not exist, if an entry for the system is not present, or if the project is invalid, one or both of the following messages will appear.

```
Can't attach to SAD: Not found (nlogin)

Profile data cannot be initialized from the SAD for the
supervisor. System defaults are being used.
```

For a detailed list of PRIMOS coldstart error messages, see the System Administrator's Guide, Part Number DOC5037-3LA.

3.10.4.2 Halt Messages

The PRIMOS halt mechanism has changed. It now displays two halt addresses instead of one, and is referred to as a "slow halt". The slow halt allows the CPU DMX transfers and the last disk write operation to complete, before stopping the CPU. This means that there won't be any partially written disk records, although the physical and logical organization of the disk is not guaranteed.

The slow halt replaces HLT in several software halt locations. Refer to Troubleshooting System Halts in Chapter 6 of this manual for a list of common PRIMOS halts. At revisions previous to REV. 20.2 most CPUs display the following message at halt time:

```
CPU halted at XXXXXX/XXXXXX
```

When Rev 20.2 PRIMOS halts, the "CPU halted at" message is preceded by the following message:

```
PRIMOS halted at XXXXXX/XXXXXX
```

The following example illustrates the two halt messages:

```
OK, SHUTDN ALL
REALLY? YES
WAIT,
PRIMOS NOT IN OPERATION

PRIMOS HALTED AT 000006/040660: 005003

DPM400: CPU halted at 000006/040660: 005011
        28 Jul 86 11:39:40 Monday

CP1>
```

The "PRIMOS HALTED AT" message is the location in memory where PRIMOS encountered the halt instruction.

The "CPU halted at" message displays the segment and word number where the halt actually occurred.

3.10.4.3 Status Command

At Rev. 20.2, the STATUS command shows the asynchronous line number of a terminal user in decimal as well as in octal.

3.10.4.4 SHUTDN -FORCE Option

Prior to Rev. 20.1, partitions on a malfunctioning disk drive could be shut down only by shutting down the entire system with the SHUTDN ALL command. At Rev. 20.1 and greater, the -FORCE option for the SHUTDN command enables PRIMOS to shut down any or all partitions on a particular disk drive under any circumstance. The -FORCE option is used with all other SHUTDN options, except -RENAMES.

The format for using -FORCE is as follows:

SHUTDN ALL [-FORCE]

The ALL option shuts down all partitions on the local system and disconnects remote partitions from the system. Use ALL for a normal shutdown of PRIMOS.

When the -FORCE option is used, PRIMOS attempts an orderly shutdown. If an orderly shutdown is not possible, PRIMOS continues with the shutdown and reports any problems to the system terminal. The integrity of the file system cannot be guaranteed if an orderly shutdown does not take place. In that case, it may be necessary to run FIX_DISK.

The format to shut down one or more local disk partitions is:

SHUTDN pdev-1 [...pdev-9] -FORCE

The above format for -FORCE shuts down from one to nine malfunctioning partitions, pdev-1 through pdev-9. If the partitions are on a remote system, use the -ON option and specify the remote system's name as nodename. The remote partitions are disconnected from your local system, but are not shut down at the remote system.

For more information, refer to System Operator's Guide (DOC5047-3LA).

3.10.5 CHANGES TO PRIMOS AT REV. 21

This section describes a few of the changes at PRIMOS Revision 21 that are readily visible to the CSR.

Included in this section are the following:

- Coldstarting the System
- Partial Tape Dump
- New PRIMOS Commands
- Physical Device Numbers

3.10.5.1 Coldstarting the System

Coldstarting procedures include three new directives:

- SYSNAM
- SET_TIME_INFO
- TPDUMP

When installing a system, you must supply a system name by putting the SYSNAM directive in the CONFIG file. If the SYSNAM directive is missing or incorrect, PRIMOS will prompt you to enter one at the system console. Coldstart will not complete until the system name has been set. The system name should consist of 1 to 6 characters, beginning with a letter, and must not contain any special characters. Once the system name has been set, it cannot be changed except by a coldstart.

The SET_TIME_INFO command establishes time information for the local time zone and whether or not daylight savings is in effect. This information is used to calculate the Universal Time. The SET_TIME_INFO command should be issued before the SETIME at coldstart, and ideally, should be part of the PRIMOS.COMI file.

NOTE

> The system will not prompt for this command, and coldstart will not complete if the command is missing.

The TPDUMP Config directive tells PRIMOS to stop for a crash dump before performing the Forced Shutdown. The default for this config directive (if not specified in the CONFIG file), is Not to stop for a crash dump. Therefore, TPDUMP should be specified in the CONFIG file.

3.10.5.2 Partial Tape Dump

Because physical memory is getting larger, tape dumps can take a long time. It is possible to get a partial tape dump by using the VCP command RUN 777, and SYSOUT INT. However, it is a Customer Service policy to <u>always</u> take a FULL crash tape dump for serious problems.

3.10.5.3 New PRIMOS Commands

Several new features have been added to PRIMOS at Revision 21. Table 3-12 summarizes the commands necessary to invoke the new PRIMOS features. Refer to <u>PRIMOS and Utilities</u> (SSG080) for details.

TABLE 3-12: NEW PRIMOS REVISION 21 COMMANDS

COMMAND	FUNCTION
SET_TIME_INFO	Sets local time and daylight savings time if applicable for the local system.
START_DSM	Starts up Distributed System Management.
START_LSR	Starts up the login server.
START_NET	Starts up PRIMENET.
START_NTS	Starts terminal activity for the Prime host node on the network.
STOP_LSR	Shuts down the login server.
STOP_NET	Shuts down PRIMENET.
CONVERT_TO_ACLS	Converts any existing password directories to ACL directories.
DUMP_SEGMENT	Specifies the segments to be written to tape during a partial tape dump.
DUMP_USER	Specifies which users are to have their segments written to tape during a partial tape dump.
PASSWORD_DIRS	Prevents the creation of password directories by users when invoked with the -OFF option by the System Administrator.
PRATIO	Allows the operator to change the paging ratios of the paging partitions currently installed on the system.

TABLE 3-12: NEW PRIMOS REVISION 21 COMMANDS (CONT.)

COMMAND	FUNCTION
RESET_DUMP	Resets the parameters of a partial dump to the default values.
SET_DEVICE_ACCESS	Sets ACLS on specific devices on the system.
SET_ASYNC	Configures an asynchronous line connected to a controller.
TRANSFER-LOG	Invokes a program that backs up and moves audit trail files.
DISPLAY_LOG	Displays all or part of a system or network log event at your terminal, or writes it to a disk.
LIST_DUMP	Displays the current parameters specified for a partial tape dump.
PRINT_SECURITY_LOG	Invokes the security audit report utility which enables the System Administrator to examine the contents of an audit trail file.
MIRROR_OFF	Removes a partition from a mirrored pair.
MIRROR_ON	Creates a mirrored pair.
STOP_NTS	Shuts down network terminal service activity on the local system.

3.10.5.4 Physical Device Numbers

The binary breakdown of physical device numbers (PDEVS) has changed at Rev. 21. The numbers in the PDEV tables for SMDs and FMDs are computed for controller 0 (controller address '24) at Rev. 21 of PRIMOS. Previous revisions of PRIMOS used controller 1 (controller address '26).

Refer to PRIMOS and Utilities (SSG080) or to Chapter 3 of Operator's Guide to File System Maintenance (DOC9300-3LA) for additional information on physical device numbers.

3.11 DISTRIBUTED SYSTEM MANAGEMENT (DSM) OPERATIONS

The new PRIMOS Distributed System Management (DSM) utility handles event logging and system management at REV. 21.0 and greater. To use DSM event logging, DSM must be installed. The command START_DSM activates the logging of both system and network events. The STOP_DSM command turns off the logging.

DSM startup, operational, and shutdown commands are described in the subsections that follow. For more DSM information, refer to Chapter

5, Preventive Maintenance, in this manual, or to DSM User's Guide (DOC10061-1LA).

3.11.1 START_DSM

START_DSM is normally included in the system startup file, PRIMOS.COMI, but can be issued at any time, from the system console. In PRIMOS.COMI, the START_DSM command should come after the CONFIG, ADDISK, and MSG-OBJ directives, and before the START_NET and BOOT_CONTROLLER commands. The format of the START_DSM command is:

```
START_DSM [options]
```

Table 3-13 lists and describes START_DSM options.

TABLE 3-13: START_DSM COMMAND OPTIONS

OPTION	DESCRIPTION
-HELP [-NO_WAIT] [-NW]	Provides information on how to use the command and its options. If you specify -NO_WAIT, the display will not paginate at your terminal.
-MULTI_NODE	Allows administrator to specify whether DSM on your system is to be networked. If you do not specify -MULTI_NODE, the ISC network server is not started, and DSM will run as a non-networked product.
-USAGE	Provides a brief example of the command syntax.

3.11.2 DSM OPERATIONS COMMANDS

Table 3-14 lists some of the DSM commands available to the user when DSM has been activated with START_DSM.

TABLE 3-14: DSM COMMANDS

COMMAND	FUNCTION
ADMIN_LOG	Enables System Administrator to create and administer DSM logs.
CONFIG_DSM	Sets up the DSM configuration file.
CONFIG_UM	Defines unsolicited message handling selections on local or remote nodes.
DISTRIBUTE_DSM	Copies the DSM configuration file to all the nodes in the configuration group.

TABLE 3-14: DSM COMMANDS (CONT.)

COMMAND	FUNCTION
LIST-ASSIGNED_DEVICES	Displays all devices that have been assigned on a system with the ASSIGN command.
LIST_ASYNC	Displays the status and configuration of any or all of the system's asynchronous lines.
LIST_COMM_CONTROLLERS	Displays information on communications controllers present in a system, including the LAN Host Controller (LHC), but excluding the Prime Node Controller.

3.11.3 STOP_DSM

STOP_DSM shuts down the Distributed System Management at a node by logging out all the DSM server processes. This command may be issued only from the supervisor terminal. The command format is:

```
STOP_DSM [options]
```

Table 3-15 lists and describes the options for the STOP_DSM command.

TABLE 3-15: STOP_DSM OPTIONS

OPTION	DESCRIPTION
-HELP [-NO_WAIT] [-NW]	Provides information on how to use the command. Overrides other options. If you specify -NO_WAIT, the display is not paginated at your terminal. The same information is available through PRIMOS HELP.

When you issue the STOP_DSM command, the following message displays at the system console:

```
DSM shutdown is in progress
```

Remember that STOP_DSM abruptly terminates all active DSM sessions.

CHAPTER 4
PRINCIPLES OF OPERATION

This chapter provides a detailed functional description of the following Model 4050/4150 system components:

- Central Processing Unit
- Major System Buses
- Memory Subsystem
- I/O Controllers
- VCP-V Diagnostic Processor
- Power Distribution Unit
- TLA10113 Power Supplies
- Floppy Disk Drives
- Cooling System
- Uninterruptible Power Supply
- Distributed System Management (DSM)

Figure 4-1 provides a major functional block diagram of the Model 4050/4150 system.

4.1 CENTRAL PROCESSING UNIT

Model 4050/4150 computers use a TTL-based Central Processing Unit (CPU) based on the 9950 pipeline. The three-board central processors consist of an IS Board, a CMI Board, and an E Board. Figure 4-2 is a major functional block diagram of the Model 4050/4150 central processing units. A functional description of the Model 4050/4150 CPUs is provided in the following subsections:

- Processor Overview
- IS Board Functions
- E Board Functions
- CMI Board Functions
- VLSI Requirements

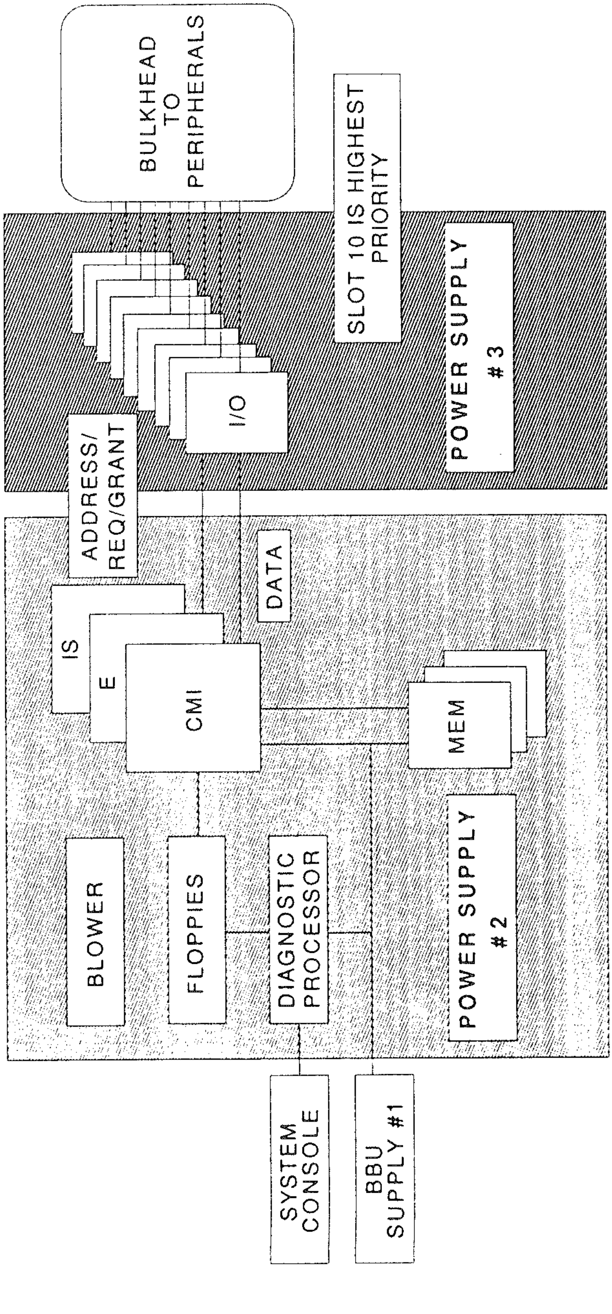
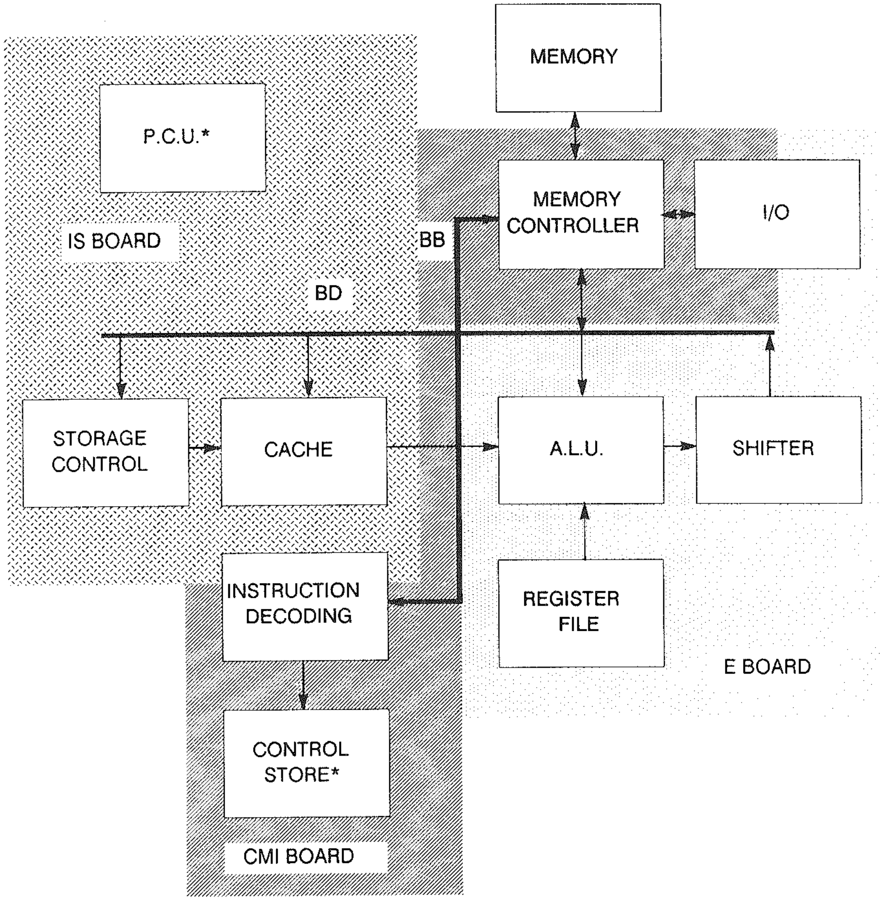


FIGURE 4-1: MODEL 4050/4150 SYSTEM BLOCK DIAGRAM



* THE C.S. AND P.C.U. GENERATE CONTROLS TO ALMOST ALL UNITS. SEVERAL UNITS RETURN CONTROL TO THE C.S. AND P.C.U. TO AFFECT FUTURE CONTROLS.

FIGURE 4-2: MODEL 4050/4150 CPU BLOCK DIAGRAM

4.1.1 PROCESSOR OVERVIEW

The Model 4050/4150 is implemented on three 16-inch by 17-inch boards. It uses AS and ALS MSI components, CMOS static RAMs with TTL-compatible I/O, Motorola MCA2800ALS Macrocell arrays (ECL internal, TTL external VLSI), and high speed PALs and PROMs. Table 4-1 provides a brief overview of the CPU boards and their major functional components.

TABLE 4-1: 4050/4150 CPU FUNCTIONAL OVERVIEW

CPU BOARD	MAJOR FUNCTIONAL COMPONENT	MAJOR FUNCTION
IS	Pipeline Control Unit	Generates stage clocks and controls the ten-stage pipeline.
	Instruction Unit	Decodes instructions, forms effective addresses and handles register file collisions.
	Storage Management Unit	Provides storage for cache, branch cache and STLB and contains logic for storage addressing.
CMI	Control Store Unit	Buffers system microcode.
	Memory Controller Unit	Interfaces memory with the CPU.
	I/O Data Interface	Provides data transfer capability to or from memory.
E	Execution Unit	Reads/manipulates data from A & B buses using ALUs; contains register file; loads data into appropriate registers.
	I/O Addressing Interface	Notifies CPU of type of I/O transfer and supplies target or source address of the data; determines which controller requires service.
	Timers	Track processes and wall clock time.
	BD Control	Controls principal inter-board bus (BD) and contains bus arbitration logic.

4.1.2 IS BOARD

The Model 4050/4150 IS Board contains the Pipeline Control Unit (PCU), cache, the Segment Translation Lookaside Buffer (STLB), the branch cache, and all effective address formation hardware. The board is the functional equivalent of the I and S boards in the 9950. Figure 4-3 is a functional diagram of the IS board. An IS board functional description is provided in the following subsections:

- Pipeline Control Unit
- Instruction Unit
- Storage Management Unit

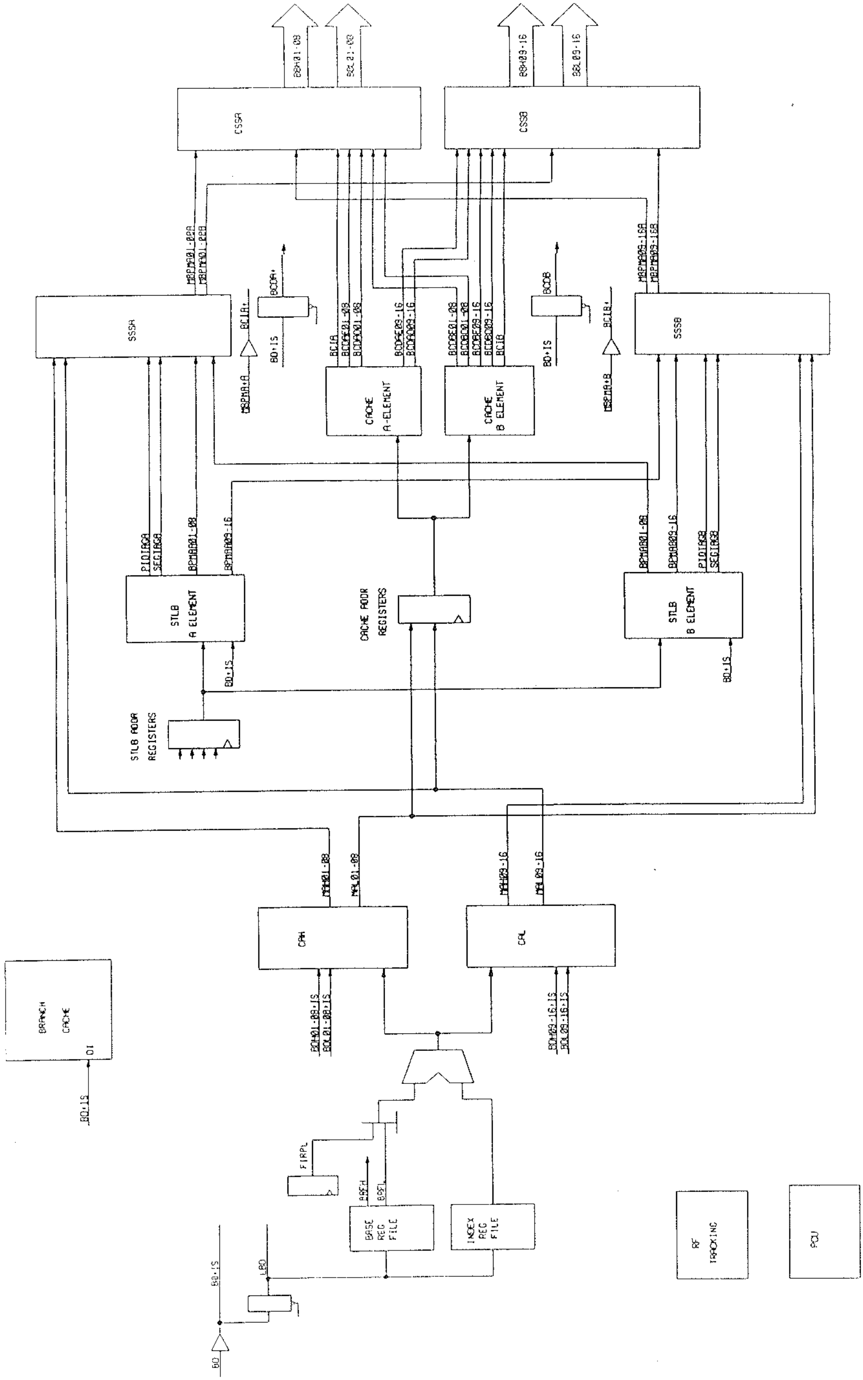


FIGURE 4-3: IS BOARD BLOCK DIAGRAM

4.1.2.1 Pipeline Control Unit

The Model 4050/4150 CPU uses a 10-stage synchronous pipeline capable of handling up to five machine level instructions simultaneously. This section provides the following Pipeline Control Unit (PCU) information:

- Pipeline Functions
- Stage Clock Generation

4.1.2.1.1 Pipeline Functions

The primary functions of each stage in the 4050/4150 pipeline are as follows:

STAGE 1 - Loads the program counter (IRP) into registers addressing cache, STLB, and branch cache.

STAGE 2 - Accesses and loads instruction data into cache data registers. Accesses the STLB and branch cache for possible use.

STAGE 3 - Transfers instruction opcode to the control store (CS) and begins decoding the instruction.

STAGE 4 - Accesses the base and index registers in the instruction (I) unit for required effective address formation. Calculates the decode net entry in control store.

STAGE 5 - Calculates effective address in I unit. Generates control store address.

STAGE 6 - Loads effective address into STLB and cache address registers. Loads microode word into RCM registers on all boards.

STAGE 7 - Accesses and loads operand data into cache data registers. Accesses STLB for possible use. Loads register file source address into execution (E) unit.

STAGE 8 - Begins execution of operation in E unit.

STAGE 9 - Completes execution of operation. Loads register file destination address into E unit.

STAGE 10 - Writes results to register file.

4.1.2.1.2 Stage Clock Generation

The time for each stage to complete its operation is called one "beat." The PCU controls the stages that are clocked in any given beat by enabling clock generation circuits on all processor boards, which in turn generate an associated clock pulse on the subsequent beat.

4.1.2.2 Instruction Unit

The Instruction Unit performs instruction decode and effective address formation during pipeline stages 3, 4, 5, and 6. The I unit also handles register file collisions in the pipeline. These functions are described in the paragraphs that follow.

4.1.2.2.1 Instruction Decoding

Instruction information is read from cache and clocked in Cache Set Select (PCSS) during stage 2. The PCSS transfers the instruction information on the B bus (BB) to the I unit for instruction decoding during stages 3 and 4. The PCSS provides the staging and steering logic to format instruction opcodes and displacements for decode and effective address formation.

The decode net, located in the Control Store (CS) Unit on the CMI Board, consists of a 20-bit-wide lookup table and supporting logic to convert opcodes into addresses for the microsequencer. The lookup table contains microcode entry points and additional control information used internally on the I unit.

4.1.2.2.2 Effective Address Formation

Effective address formation occurs between stage 4 and stage 6. The opcode bits pass through logic that forms the read address of the base and index register files.

The upper 16 bits of the effective address are formed by the contents of the high side of the base register or by the program counter for RP relative operations. The lower 16 bits of the address are formed by taking the contents of the base register or program counter and feeding it through an index Arithmetic Logic Unit (ALU) and a displacement ALU.

4.1.2.2.3 Register File Collisions

A register file collision occurs during pipeline processing when an instruction requires a value in the register file that the current instruction has not finished calculating.

Logic on the I unit detects such collisions and notifies the PCU. The PCU prevents stages 5 and 6 from executing until the execution unit has finished updating the register file.

4.1.2.3 Storage Management Unit

The Storage Managment (S) unit contains the cache storage, branch cache storage, and Segment Table Lookaside Buffer (STLB) storage functional blocks. The S unit also contains logic to address these storage devices. S unit functions are described in the following subsections:

- Cache Logic
- Cache Addressing

- Branch Cache Operations
- Segment Table Lookaside Buffer (STLB)
- Memory Traps

4.1.2.3.1 Cache Logic

The Model 4050/4150 contains a two way associative, virtual instruction and data cache. Each set has a capacity of 64Kb, organized in a 16K X 32-bit arrangement, for a total cache capacity of 128Kb. Cache access time is one beat, so cache hits are possible every beat. The hit rate is projected at 98

The two-set cache allows two virtual addresses with identical displacements to reside in cache simultaneously. This reduces the amount of thrashing in cache, a condition where a cache miss-sequence overwrites a cache reference and is overwritten by the original reference a short time later. In a two-set cache, the data for each reference can be in opposite cache sets, which avoids thrashing.

The cache is a high-speed buffer that holds the last memory locations accessed. The buffer is loaded the first time a memory location is referenced, allowing subsequent references at faster access times.

4.1.2.3.2 Cache Addressing

Cache addressing is performed using the following five registers:

- IRP
- ERMA
- PRMA
- EAS
- EAD

The IRP register provides addresses for fetching instructions of the executing program.

The ERMA and PRMA registers are used to restore cache addresses after a cache miss or an unaligned read. The PMA register stores instruction addresses, while the PRMA register stores operand addresses.

The EAS and EAD registers are microcode-visible 32-bit registers that handle string instructions. The registers are used together to execute string instructions, procedure calls, process exchanges, and other microcode algorithms that reference consecutive memory locations.

4.1.2.3.3 Branch Cache Operations

Branch cache logic is designed to speed the flow of branch or jump class instructions through the pipeline. Branch instructions alter the instruction sequence, forcing the machine to flush partially processed instructions from the pipeline following the branch. This detriment to system performance is avoided by replacing the address of the next sequential instruction in the program counter with the target address of the branch.

The branch cache algorithm causes the branch instruction to branch the same way as the previous time the instruction was executed. This maintains a higher level of system performance. Branch cache logic consists of the branch cache array, detection logic, and gaffe or "bad branch" logic.

4.1.2.3.4 Segment Table Lookaside Buffer (STLB)

The Segment Table Lookaside Buffer (STLB) is a hardware memory mapping buffer used by the CPU that contains previously translated physical memory addresses. The Model 4050/4150 is equipped with a two way set associative STLB that has a total of 1024 entries, 512 per set.

The STLB performs fast virtual address to physical address conversion when the CPU is in segmented/virtual mode. A trap condition (STLB miss) occurs if the conversion is not successful.

4.1.2.3.5 Memory Traps

The S unit detects the following memory traps each time cache is accessed for instruction or operand data:

- STLB misses
- Read and write address traps
- Ring 3 and ring 1 access violations
- Page modified traps

4.1.3 E BOARD

The Model 4050/4150 E Board combines the functional components of the E1 and E2 Boards of the 9950, with some variations. For example, the I/O addressing logic and priority resolution logic reside on the 4050/4150 E Board. The E Board also contains the system's number crunching hardware, and timers to track process and wall clock time. Figure 4-4 is a functional diagram of the E Board. The E Board contains the these major functional blocks, which are described in the sections that follow:

- Execution Unit
- I/O Addressing Interface
- Timers

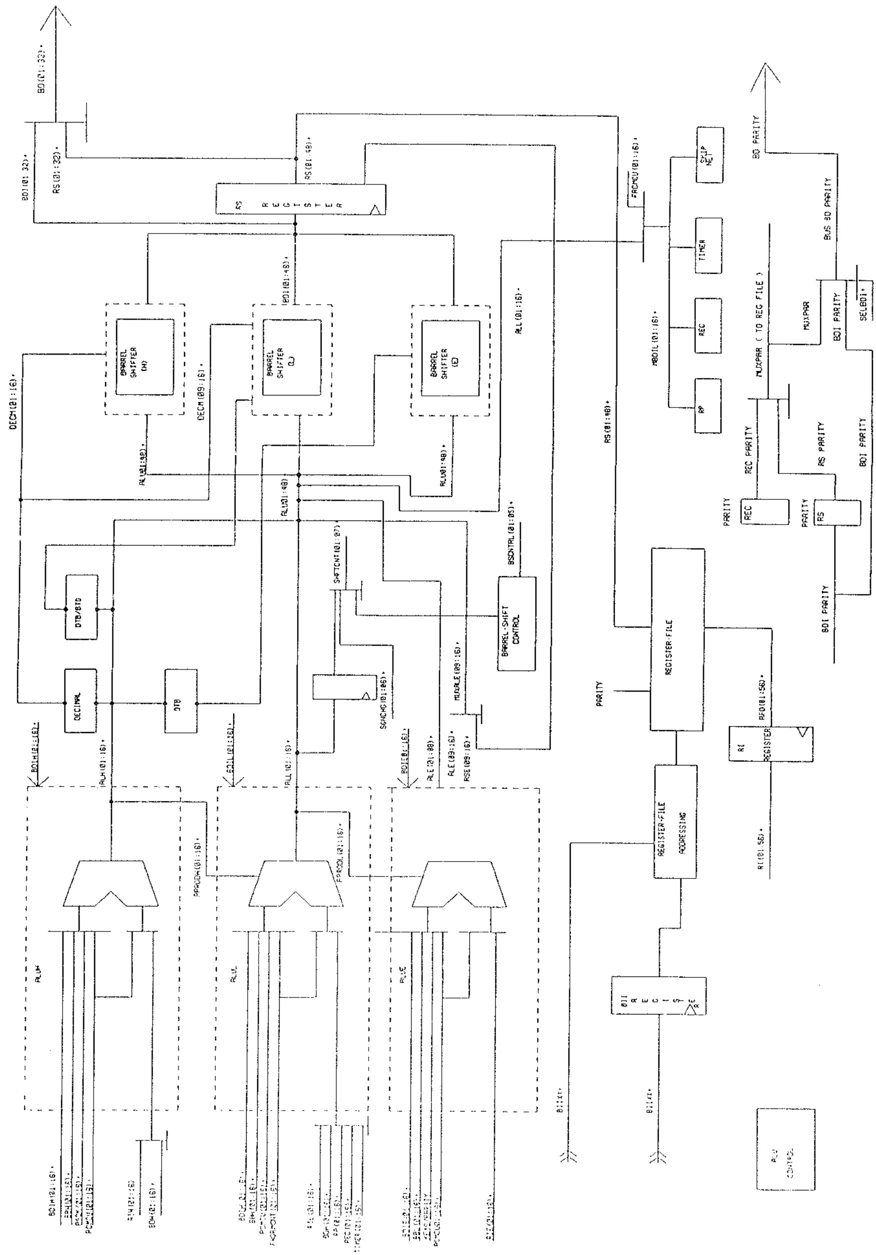


FIGURE 4-4: E BOARD BLOCK DIAGRAM

4.1.3.1 Execution Unit

The Execution (E) Unit consists of the Arithmetic Logic Unit (ALU), the barrel shifter, the register file, register file addressing logic, and other data manipulation registers. The E Unit reads one or more sources of data, manipulates the data in the ALU, transports or manipulates the data in the barrel shifter, then loads the data into one of the registers on the E Unit, the I Unit, memory, or into the register file.

These E Unit functional blocks are described in the paragraphs that follow:

- Arithmetic Logic Unit (ALU) Slices
- Barrel Shifter
- Register File Logic

4.1.3.1.1 Arithmetic Logic Unit (ALU) Slices

The ALU is implemented on seven PEALU slices. They are described in more detail under VLSI Requirements in this chapter. The ALU manipulates data from two sources, the A Bus and B Bus (refer to Major System Buses in this chapter). The main 48-bit ALU is divided into three 16-bit sections. These sections are designated High (H), Low (L), and Extra (E). The sources for these buses are shown in Table 4-2.

TABLE 4-2: ALU DATA SOURCES

BUS	SOURCE	COMMENT
A(H)	RIH(1 : 16) BDH(1 : 16)	Register file data
A(L)	RIL(1 : 16) BDL(1 : 16) RPREC(1 : 16)	 Counters
A(E)	RIE(1 : 16)	
B(H)	BDIH(1 : 16) BBH(1 : 16) PACK(1 : 16) RCMCU(1 : 16)	 For decimal conversions the emit field
B(L)	BDIL(1 : 16) BBL(1 : 16) RCMCU(1 : 16) FNRMCNT(1 : 16)	 Floating point operations
B(E)	BDIE(1 : 16) BBL(1 : 16) KEYS/PARITY(1 : 16) RCMCU(1 : 16)	

The Model 4050/4150 system ALUs incorporate multiply and divide logic in them, but are otherwise predominantly functionally equivalent to 9950 ALUs.

4.1.3.1.2 Barrel Shifter

The barrel shifter performs shift/rotates on 16, 32, or 48-bit boundaries. The barrel shifter is also used for floating point adjust and normalize operations.

4.1.3.1.3 Register File Logic

The register file address component generates the address for the register file for read/write phases. It also generates information used during register bypass, IS Board regiser file tracking, the RP/REC counter pair, and address trap logic.

4.1.3.2 I/O Addressing Interface

Model 4050/4150 I/O logic is implemented on two CPU boards. The I/O data interface resides on the CMI board (refer to CMI Board Functions in this chapter). The I/O addressing interface resides on the E Board.

In the address phase of an I/O transfer, the I/O controller with bus control sends information to the CPU about the type of I/O transfer required and the target or source address of the data. After the data is actually transferred during the data phase, another address phase is performed to determine if any other controllers require servicing. When all controllers are serviced, the microcode exits the trap caused by the initial service request and returns to its original task.

Control and data paths are closely tied to the memory controller logic on the CMI board. Data is transferred to or from memory on an internal MC bus, rather than the system BD bus.

4.1.3.3 Timers

The E Board contains two timers that track process and actual time. These counters are the microsecond timer and the PIC timer. The microsecond timer overflows every millisecond if there are no other gating conditions. The PIC overflows every four seconds. These overflows cause fetch cycle traps, which activate microcode to perform the necessary task.

4.1.4 CMI BOARD

The Model 4050/4150 CMI board is the functional equivalent of the CS, MC, and clock boards of the 9950. The CMI board includes the control store, the memory controller, I/O data interface support, and clock generation circuitry. The board also contains an VCP-V Diagnostic Processor interface, decode net logic, and other instruction decoding hardware used for microcode sequencing. Figure 4-5 is a functional diagram of the CMI Board.

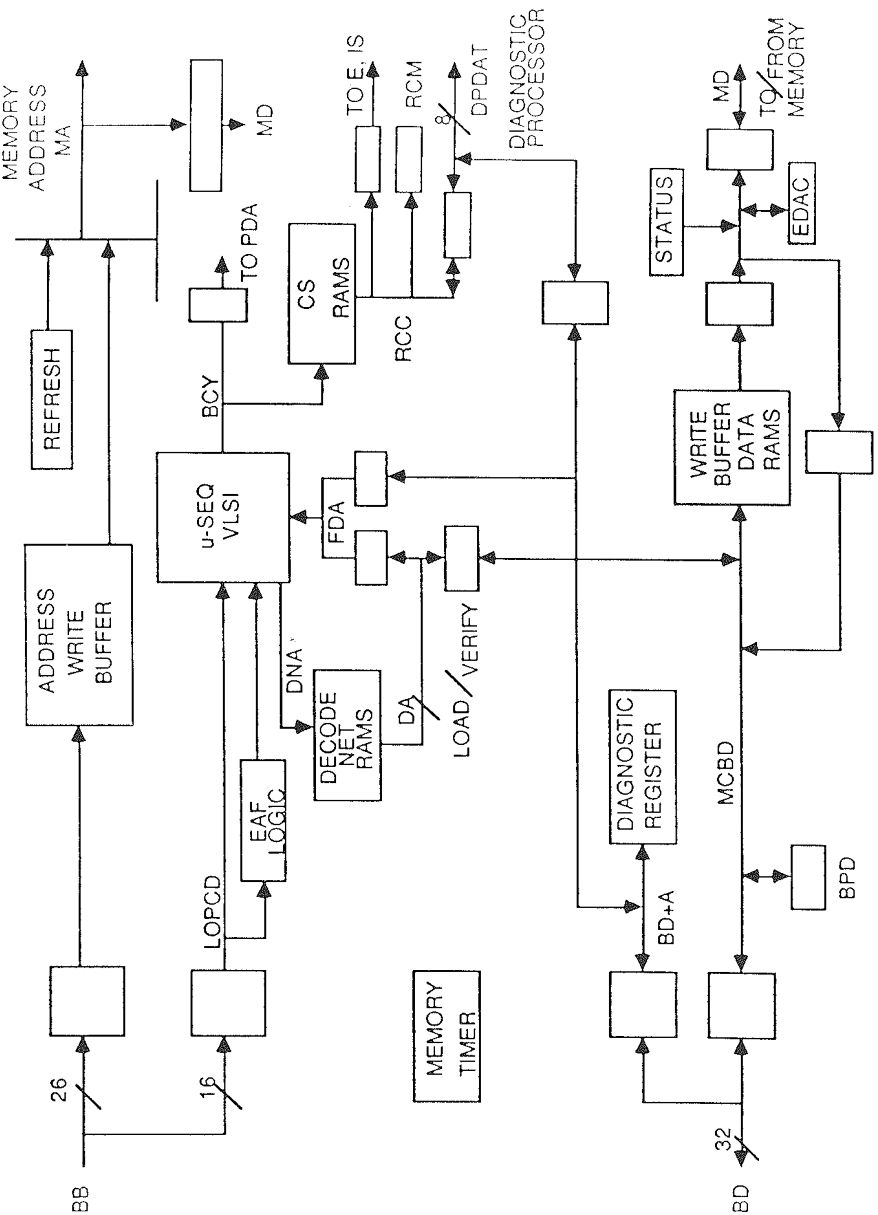


FIGURE 4-5: CMI BOARD BLOCK DIAGRAM

A CMI Board functional description is provided in the following subsections:

- Control Store Unit
- Memory Controller Unit
- I/O Data Interface

4.1.4.1 Control Store Unit

The Control Store (CS) is a writable memory for buffering system microcode. CS logic allows execution of the current microword to overlap the the next microword fetch from the CS.

Control store logic is comprised of the hardware elements described in the subsections that follow:

- Microsequencer Logic
- Control Store RAM
- Maintenance & Initialization Logic
- Decode Net
- Modals
- Effective Address Field (EAF) PROMs
- Parity Checkers
- Bus Operand Source (BOPS) Logic
- Opcode Latch
- BCYPDA Bus

4.1.4.1.1 Microsequencer Logic

The microsequencer logic consists of two VLSI components that produce the control store address. The address bits are referred to as BCY bits.

4.1.4.1.2 Control Store RAM

The control store consists of a 16K x 80-bit static RAM array. The output of the array is buffered, latched, or registered as appropriate, and then sent to all microcode controller hardware.

4.1.4.1.3 Maintenance & Initialization Logic

Maintenance and initialization logic consists of an interface between the VCP-V Diagnostic Processor or Processor Diagnostic Aid (PDA) and the CPU. The interface is performed by one of the following three modes of operation:

1. The CPU is halted and either the VCP-V or PDA needs to write or read the control store
2. The CPU is running and the VCP-V and CPU needs two-way communication.
3. The CPU is running and either the VCP-V or PDA needs to force a BCY address.

4.1.4.1.4 Decode Net

The decode net is a 4096 x 20 bit lookup table addressed by the microsequencer logic. The output can by used by the microsequencer to address the control store. This provides the machine with a way to determine the microcode entry point for PMA routines.

4.1.4.1.5 Modals

The control store logic maintains a copy of the modals. The modals contain information about the way the machine should process the instruction stream.

4.1.4.1.6 Effective Address Field (EAF) PROMs

The output of the Effective Address Field (EAF) PROMs are used by both the microsequencer and the I Unit to help calculate the effective address of the operand.

4.1.4.1.7 Parity Checkers

The outputs of the control store RAMs (80 bits) are parity checked on 10-bit boundries.

4.1.4.1.8 Bus Operand Source (BOPS) Logic

The bus operand source bits are generated in the control store logic and sent to the I unit. They are used in register file tracking.

4.1.4.1.9 Opcode Latch

The control store receives BBH bits (1-16) containing opcode information during odd pipeline stages. These bits are latched on a signal from the I unit and sent to the microsequencer, the EAF PROM, and the BOPS logic.

4.1.4.1.10 BCYPDA Bus

The control store sends a private bus containing BCY information to the PDA.

4.1.4.2 Memory Controller Unit

The Memory Controller (MC) Unit acts as an interface between memory and the CPU. The MC unit buffers data destined for memory, then writes to memory while the CPU continues processing. The MC unit automatically adjusts its memory addressing scheme to interface with any legal memory configuration during system initialization.

The Memory Controller contains these two functional blocks that are described in the subsections that follow:

- Write Buffer (WB)
- Memory Timer (MT)

4.1.4.2.1 Write Buffer (WB)

The Write Buffer (WB) consists of four 64-bit locations further divided into four 16-bit sections. The WB consists of two main parts as follows:

- ADDRESS SECTION - This section consists of two VLSI parts that hold addresses sent from the IS Board for main memory writes. It contains valid and status information about data destined for memory.
- DATA SECTION - This section consists of RAMs that hold data destined for memory, and ECC circuitry that generates and checks ECC bits to improve the integrity of main memory.

4.1.4.2.2 Memory Timer (MT)

The Memory Timer consists of PROMs whose data outputs are flopped and then sent to memory as control signals or are used in MC logic as additional control bits.

4.1.4.2.3 I/O Data Interface

Model 4050/4150 I/O logic is implemented on two CPU boards. The I/O address interface resides on the E board (refer to E Board Functions in this chapter). The I/O data interface resides on the CMI Board.

Control and data paths are closely tied to the memory controller logic, which is also on the CMI board. As a result, data is transferred to or from memory on an internal MC bus, rather than the system BD bus.

4.1.5 VLSI REQUIREMENTS

The Model 4050/4150 system CPU uses the following Very Large Scale Integration (VLSI) parts:

- Microsequencer (PUSEQ)
- Cache Address (PCADR)
- STLB Set Select (PSSS)
- Cache Set Select (PCSS)
- Execution ALU (PEALU)
- Barrel Shifter (PBDI)
- Write Buffer Address (PADBUF)

- Register File Address (PRFADR)

The mnemonic for each part has a "P" added as a prefix to distinguish it from similar parts on the Model 6350/6550 system.

Each is briefly described in turn in the following sections.

4.1.5.1 Microsequencer

The microsequencer (PUSEQ) controls the execution of microcode from the control store (CS). The PUSEQ's BCY (Bus Control Address) outputs are used to address the CS RAMs.

The PUSEQ is partitioned into two identical slices. Each slice produces seven of the 14 lines necessary to address the CS. Each slice also produces decode net address bits. Both slices reside on the CMI board.

4.1.5.2 Cache Address

The Cache Address (PCADR) chip contains logic to maintain and source the I and S units internal memory address bus. This bus is used to produce the address for all memory related accesses on the IS board. These include cache address, STLB address, branch cache address, and backup copies of the effective address (ERMA) and program counter (PRMA) registers.

PCADR is partitioned into two identical slices. One slice produces the low order bytes of both MAH and MAL buses, while the other slice produces the high order bytes of those same buses. Both PCADR slices reside on the IS board.

4.1.5.3 STLB Set Select

The Segment Translation Lookaside Buffer (STLB) contains previously translated physical memory addresses. The 4050/4150 employs a two-set STLB. The STLB Set Select (PSSS) chip determines which set, if either, has a valid translation for the current memory reference. If neither set has a valid translation, a memory trap is raised and the processor's microcode determines memory access.

The PSSS is partitioned into two identical slices. Each slice monitors one set of the STLB for valid translations and signals its findings on its outputs. The IS board monitors these outputs and takes the translation from the valid set. Both slices reside on the IS board.

4.1.5.4 Cache Set Select

The 4050/4150 used a two-set data cache similar to the two-set STLB. The Cache Set Select (PCSS) chip monitors the cache to determine which set, if either, has valid data, and signals a cache miss, if neither set is valid. The PCSS also drives BB with the required source as specified by the microcode.

The PCSS is partitioned into two identical slices. Each slice watches one set of the cache and signals its findings on its outputs. The IS board, which holds the PCSS chips, makes the final hit/miss decision, and starts a cache miss routine on the MC if necessary. Both slices reside on the IS board.

4.1.5.5 Execution ALU (PEALU)

The 4050/4150 E unit consists of a 48-bit data path that can be extended to 56-bits for multiply and divide operations. The E unit ALU (PEALU) chip provides the full-function two-input ALU, which performs the number crunching functions of the data path. Look ahead carry logic and carry-save adder logic is also provided by these chips.

The 56-bit data path is made up of seven identical PEALU slices. Each slice is eight bits wide. All slices reside on the E board.

4.1.5.6 Barrel Shifter

The Bus D Interface (PBDI) chip provides full arithmetic, logical and barrel shifting, rotating, normalization of floating point numbers, and floating point adjust, all over a full 48-bits. It also provides guard bit support for multiplication, and decimal pack and unpack.

The PBDI is implemented in three identical slices. Each slice produces 16 outputs, which are driven to the rest of the machine. All three slices reside on the E board.

4.1.5.7 Write Buffer Address

The write buffer attempts to make better use of the memory bandwidth by saving 16 and 32-bit writes coming in from the CPU and concatenating them into 64-bit writes before actually writing to memory. The ADdress BUFfer (PADBUF) chip provides the address and valid bit memories necessary for such a buffer.

The PADBUF is implemented in two identical slices, each of which drives half of the memory address bus. Status about the write buffer as a whole can be taken from either slice. Both slices reside on the CMI board.

4.1.5.8 Register File Address

The Register File Address (PRFADR) chip provides an 8-bit address to the E unit's register file. The addresses are determined from RCM bits, BPA bits, DTAR bits, BBH bits, base register select bits, or BOPS bits. The PRFADR chip can handle all of these cases. The skip net and the RP and REC counters are also implemented by the PRFADR.

Only one PRFADR slice is necessary to perform all these functions. The slice resides on the E board.

4.2 MAJOR SYSTEM BUSES

The Model 4050/4150 system uses the following major buses:

- Bus BLEG (BB)
- Bus Data (BD)

- Bus Peripheral Address (BPA)
- Bus Peripheral Data (BPD)
- Bus Memory Address (MA)
- Bus Memory Data (MD)

Buses are described in the paragraphs that follow.

4.2.1 BUS BLEG (BB)

Bus BLEG (BB) is driven only by the I unit and S unit. It is most frequently used to transfer cache data from cache to the E unit (operands) or control store (instruction stream). The BB also drives the physical address to the memory controller on memory references.

4.2.2 BUS DATA (BD)

Bus Data (BD) is driven by any processor unit. It is most frequently used to transport Arithmetic Logic Unit (ALU) output to I unit destinations or memory. It is also used to transport data from memory to cache during cache misses, and to transport data from the VCP-V to the CPU.

Bus Data is the only bus in the system that can be driven by multiple sources on different processor boards, thus the need for arbitration. The execution unit on the E Board performs BD arbitration.

The E unit normally has control of the BD. Control must be relinquished during the following system events:

- Cache misses
- Processor Diagnostic Aid forced BCYs
- I/O transfer address phases
- Explicit microcode controller memory reads

When a change of BD control is required, the unit in control of the bus is disabled. One half beat later, the new unit in control is enabled. This technique provides a half beat period between any two units driving the BD to avoid tri-state clashes.

4.2.3 BUS PERIPHERAL ADDRESS (BPA) AND BUS PERIPHERAL DATA (BPD)

The Bus Peripheral Address (BPA) and the Bus Peripheral Data (BPD) are used to transfer address and data information respectively between the CPU and I/O controllers.

4.2.4 BUSES MEMORY ADDRESS (MA) AND MEMORY DATA (MD)

Buses Memory Address (MA) and Memory Data (MD) are used to address main memory and transfer data to and from memory respectively.

4.3 MEMORY SUBSYSTEM

The MMW3-8MB memory array board provides storage media for Model 4050/4150 systems. Model 4050/4150 systems hold up to four MMW3-8MB memory array boards for a total of 32 Mb of internal storage.

The MMW3-8MB memory array board has the following features:

- Provides a maximum of 1,048,576 words of 78 bits of storage through the use of 312 256K x 1 dynamic RAM chips.

- 78-bit internal data storage (64 data bits and 14 check bits, representing two 39-bit words).

- A 39-bit external data path between MMW3-8MB and the CPU.

- Communicates with the memory controller unit of the central processor via a bus that automatically adjusts to the operating speed of the controller.

- Provides the storage for the check bits used in error detection and correction, but the detection and correction take place in the memory controller portion of the CMI CPU board (ECC VLSI).

- Odd parity

4.3.1 MEMORY ARRAY LAYOUT

The storage array is configured as a matrix of 12 rows and 26 columns of 256K x 1 dynamic RAM chips (see Figure 4-6). Three contiguous rows constitute one memory bank of 2 Mb. MM24-8MB has 12 rows, or four banks, for total storage capacity of 8 Mb.

The 26 columns represent the data (and check bits) of 13 of the bits of two interwoven 39-bit words.

4.3.2 MEMORY ARRAY SELECTION

To select a memory array board, four memory address bits (MA91+ through MA94+) are compared to the slot ID Code (select control inputs, MSSO+, MSS1+, MSS2+). Address bits MA95+ AND MA96+ select one of four banks in the array.

4.3.3 FUNCTIONAL DESCRIPTION

A functional block diagram of the MA board is shown in Figure 4-7. The major functional blocks are as follows:

- Control Latch

- Board and Bank Select

- Row and Column Address Mux

- Parity Check

- Timing and Controls

HANDLE END OF BOARD

LEFT SIDE OF BOARD

A ODD
B EVEN

	A	B	A	B	A	B	A	B	A	B	A	B
BANK 3	32	32	29	29	26	26	23	23	20	20	17	17
	31	31	28	28	25	25	22	22	19	19	16	16
	30	30	27	27	24	24	21	21	18	18	15	15
BANK 2	30	30	27	27	24	24	21	21	18	18	15	15
	31	31	28	28	25	25	22	22	19	19	16	16
	32	32	29	29	26	26	23	23	20	20	17	17
BANK 1	32	32	29	29	26	26	23	23	20	20	17	17
	31	31	28	28	25	25	22	22	19	19	16	16
	30	30	27	27	24	24	21	21	18	18	15	15
BANK 0	30	30	27	27	24	24	21	21	18	18	15	15
	31	31	28	28	25	25	22	22	19	19	16	16
	32	32	29	29	26	26	23	23	20	20	17	17

DRIVERS

RIGHT SIDE OF BOARD

A	B	A	B	A	B	A	B	A	B	A	B	A	B
14	14	12	12	10	10	8	8	6	6	4	4	2	2
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
14	14	12	12	10	10	8	8	6	6	4	4	2	2
14	14	12	12	10	10	8	8	6	6	4	4	2	2
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
14	14	12	12	10	10	8	8	6	6	4	4	2	2

CONNECTOR END OF BOARD

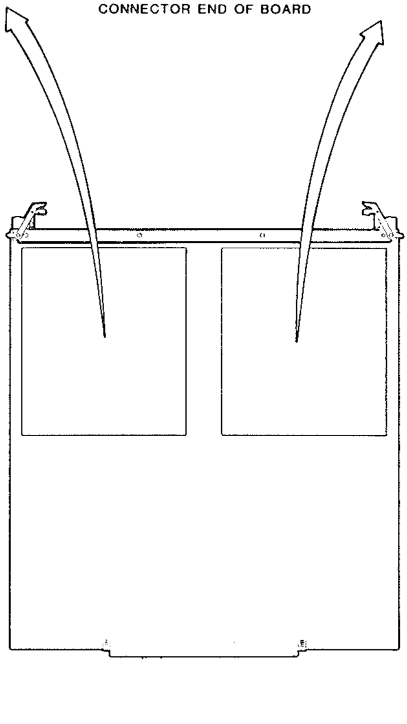


FIGURE 4-6: MEMORY ARRAY LOCATIONS

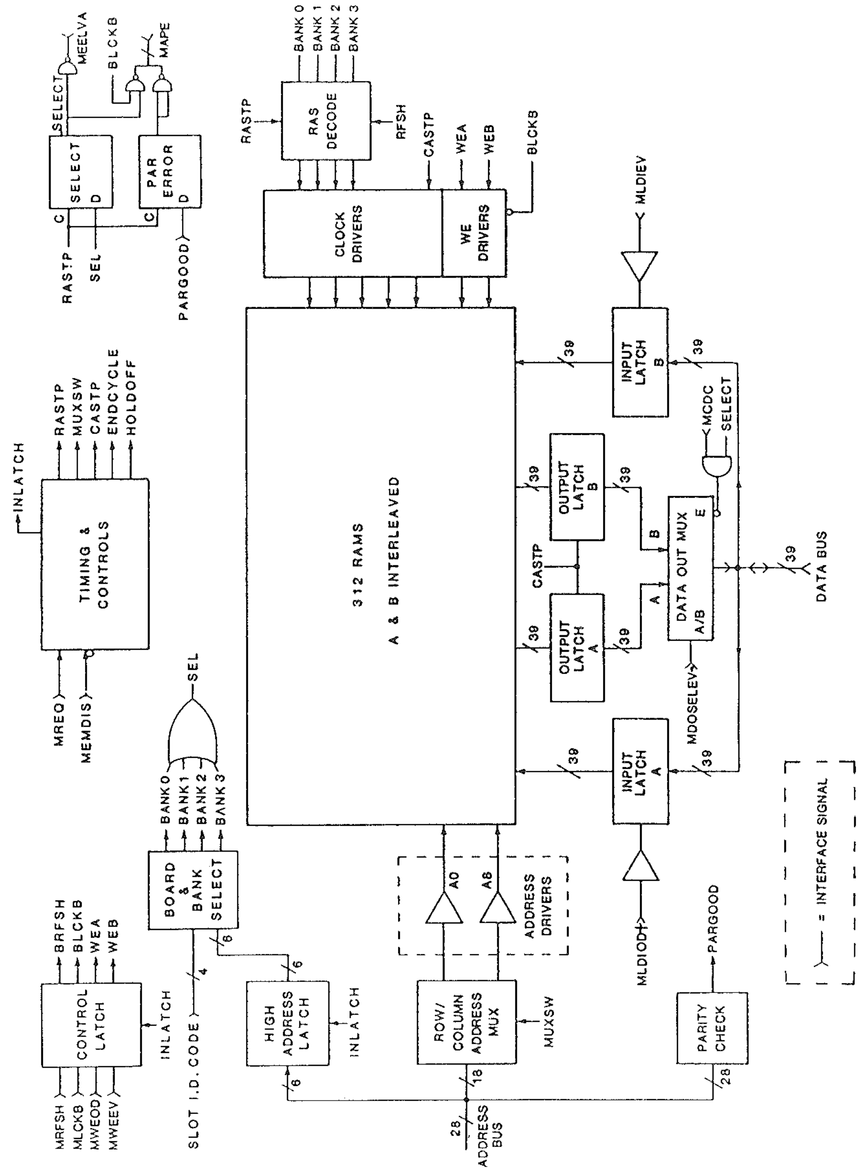


FIGURE 4-7: MEMORY ARRAY BLOCK DIAGRAM

Tables 4-3 and 4-4 present the input control and output control signals of the MMW3-8MB memory array board.

TABLE 4-3: INPUT CONTROLS

SIGNAL	DESCRIPTION
MREQ-	Memory Cycle Request (Low True)
MEMDIS-	Disable MREQ from initiating a cycle
MRFSH-	Refresh Cycle Indicator
MGDO-	Gates Output Data to Bus
MLDIOD+	Close Odd Input Data Latch
MLDIEV+	Close Even Input Data Latch
MDOSELEV-	Select Odd or Even Output Data
MWEEV-	Write 39 Bits to Even Array
MWEOD-j	Write 39 Bits to Odd Array
MLCKB-	Inhibit Writing to Check Bits
MSSO+	Slot Select ID Code LSB
MSS1+	Slot Select ID Code Next MSB
MSS2+	Slot Select ID Code MSB

TABLE 4-4: OUTPUT CONTROL SIGNALS

SIGNAL	DESCRIPTION
MAPE-	Address Parity Error Flag
MSELVAL-	MM24-8MB Responded to MREQ-
MEMSIZEA-	Array Board Size Indicator
MSIZEB-	Array Board Size Indicator

4.3.4 MEMORY OPERATIONS

The MMW3-8MB Memory Array unit performs the following operations:

- Refresh Cycle
- 39-bit and 78-bit Write Cycles
- Read Cycle

4.3.4.1 Refresh Cycle

DRAM memory devices require periodic refresh signals to maintain the stored data. Data is refreshed along 256 specific row addresses (MA14+ through MA-07+).

Refresh occurs when the controller provides the Row address for the RAMs in the array and issues the signal MRFSH-, along with the MREQ signal. All RAMs at the row addressed are refreshed. The controller then increments the Row address and issues another Refresh cycle request.

4.3.4.2 Write Cycle

The MMW3-8MB performs write cycles in which words of 39 bits of data or 78 bits of data are written to memory. Both write cycles take the same amount of time to complete.

4.3.4.2.1 39-Bit Write

During a 39-bit Write to the MMW3-8MB memory array board, the controller performs the following operations:

1. Determines the address into which the data is to be written.

2. Sets the data onto the data bus.

3. Presents the appropriate WE signal to the memory board.

4. Initiates the write operation by issuing MREQ-.

A parity error causes a write operation to become a refresh operation. At the beginning of each cycle, MMW3-8MB checks the parity of the address to see that odd parity is obtained. In the event of a parity error, the parity error flop is set and the signal MAPE- is activated, and the CAS signal is inhibited on MMW3-8MB. When CAS is inhibited, the data that was to be written is ignored, and the cycle becomes in effect a refresh to the address that is selected by the suspect address.

Since MMW3-8MB selects both the A and B halves of the selected address on each operation, in a 39-bit write operation, the half that is not written into is still cycled and a non-destructive read of that side takes place while the selected side is being written.

4.3.4.2.2 78-Bit Write

A 78-Bit Write operates as follows:

1. The controller preloads one set of MMW3-8MB input data latches with the first 39-bit word and provides the appropriate latch control signal (MLDIODD+ or MLDIEV+) before initiating the memory write cycle.

2. The controller loads the second 39-bit word into the other set of input latches.

The rest of the cycle is the same as a 39-bit write, with the exception that both WE signals must be provided in order that both 39-bit words are written into MMW3-8MB.

3. The controller presents both WE signals to MMW3-8MB.

4. The controller initiates the write operation by issuing MREQ-.

4.3.4.2.3 Diagnostic Aid Lock Check Bits

MMW3-8MB logic allows the memory controller to inhibit the writing of data into the check bit RAM chips. This feature provides the controller with a means to diagnose its error detecting and correcting circuits. The feature is activated during a write operation when the controller issues the lock check bit signal (MLCKB-). The MLCKB- signal is common to both the A and B words.

The controller can identify which memory board has been selected and its location by a unique MAPE- signal sent from the board to the controller.

4.3.4.3 Read Cycle

All read cycles obtain 78 bits of data from the RAMs. Data is read from the RAMs and latched into two sets of 39 latches whose outputs feed a two to one multiplexer. The selector control of the multiplexer is derived from the MDOSELEV- interface signal and determines which of the two 39-bit words will be presented to the data bus.

4.3.5 BATTERY BACKUP UNIT FOR MEMORY SUBSYSTEMS

MMW3-8MB incorporates a voltage plane, a groundplane, and two signal layers in its printed circuit board assembly. The voltage plane is separated into two sections, a feature that allows memory refresh operations even when the system temporarily loses main power.

One section of the voltage plane is connected to the input and output data latches and to pins on the interface connector that supply a voltage that is not backed up by batteries. The other section is connected to the RAM chips, the address and clock drivers, and the time circuitry, and to pins on the connector that are supplied with a battery backed-up power supply. This allows the system to maintain the integrity of memory contents by requesting MMW3-8MB to do refresh cycles during the power outage.

The system can prevent MMW3-8MB from responding to false MREQ- signals during the power fail detection time by issuing the MEMDIS- signal. During the power outage time, the controller need not vary the state of MRFSH- for every cycle; instead the controller can assert MRFSH-, keep it asserted and issue MREQ- at the refresh rate along with refresh address.

4.4 I/O CONTROLLERS

The basic function of peripheral and communications controllers are detailed in this section.

An I/O controller has the following three basic functional components (see Figure 4-8):

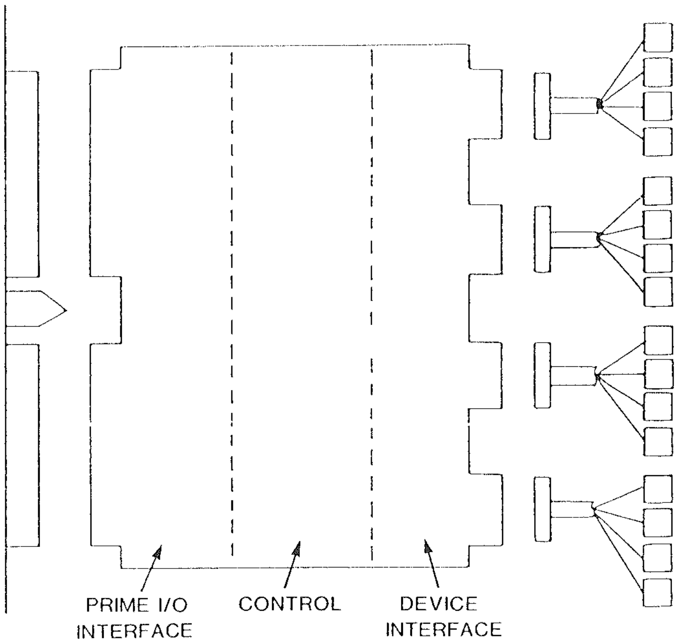


FIGURE 4-8: I/O CONTROLLER FUNCTIONAL COMPONENTS

- The I/O Bus Interface Logic - Interfaces the controller with the CPU. Because it is a standard, this section is nearly identical, both physically and logically, for all controllers.

- The Peripheral Device Interface - Interfaces the Control Section Logic to the peripheral device or communications link. For example: the EIA or 20 mA drivers and UARTS (universal asychronous receiver/ transmitter), that actually drive the communication lines on an AMLC, are part of the Peripheral Device Interface for the AMLC controller.

- The Control Section Logic - Provides control over the conversion of data and commands from the CPU, to a format compatible with the output device. This logic interfaces the other two sections.

I/O controllers provide data link between external devices and the CPU. This is accomplished by an I/O bus common to all controllers and the CPU. The I/O Bus consists of the BPA (Peripheral Address Bus), the BPD (Peripheral Data Bus), and the Peripheral Command Bus (BPC). The CPU places a PIO command on the BPC and the controller with the correct device address responds.

The I/O controllers have unique device addresses hard wired to the board, instead of being determined by slot selection. When identical model controllers are configured in a system, the device address must be changed, thus allowing the CPU to interface with the correct device.

The types of I/O controllers supported by both models are as follows:

- Peripheral Controllers
- Communication Controllers

4.4.1 PERIPHERAL CONTROLLERS

Peripheral controllers provide the following two functions:

- Regulate the transfer of data between the CPU and external devices.
- Ensure consistency between the electronic speed of the CPU with the mechanical speed of the external device.

For information regarding Prime peripheral controllers, reference the Memory and Controller Boards Service Manual (SMN500) and the appropriate peripheral service manual.

4.4.2 COMMUNICATIONS CONTROLLERS

The Model 4050/4150 system supports all of Prime's communications hardware controllers. User terminal communications are handled by the Intelligent Communications Subsystem Model 3 or the Asynchronous Multi-line Controller (AMLC).

Communications for synchronous software products are handled by the Multi-Line Data Link Controller (MDLC), a controller handling multiple line protocols. For local area networks, the system can be linked in a high-speed ring network with other 50 Series systems via PRIMENET Node Controller (PNC or PNC-II), or Local Area Network (LAN300).

Prime offers the following communications products:

- Asynchronous Multi-Line Controller (AMLC) - allows interfacing between user terminals and the host system.
- PRIMENET Node Controller (PNC and PNC-II) - and PRIMENET software, connects Prime hosts/nodes into a local ring network.
- Multi-Data Link Controller (MDLC) - provides interface between a Prime host and a packet-switching network or another type of host; such as IBM, CDC, UNIVAC, and Honeywell.
- Local Area Network (LAN300) - enables data exchange among computers and other network-related devices.

It is possible to configure a very large network over hundreds of miles, using a combination of Prime systems with PNCs and MDLCs, and packet-switching networks.

Prime communications hardware is supported by software products other than PRIMENET. Remote Job Entry (RJE) allows an interactive Prime host to network with and simulate the batch operation of large mainframes, such as IBM and UNIVAC. Distributed Processing (DPTX) networks a Prime host to an IBM 3270. Transparent to the users, all terminals can communicate directly with either host. All resources of both systems are shared.

Communications products are described in the following subsections:

- ICS3
- PNC-II
- AMLC
- LAN300
- MDLC

4.4.2.1 Intelligent Communications Subsystem 3 (ICS3)

The ICS3 is a 16-bit Zilog Z8001 based communications controller capable of supporting synchronous and asynchronous serial communications lines concurrently. Each line can be configured to support a variety of protocols and electrical interfaces.

The ICS3 includes the following components:

- ICS3 Controller
- Sixteen-Slot Card Cage
- Buffer Card
- LAC Backplane
- Line Adapter Cards (Synchronous and/or Asynchronous)

ICS3 components are described in the following subsections. For a more detailed functional description, refer to Intelligent Communications Subsystems Service Manual (SMN250-B).

4.4.2.1.1 ICS3 Controller

The ICS3 controller is a programmable, microprocessor based communications controller. It uses the same architecture as the ICS2 controller, but provides enhanced speed and memory. The ICS3 RAM ECC logic can detect multiple bit errors and correct single bit errors.

The controller has two main functional areas: the Z8001 microprocessor and its related support logic, and the Inter-Bus Controller (IBC).

The Z8001 functional area contains the Z8001 microprocessor itself, PROM and RAM memory, the Z8001 Bus, a Counter-Timer-Circuit, a serial communications controller, and interface logic.

The Inter-Bus Controller is a specialized, high-speed microcode controlled device whose primary task is to control the flow of data between the Z8001 bus, the Line Adapter Card bus, and the Prime I/O bus.

4.4.2.1.2 Sixteen-Slot Card Cage

The ICS3 card cage is mounted on the mainbay bulkhead or in the peripheral cabinet. The card cage houses up to 16 Line Adapter Cards in two groups of eight. Each group of eight LACs has its own backplane and buffer card. One power supply mounted between the two groups of LACs provide operating power for all 16 cards. When mounted in the mainbay, the card cage is cooled by the system blower assembly. When mounted in the peripheral cabinet, the card cage is cooled by its own fan tray.

4.4.2.1.3 Buffer Card

The buffer card provides an electrical interface between the ICS3 controller and the LAC bus. It also checks the parity of data and address information transmitted between the controller and buffer board, and controls LAC card interrupt priority.

The buffer card contains a green LED, which should always be on when the system is powered to indicate the presence of +5 Vdc.

4.4.2.1.4 LAC Backplane

The LAC backplane provides seating for all LAC cards. The LAC backplane bus is a synchronous, tri-state eight-bit bus incorporating a multiplexed address and data path. The LAC bus also provides control signals and select bits for LAC card and communications line selection.

4.4.2.1.5 Line Adapter Cards

The asynchronous RS-232 LAC sends and receives serial streams of data to and from the Data Terminal Equipment (DTE). Each LAC supports four communications lines (circuit numbers 0, 1, 2, and 3), its own baud rate generator, timing logic, and loopback control logic. The asynchronous LAC contains an integral bulkhead. Connectors for the four communications circuits supported by the LAC are mounted on the integral bulkhead. These nine-pin D-type connectors are labelled J1, J2, J3, and J4.

The synchronous LACs are available in two versions: V.24 and V.35. The V.24 LAC supports line speeds up to 19,200 baud. The V.35 LAC supports line speeds ranging between 19,200 to 64,000 baud. Synchronous LACs support only two communications circuits (0 and 1), and does not contain any internal loopback logic, but does contain an integral bulkhead. The two circuits are labelled J1 and J2.

<u>4.4.2.2 PRIMENET Node Controller (PNC-II)</u>

The PNC-II is a programmable, microprocessor-driven data communications subsystem. It consists of:

- Controller Assembly
- Associated Cabling
- Junction Box

4.4.2.2.1 Controller Assembly

The PNC-II controller is a standard-size 50-series PCB. It attaches to the Prime I/O bus in the standard manner, using 2 100-pin connectors and occupying one slot in the backplane. Firmware for self-testing is resident on the board in PROM. The board also contains 22 chips of RAM, and six LEDs at the board edge. Significant components in the architecture of the PNC-II are:

- INTEL 80186 microprocessor
- Address and Data Busses
- PROM
- RAM
- DMA Controller
- Host Backplane Interface Logic
- Zilog Counter Timer
- Zilog Serial Communication Circuit
- LED Displays

80186 MICROPROCESSOR AND SUPPORT LOGIC

A 16-bit, 8 MHZ, microprocessor, the Intel 80186 (referred to as the 186), is the main control element of the PNC-II. The 186 has direct control of all memory and peripherals. All peripheral devices are accessed via I/O instructions, whereas all RAM and PROM use memory instructions. One non-maskable interrupt (NMI) and 4 maskable interrupts notify the 186 of hardware events. Logic in support of the 80186 includes various buffers, drivers, memory and I/O address decoding logic, and system clock circuitry. A 16 MHz crystal oscillator provides the input clock to the 186 which outputs an 8 MHz clock which is used as the system clock for the 186.

INTERNAL BUS STRUCTURE

The PNC-II utilizes several address buses and many data buses.

- 80186 address buses
- Board data buses
    - 80186 address/data bus
    - RAM data bus
    - I/O data bus

Refer to Figure 4-9 in this section for the layout of the PNC-II board.

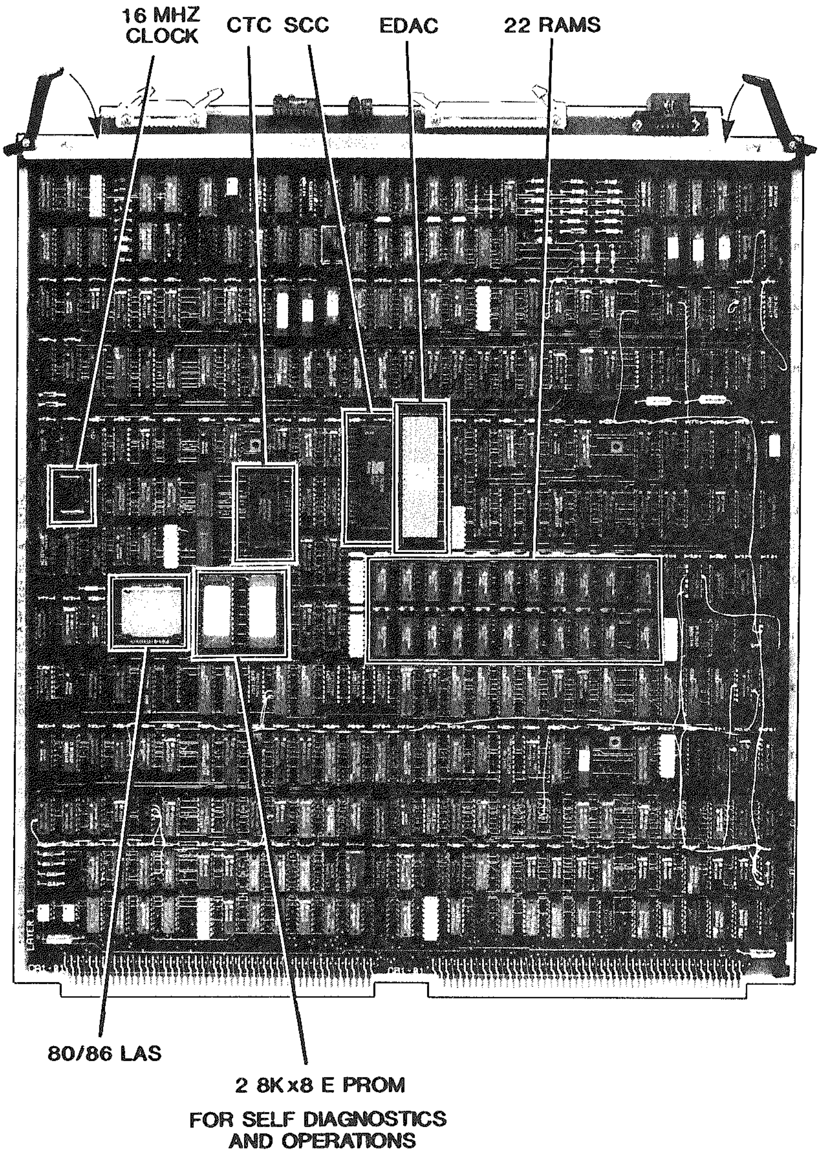


FIGURE 4-9: PNC-II BOARD LAYOUT

The 186 provides a 16 bit Address/Data bus plus four more bits of address. Two address buses are latched from this: the first provides 13 bits for the Prom and I/O Decoding, the second is shared with the DMA to provide the 9 bit address for the dynamic RAMs.

The board has three main 16 bit data buses: 186 Address/Data bus, RAM Data bus, and the I/O Data bus. The 186 Address/Data bus provides the path for all data to and from the 186 by connecting to the PROM, SCC (Serial Communications Controller), CTC (Counter Timer Circuit), both Address latches, and bidirectional buffer to the RAM Data bus.

The RAM Data bus is between the 186 Address/Data bus and the I/O Data bus. This bus has the dynamic RAMs, ECC (Error Correcting Code) chip, parity generators/checkers (for data to and from the backplane), bidirectional buffer to the 186 Address/Data bus, and bidirectional buffer to the I/O Data bus.

The I/O Data bus has all of the I/O latches and buffers used by the 186 to monitor, control, and move data to and from all peripheral devices (except the SCC and CTC). All data for the I/O Data bus must use the RAM Data bus to get to and from the 186. This arrangement of data buses allows the 186 to be fetching instructions or data from the PROM while the DMA is moving data between the RAM and network or the RAM and backplane.

The 186 and DMA Share the RAM and I/O Data buses. The DMA has priority over the 186, when the DMA requests a cycle it is granted the next RAM cycle. When the 186 requests a RAM cycle (includes all I/O except with the SCC or CTC) it will be granted the first cycle with the DMA inactive. (Note that 186 I/O to or from the DMA registers can only happen when the DMA is inactive.)

PROGRAMMABLE READ ONLY MEMORY (PROM)

Two 8K x 8 PROM chips are used to provide all the self verify and run time code needed to emulate the PNC for backward compatibility. The PROM has no support logic (except address latches) and is controlled completely by signals from the 186.

RANDOM ACCESS MEMORY (RAM)

The read/write memory space on the PNC-II is provided by 22 Dynamic RAM chips (16 data bits and 6 ECC bits) and uses ECC (Error Correcting Code) to correct single bit errors and detect multiple bit errors. A single bit error will cause an interrupt to allow for logging of the ECC syndrome bits but will have no other affect on the 186 operation. A multiple bit error is uncorrectable and will reset the controller. Total memory size is programmed into the PROMs.

The RAM has arbitration and control logic which does the following:

1. Generates a RAM cycle when requested.

2. Assigns each cycle to either the DMA or 186.

3. Generates a "false" RAM cycle for 186 I/O.

4. Controls the Ready line to the 186.

5. Provides timing and control for the Dynamic RAMs.

6. Checks for multiple bit data errors (ECC - Uncorrectable).

7. Latches and corrects single bit errors (ECC - Correctable).

8. Checks and Generates Parity for backplane data.

DIRECT MEMORY ACCESS CONTROLLER

A DMA device is provided for moving blocks of data between RAM and the network and RAM and the backplane. The DMA has eight independent channels: five for receiving from the network, one for transmitting to the network, one bidirectional to and from the backplane, and one to maintain refresh on the Dynamic RAMs. The five network receiving channels let the PNC-II receive up to five consecutive packets from the network without software intervention.

HOST BACKPLANE INTERFACE LOGIC

The hardware interface to the Prime host I/O backplane consists of two separate sections.

The first portion of the logic is the standard Prime I/O Bus Interface Logic. This circuitry has been logically reduced, and no longer uses H-series logic elements.

Address Parity checking logic has been added to provide integrity on all PIO cycles. On an Address Parity Error the hardware will ignore the PIO cycle and will drive the corresponding Address Parity Error signal on the backplane. Data Parity is maintained into and out of the controller. A Data Parity error will NOT notify the host via the Data Parity Error Signals but the 186 will stop responding to OTAs handling this as a fatal error.

The PIO & DMx logic is designed to support all operations (i.e., OTAs, INAs, OCPs, SKSs [one], DMx operation, and interrupts) necessary to implement the software interface to the host processor. This logic is a minimal hardware implementation, and so all modes, function codes, addresses, and data must be handled and processed by the microprocessor.

ZILOG COUNTER TIMER CHIP

A Zilog Z80A-CTC is provided for use as a network event counter. The four channels count Tokens, NAKs (Negative Acknowledge) received, NAKs set, and WACKs (Waited Acknowledge).

ZILOG SERIAL COMMUNICATION CIRCUIT

A Zilog SCC (8530) is used to provide a serial interface. An RS232 asynchronous line is available on channel A of the SCC to enable a terminal to plug into the PNC-II for manufacturing debug purposes.

LED DISPLAYS

Six Light-Emitting Diodes (LEDs), one green, three red, and two yellow, are mounted on the board edge to provide a visual indication of the operational status of the PNC-II and the Ring Network.

4.4.2.2.2 Functional Descriptions

This section includes information on the following topics:

- Microcode Functionality
- Self-Verify Functionality
- LED Displays
- Initialization

MICROCODE FUNCTIONALITY

The PNC-II software contained in the two 8K x 8 programmable read-only memory (PROM) circuits is referred to as the PNC-II firmware. This code performs two basic functions: backwards compatible functionality with the PNC, and self-test of the PNC-II hardware.

The PROMs main function is to emulate the PNC as the interface from the host to Ring Net.

Following power-up or receipt of an OCP '06, the PROM firmware enters the self-test section of code and then begins a series of self-tests to determine the operational status of the hardware. There are five basic self-test modules, with each being responsible for verifying the operation of a specific hardware function. The PROM, RAM, DMA, DMx, and Network Interface are tested in sequence. Status may be reported back to the host at the beginning of the down-load routine (provided the PROM tested OK).

SELF-VERIFY FUNCTIONALITY

Following power-up or the receipt of an OCP '06, the hardware is initialized, and the microprocessor executes a series of self-verification routines. First the PROM itself is tested using a checksum algorithm, and then the RAM, DMA, DMx and Network Interface are exercised. One pass of the verification takes approximately five seconds.

When the 186 begins the self verify it turns all the LEDs on. If all tests pass then the Green LED, Verify Pass, is turned on, the Red LED, Verify Fail, is turned off, and the four Network LEDs are used to display the network status. If any verify test fails, the Green LED is turned off, the Red LED, Verify Fail, is turned on, and the four network LEDs are used to display a Fail Code.

The four network status LEDs are duplicated on the MJ-Box. During self-verify and on a failure these LEDs will all be ON.

After power-up or receipt of an OCP '06 the PROM firmware executive enters the read-only memory self-test module, and performs a checksum on the contents of the PROM. If an error is detected it is displayed in the LEDs, and the 186 Halts with INAs and OTAs disabled.

The RAM portion of memory is checked via two independent procedures. The first procedure checks for data errors by first writing both logic levels (0 and 1) to every memory bit location, and then reading back the data and verifying that it is correct. The second procedure checks for addressing errors by guaranteeing that no overlapping of memory portions exists. Both of the above are first done with the EDAC, Error Detection And Correction for the RAM, disabled and then repeated with the EDAC enabled using data patterns to 1 and 0 all RAM locations used for the error checking.

The extent of DMA testing only includes verifying the internal register file and the 186's ability to read and write it. The data moving and handling is tested by the local looping of data in the network verify.

The DMx data paths are tested by looping the Put (to host) Data Fifo back into the Get (from host) Data Fifo and the OTA Data Fifo and passing data thru these to verify these data paths and parity.

The CTC is verified by setting up all four channels, bumping them N times and then reading back and verifying the returned counts.

The network logic is exercised by looping data from the transmitter back to the receiver and verifying the received data. This is done both with a loopback on board and loopback thru the J-Box. Bad CRC and bad ACK byte can be transmitted and check by the receiver.

LED DISPLAYS

The PNC-II has two LED displays of network and board status:

- The controller board has six LEDs
- The modular junction box (MJ-Box) has four LEDs

All LEDs are initialized to the ON state by hardware except the green Board Status LED which initializes OFF. If the 186 is unable to function properly then the LEDs will stay in this state indicating so. If the MJ-Box is being used, then its Network Status LEDs are all on to indicate a board failure.

Of the six on board LEDs the first two indicate the state of the controller. The other four of these LEDs are for Network Status and are Duplicated on the modular junction box (MJ-Box). These LEDs are under the complete control of the 186. They are hardware reset to a 186 fault state. Normally the Green Board Active LED (left most) will blink indicating the hardware has verified and the microprocessor is active. The controller constantly checks itself both in hardware and microcode to verify proper operation. If an uncorrectable error occurs the board will display this with the Red Board Fail LED and an error code in the remaining four LEDs. If a board failure occurs the four on board Network State LEDs are used for failure status and all MJ-Box LEDs are forced ON (an invalid combination) to indicate an uncorrectable error.

The modular junction box has three LEDs to show the network state, when used with the PNC-II, and a fourth LED showing the connect/disconnect status. When this is used with the PNC the three network LEDs are left OFF (not supported) and the fourth LED will display connect/disconnect status as on the J-Box.

INITIALIZATION

Table 4-5 summarizes PNC-II initialization events and their effect on its operation:

TABLE 4-5: PNC-II INITIALIZATION EVENTS

EVENT	RESET CONTROLLER	RESET DMx & HOST INTERRUPTS	SET 186 NMI	FIRMWARE ACTION
Power fail	yes	yes	no	Self Verify
or OCP '06	yes	yes	no	Self Verify
Master clear (SYSCLR)	no	yes	yes	Run Code
OCP '17	yes	yes	no	Run Code
Uncorrectable RAM Error	yes	yes	no	Fatal Error
Data Parity Error	no	no	yes	Fatal Error

Note: INA and OTA Ready are NOT cleared by Master Clear or OCP 17 (to support backward compatibility).

The PNC-II is described in detail in PRIMENET Node Controller Service Module (SMN601) in the Communications Service Manual (SMN600).

4.4.2.3 Asynchronous Multi-Line Controller (AMLC)

For detailed information on the AMLC board, refer to Asynchronous Multi-Line Controller Board Service Module (SMN602) in the Communications Service Manual (SMN600).

4.4.2.4 LAN300 Controller

For detailed information on the LAN300, refer to LAN300 Service Module (SMN603) in the Communications Service Manual (SMN600).

4.4.2.5 Multi-Data Link Controller (MDLC)

The MDLC is a micro programmed controller designed for synchronous communications. It replaces the High Speed Synchronous Multi-Line Controller (HSSMLC) and the original product, the Synchronous Multi-Line Controller (SMLC). The terms MDLC and SMLC are often used interchangeably.

Each system can support up to two MDLCs. Each MDLC has two cables. Each cable has:

- Two full-duplex lines that are usually connected to modems
- One protocol support, so there is a maximum of two protocols per MDLC

A protocol is a series of instructions that allow two different machines to communicate. The protocol converts the data word format of one machine into that of another. Some of the protocols available on the MDLC are:

- Bisync - IBM's version of synchronous communication, based on the EPSDIC character set
- SDLC - the protocol used specifically by the IBM8100 and 3790 series
- HDLC - the X.25 protocol with no specific character set, used by packet switching networks, such as Tymnet
- ICL7020 (U.K.)
- UT200 (CDC)
- GRTS (Honeywell)
- UNIVAC1004

The basic MDLC microcode is a 512 X 48-bit PROM. Two additional PROMs are also provided. One PROM provides a one u-step decode of the line status (data mode, buffer full, etc.) to determine the jump address. The other PROM does the same thing for the protocol, decoding special characters and some mode bits.

MDLC operation is similar to the AMLC. Each MDLC line has a Large Scale Integration (LSI) device called the USNRT. The USNRT transmitter converts data from parallel to serial. The USNRT receiver converts data from serial to parallel. Each MDLC has four USNRTs.

Parity checking (Cyclical Redundancy Check) is done with hardware rather than microcode. Eight 24-bit registers in RAM hold the current CRC accumulation for the eight data lines (4 transmit, 4 receive). An additional 8-bit register is used for shifting a character for inclusion in the CRC accumulation. A bank of 16 Exclusive-OR nodes is also used to calculate the CRC.

The I/O Data Register holds the data being transferred. The address register holds the DMA/DMC address of the data being transferred from/to the CPU.

The MDLC uses a sequence of PIO instructions to transfer data. During MDLC initialization, each line's parity, character length, and any special characters used by the protocol for transmit formatting, are sent with a series of OTA commands. Another OTA command specifies the DMA/DMC address where the data is to be transmitted from/to. On receives, two DMA/DMC addresses are specified. Then, an additional OTA command enables the transmitter and receiver.

During transmits, the MDLC fetches data from memory and stores it in a register location. The data is reformatted according to parity, character, and protocol information; then transmitted down the line. During receives, the MDLC stores data in two buffers, decodes the data, and then transmits it to the CPU on the BPD.

4.5 VCP-V DIAGNOSTIC PROCESSOR

The Diagnostic Processor (VCP-V) is a Z80A microprocessor based controller that handles general system housekeeping. The hardware/software functionality of the VCP-V is very similar to that of its predecessors, the VCP-III and VCP-IV. This includes support for a system console, user mode terminal, remote system terminal, an interface to the CPU, loadable control store support, system ID PROM, time of day clock, microdiagnostics, status panel interface, environmental sensing, and VCP functions.

The VCP-V is described in the following subsections:

- VCP-V Functional Description
- VCP-V Self-Tests and Power-Up Procedures

4.5.1 VCP-V FUNCTIONAL DESCRIPTION

The VCP-V processor is contained on a standard 15-inch board and is installed in slot DP (diagnostic processor) of the system card cage.

VCP-V functions are described in the following subsections:

- Z80 Microprocessor
- Memory
- Serial Number and Identification PROMs
- Serial Ports
- Floppy Disk Drive Interface
- On-Board Modem (domestic units only)
- Environmental Sensing Hardware
- Power Systems Support
- Soft Shut-Down

- Time of Day Clock

Figure 4-10 illustrates the functions of the VCP-V diagnostic processor.

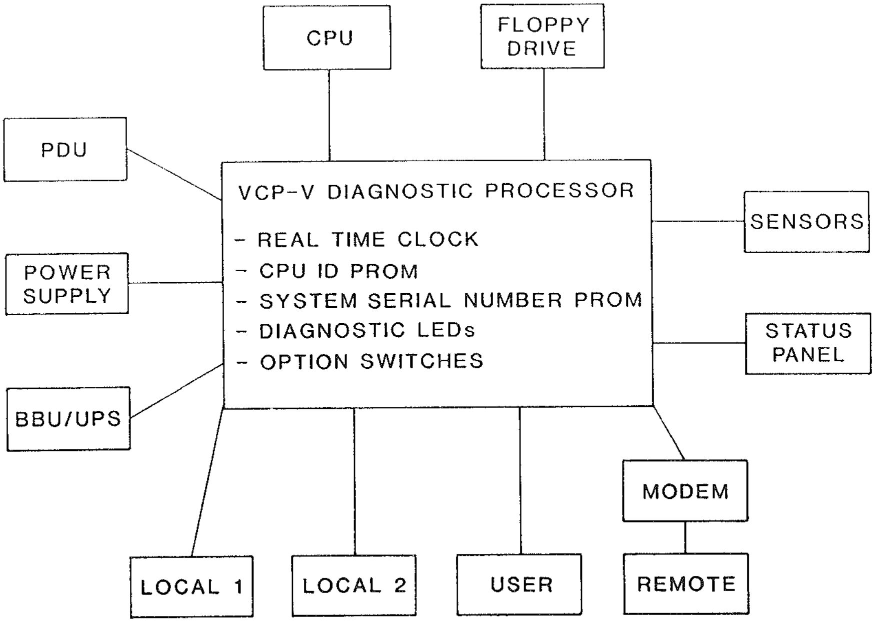


FIGURE 4-10: VCP-V BLOCK DIAGRAM

4.5.1.1 Z80 Microprocessor

The VCP-V processor contains a Z80A microprocessor operating at a 4MHz clock rate. This processor supports an 8-bit bidirectional data bus and a 16-bit unidirectional address bus. It can support up to 64KB memory and 256 I/O ports.

4.5.1.2 Memory

The VCP-V processor uses 2764 EPROMS and 8464 Static RAMS. It is configured to contain 8K of EPROM, 52K of RAM, and 4K of memory mapped I/O space. The EPROM firmware supports the self-verification and boot from floppy disk drive routines. At power-up, the Z80 executes instructions in the on-board PROM starting at address 0000H after the Z80A's reset line goes false (HIGH).

4.5.1.3 Serial Number And Identification PROMs

The VCP-V contains two 512 X 8 bit PROMs on an ID paddleboard. These PROMS contain data used to make sure that the CPU microcode corresponds to the CPU type and revision level, and to make sure that the customer is running licensed equipment. System hardware identifiers on the PROMS are then checked against descriptions contained on the floppy disk drives during system and application code loading. An unacceptable match displays an appropriate error message and terminates the verification process.

The ID paddleboard at connector J03 contains two PROMs as follows:

- Processor Description PROM
- Serial Number PROM

The Processor Description PROM contains fields identifying the CPU model number, the CPU revision level, and equipment licensing data. Information contained on this PROM is accessed by the LISTREV control panel mode command.

The System Serial Number PROM contains the unique serial number of the system for use by the Support Center during remote diagnosis. The serial number assigned to a machine does not change, even if the processor is upgraded from one type to another.

In addition, the VCP-V board contains a boot PROM with the diagnostic processor's own revision level. This information only changes with each hardware modification that requires new VCP-V code.

4.5.1.4 Serial Port Operation

The VCP-V supports four RS-232 serial ports for console or modem connections. The serial ports are as follows:

- Local 1 Port
- Local 2 Port
- Remote Port
- Spare Port

The Local 1 port has the same functionality as the system terminal port on other systems. The terminal connected to this port is used to bring the system up and down, change system configurations, and provide an operator interface to the Virtual Control Panel.

The Local 2 port is an additional system terminal port for more flexibilty in the placement of the system terminals. A terminal connected to the Local 2 port has the same functionality as a terminal connected to the Local 1 port if the Local 2 port is ENABLED and PRIVILEGED.

The remote port supplies an interface, via a modem, for a remote system terminal. A terminal connected to the remote port has the same functionality as a terminal connected to the Local 1 or Local 2 ports if the remote port is ENABLED and PRIVILEGED. The remote port can be used to access a system and run diagnostics remotely.

The spare port is a multipurpose port. The spare port is used primarily as a user mode port. This port allows the system terminal connected to the Local 1 or Local 2 ports to operate as a standard user terminal. The user mode port is connected to an asynchronous communication line via an interface cable.

4.5.1.4.1 Local 1 Port Operation

The Local 1 port provides an interface for the system console. It is RS-232 compatible and supports the Tx and Rx signals. When the system terminal is connected to the Local 1 terminal port, it should be installed close to the VCP-V processor.

When the VCP-V is in Control Panel (CP) mode and the Local 1 port is privileged the VCP-V displays the following prompt:

CP1>

The CP mode command MO ST places the VCP-V in System Terminal (ST) mode. In ST mode, the terminal connected to the Local 1 port acts as the system terminal (device '04). To return the VCP-V and terminal to CP mode, press ESC twice. The CP mode command SYSOUT INT displays messages written to device '04 Local 1 terminal. SYSOUT IGN ignores messages while in CP mode. The SYSOUT BUF command holds messages to device '04 in a buffer. When ST mode is entered, the messages are displayed.

4.5.1.4.2 Local 2 Port Operation

The Local 2 port provides an interface for a second system console. The system console need not be installed close to the VCP-V processor when connected to the Local 2 port. The Local 2 Terminal port operates similar to the Local 1 Terminal port. The following CP prompt is displayed:

CP2>

Before the Local 2 port can be used, it must be enabled and then privileged via the CP mode ENABLE and PRIVILEGE commands. An example of enabling the Local 2 port is as follows:

CP1> <u>ENABLE :2 <CR></u>

DPM901: Terminal is being enabled.

CP1>

Once the Local 2 port is enabled the VCP-V prompts the user as follows:

DPM203: Please enter password:

The user of the Local 2 port then has three tries at entering the correct password. If the user enters the incorrect password, the following message is displayed and the user is prompted to enter the password again.

DPM205: Incorrect password entered.

If 40 seconds elapse before an attempt is made to enter the password the VCP-V ignores the request to enable the port and displays the following message:

DPM908: No response for password from requested terminal.

NOTE

The -NOPASS option can be used with the ENABLE command to prevent the VCP-V from prompting for the password.

Once the Local 2 port is enabled and the correct password supplied, an operator at the Local 2 terminal can monitor the activity of the privileged system terminal port. The operator can not execute commands from the Local 2 port until the Local 2 port is privileged, as follows:

CP1> PRIV :2 <CR>

DPM905: Terminal is being privileged.

CP1>

After the Local 2 terminal has been successfully privileged the operator at that port has all rights allowed to the system console. Operators at the Local 1 and Remote terminals may only monitor system console activity at this time.

After the Local 2 port is enabled, executing the CP mode DISABLE command disables the Local 2 port. An example of using the DISABLE command follows:

CP*> DISABLE :2 <CR>

DPM902: Terminal is being disabled.

4.5.1.4.3 Remote Port Operation

The Remote port is a full Post, Telegraph and Telephone (PTT) compliant RS-232 port and supports almost any type of modem.

NOTE

The VCP-V processor supports CCITT protocol and requires the remote cable input to have the corresponding control signal active. Therefore, it is not possible to connect a cable directly from a terminal to the VCP-V remote port without going through a modem.

The remote terminal operates similar to the Local 1 and Local 2 ports. The following is displayed:

CP*>

When the VCP-V detects that a remote terminal is connected to the system via the modem it flashes the REMOTE ENABLE or the REMOTE PRIVILEGE status panel LED, or both. The condition of the status panel LEDs indicate whether the remote terminal is enabled or privileged (refer to Table 4-6). For additional information, refer to Status Panel Controls and Indicators in Chapter 3 of this manual.

TABLE 4-6: REMOTE TERMINAL LED DEFINITIONS

LED REMOTE ENABLE	LED REMOTE PRIVILEGE	REMOTE TERMINAL STATUS
OFF	OFF	Disabled/Inactive
ON	OFF	Enabled/Active
ON	ON	Enabled/Privileged
FLASHING	FLASHING	Disabled/Active
FLASHING	OFF	Enabled/Active
ON	FLASHING	Enabled/Privileged/ Active

If the remote port is enabled (either by the switch or by the command) when no remote connection exists, the VCP-V displays the following message:

DPM907: Terminal is not active.

Followed by:

DPM901: Terminal is being enabled.

When the VCP-V detects a remote connection, it issues a SYSOUT BUFF command to the CPU and stop any current system terminal output from being printed. After the port is enabled and the password entered successfully, the operator at the privileged port can execute the SYSOUT INT or MO ST commands to resume normal operation.

The remote port must be enabled and then privileged before it can be used. Enable the remote port by pressing the status panel REMOTE ENABLE switch or by executing the CP mode ENABLE command. An example of enabling the Remote port via the ENABLE command is as follows.

CP1> ENABLE ;3 <CR>

DPM901: Terminal port is being enabled.

CP1>

When the VCP-V detects that the remote terminal is connected, the following message displays:

DPM203: Please enter password:

The remote port user has three tries at entering the correct password. If the user enters the incorrect password, the following message is displayed and the user is prompted again to enter the password:

ERR205: Incorrect password entered.

If 40 seconds elapse before an attempt is made to enter the password, the VCP-V drops the Data Terminal Ready (DTR) line to disconnect the remote terminal and displays the following message:

DPM908: No response for password from requested terminal.

DPM908: No response for password from requested terminal.

NOTE

The -NOPASS option can be used with the ENABLE command to prevent the VCP-V from prompting for the password.

Once the remote port is enabled and the correct password supplied, an operator at the remote terminal can monitor the activity of the privileged system terminal port. The operator cannot execute commands until the remote port is privileged. Privilege the remote port by pressing the status panel REMOTE PRIVILEGE switch or by executing the CP mode PRIVILEGE command as follows:

CP1> <u>PRIV :3 <CR></u>

DPM905: Terminal is being privileged.

CP1>

After the remote port is successfully privileged, the operator at that terminal has all system console rights. Operators at the Local 1 and Local 2 terminals can only monitor system console activity at this time.

After the remote port is enabled, pressing the status panal REMOTE ENABLE switch or executing the CP mode DISABLE command disables the remote port and disconnects the modem if the port is active. An example of using the DISABLE command is as follows:

CP*> <u>DISABLE :3 <CR></u>

DPM902: Terminal is being disabled.

NOTE

If the remote port is privileged when either the REMOTE ENABLE or REMOTE PRIVILEGED status panel switch is pressed, the VCP-V tries to revert the privilege condition to the Local 1 port first, and then to the Local 2 port. One of these ports must be enabled to accept the privilege. If neither port is enabled the VCP-V displays the following message:

DPM910: Another terminal must be enabled to disable remote terminal.

Once another terminal is privileged, the VCP-V performs the desired action (either disabling the remote terminal or removing its privilege rights). If the action was the removal of its privilege rights, the VCP-V displays the following message:

DPM911: Terminal is being slaved.

4.5.1.4.4 Spare Port Operation

The spare port is a general purpose port. The spare port is generally used for systems that use the supervisor terminal as a user (USER mode) terminal. The CP mode command MO USER places the VCP-V into a route-through mode, where any data typed on the Local 1 privileged port is transmitted directly out the spare port and any data received at the spare port is printed on the privileged port. The spare port is usually connected to an asynchronous communication line, creating a virual connection between the privileged Local 1 port and the spare port.

After the MO USER command is executed, the operator at the spare port can login to the system, using a valid user ID, and function as a standard user. To return to system terminal mode, enter CP mode by pressing the ESC key twice and then executing the command MO ST.

NOTE

The spare port cannot be enabled, disabled, or privileged.

4.5.1.5 Floppy Disk Drive Interface

The CPU Control Store microcode and VCP-V application code are stored on floppy disk media in a floppy drive directly below the control panel. Under the control of the VCP-V, data can be transferred from the floppy drive to VCP-V or EE memory, or to the CPU Control Store.

The CPU microcode and microdiagnostic floppy diskettes are described in the paragraphs that follow.

4.5.1.5.1 CPU Microcode Diskette

The CPU microcode file is based on a double-sided diskette formatted into 35 tracks with 32 sectors per track. Each sector is comprised of 256 data bytes for a total data capacity of 286,720 bytes of data for a 40 track diskette.

When the microcode diskette is installed, the following command displays its contents on the system terminal:

```
DIR :0
```

The display is illustrated in Figure 4-11.

FILENAME	TYPE	VF	ERL	LOAD ADDRESS	START ADDRESS	LENGTH
MINK_CODE	Z	0	1	2000	000 004	AE99
RAS_CODE	U	0	3	4000	005 019	1D79
HELP	H	0	1	0000	006 017	0435
COPYRIGHT	E	0	1	8A00	006 020	00B5
CONFIG	C	0	1	0000	006 028	0201
CPU_UCODE	B	1	1	0000	006 031	2000
DECODE_NET	D	0	1	0000	017 007	3000
BOOT_CODE	P	0	1	0030	018 023	20F8
ZEROMEM	T	0	1	0200	020 025	0036
SYSV1	S	0	1	0000	020 026	1DB8
SYSV2	S	0	1	0000	030 011	1104
SYSV3	S	0	1	0000	035 026	1F51
SYSV4	S	0	1	0000	045 027	1415
SYSV5	S	0	1	0000	052 009	13A6
SYSV6	S	0	1	0000	058 019	1FE3

FIGURE 4-11: MICROCODE DISKETTE DISPLAY

The first column of the display indicates the name of each file stored on the media.

The second column (TYPE) contains a letter that indicates the type of the file. The file types are explained in Table 4-7.

TABLE 4-7: MICROCODE FILE TYPES

TYPE	EXPLANATION
Z	VCP-V Application Code
S	Sysverify Microcode
B	Base Instruction Set Microcode
D	Decode Net
E	Extension Instruction Set Microcode
M	Microdiagnostic Microcode
P	PMA Boot Code
T	T&M PMA Code
R	Required Processor Revision File
V	Microcode File Verification Copy
H	Help File Source
I	History Disk
C	Configuration File

The third column (VF) indicates to the VCP-V whether or not the file requires verification after it has been downloaded into the CPU control store. If VF is a 1, a verification file (type V) for this microcode file must exist on the diskette.

The fourth column (ERL) indicates the Engineering Level of the file.

The fifth column (LOAD ADDRESS) indicates the starting address in memory where the file is loaded. If the file is a VCP-V code file the address indicates hexidecimal bytes. If the file is a CPU microcode file the address indicates hex words.

The sixth column (START ADDRESS) indicates the starting address on the load device. The first set of three numbers indicates the decimal track number and the second set of three numbers indicates the sector number.

The last column (LENGTH) indicates the length of the file in hex bytes if it is a VCP-V code file or in hex words if it is a CPU microcode file.

4.5.1.5.2 Microdiagnostic Diskette

The microdiagnostic diskette contains the following six microdiagnostic overlays:

- UDIAG 1 - Tests CPU E-Unit jump conditions, PCU, register event counter, register program counter, address traps, and ALU modes on a slice basis.

- UDIAG 2 - Tests remaining CPU E-Unit jump conditions and BDI modes.

- UDIAG 3 - Tests CPU I-Unit data paths, cache tests and set selection, decode net, I-Unit jump conditions, and EAF logic.

- UDIAG 4 - Tests the cache miss logic, branch cache, and STLB.

- UDIAG 5 - Tests CMI-Unit data paths, memory timer, ECCC and ECCU traps.

- UDIAG 6 - Tests I/O and data paths, character hardware, decimal hardware, system timers, and parity checking.

Procedures for loading and executing microdiagnostics are described in Chapter 6 of this manual.

4.5.1.6 On-Board Modem

Diagnostic processors configured for domestic use (60Hz) are equipped with an on-board direct connect modem for use with the remote terminal.

When using the internal modem, VCP-V option switch 13 must be set ON (up) to enable the modem. A telephone jack is supplied on the board for direct connection to a telephone line.

When using an external modem, VCP-V option switch 13 must be set OFF (down). In this mode, the VCP-V monitors control lines from a connector instead of from the internal modem.

4.5.1.7 Environmental Sensing Hardware

During system operation, the VCP-V monitors environmental sensing hardware that detects increases in CPU and VCP-V board temperature, increases in the system's ambient air temperature, and loss of cabinet air flow.

The VCP-V supports the following sensors on the Model 4050/4150 system:

- Air Flow
- CPU (CMI) Board Temperature
- VCP-V Board Temperature

The air flow sensor and the CPU and VCP-V board temperature sensors are digital indicators.

The digital sensors become active when they detect either a high board temperature or an insufficient air flow. An active signal from a digital sensor triggers a system shutdown.

Except for its own board sensor, the VCP-V ignores data from board and air sensors unless the sensors are specified in the system configuration table. Each sensor entry in the configuration table contains the following data:

- A present flag to indicate that the sensor is being monitored by the VCP-V.
- A check character that indicates to PRIMOS the kind of sensor fault that has occurred.
- A timeout period that defines the length of time the VCP-V permits the system to perform an orderly shutdown before removing system power. The VCP-V treats the airflow sensor as a first level shutdown indicator. Upon detection of an active airflow sensor, the VCP-V initiates an orderly system shutdown. The board temperature sensors are treated as critical temperature indicators. Upon detection of an active board temperature sensor, the VCP-V initiates an immediate system power down.

Environmental sensors are summarized in Table 4-8:

TABLE 4-8 ENVIRONMENTAL SENSOR SUMMARY

SENSOR	TYPE	CHECK CODE	TIMEOUT
AIRSENS+C	Airflow	04	2 Minutes
BRDTEMP1-C1	CMI CPU Board	01	0 Minutes
TEMPMP	VCP-V Board	01	0 Minutes

Environmental sensing hardware is described in detail in the subsections that follow.

4.5.1.7.1 Air Flow Sensor Operation

The Model 4050/4150 system supports a single air flow sensor (AIRSENS+C). When the airflow sensor becomes active (low) and the configuration table indicates the sensor is present, the VCP-V performs the following actions:

1. Logs an error message on the History Disk.

2. Turns off all terminal input. Output to all terminals continues normally.

3. Displays the following message on the system console:

```
ERR401: Diagnostic Processor detects insufficient air flow.
        Refer to your CPU handbook.
```

4. Sends the processor check code 04 Hex to initiate a PRIMOS system shutdown.

5. Waits for the CPU to halt, or for a two-minute time period to elapse. If another sensor becomes active before the timeout expires, and that sensor has a shorter timeout period, the original two-minute time period is shortened accordingly.

6. Displays the following message on the system console:

```
WRN400: Diagnostic Processor shutting down system power.
        Refer to your CPU handbook.
```

7. Activates the OVERRIDE+ signal to the VCP-V PDU power control relay. This keeps the system from restarting with the ON/INITIATE SHUTDOWN button still in the ON position. Press the button to the INITIATE/SHUTDOWN position and then to the ON position to power up the system.

8. Turns off power to the system power supply by releasing RELAY.PICK+C to the PDU.

4.5.1.7.2 CPU Board Temperature Sensor Operation

The Model 4050/4150 supports a CPU temperature sensor. BRDTEMP1-C monitors temperatures on the CMI board. The timeout period is zero seconds.

NOTE

> Although the timeout period is zero seconds, the VCP-V still sends a check character to PRIMOS and logs an error message. During this time, PRIMOS may shutdown without data loss before the VCP-V removes power to the system.

When the CPU board temperature sensor becomes active (high) and the configuration table indicates the sensor is present, the VCP-V performs the following actions:

1. Logs an error message on the History Disk.

2. Turns off all terminal input. Output to the terminals functions normally.

3. Displays the following error message on the system console:

```
ERR405: Diagnostic Processor detects CPU board 1
        overtemperature.
        Refer to your CPU handbook.
```

4. Sends the processor check code 01 Hex to initiate a PRIMOS system shutdown.

5. Activates the OVERRIDE+ signal to the VCP-V PDU power control relay. This keeps the system from restarting with the ON/INITIATE SHUTDOWN button still in the ON position. Press the button to the INITIATE/SHUTDOWN position and then to the ON position to power up the system.

6. Turns off power to the system power supply by releasing all PHASEn+C lines to the PDU, including RELAY.PICK+C.

4.5.1.7.3 VCP-V Board Temperature Sensor

The VCP-V monitors two sensor inputs (TEMPMP) on its own board. The two sensors are daisy-chained. If either sensor becomes active, the system begins an abrupt shutdown (timeout zero seconds). Unlike the CPU board temperature and airflow sensors, the VCP-V sensors cannot be disabled by the configuration table.

NOTE

> Although the timeout period is zero seconds, the VCP-V still sends a check character to PRIMOS and logs an error message. During this time, PRIMOS may shutdown without data loss before the VCP-V removes power to the system.

When the VCP-V board temperature sensor becomes active (low), the VCP-V performs the following actions:

1. Logs an error message on the History Disk.

2. Turns off all terminal input. Output to the terminals functions normally.

3. Displays the following error messages on the system console:

```
ERR404: Diagnostic Processor detects overtemperature
        on its own board.
        Refer to your CPU handbook.
```

4. Sends the processor check code 01 Hex to initiate a PRIMOS system shutdown.

5. Activates the OVERRIDE+ signal to the VCP-V PDU power control relay. This keeps the system from restarting with the ON/INITIATE SHUTDOWN button still in the ON position. Press the button to the INITIATE/SHUTDOWN position and then to the ON position to power up

the system.

6. Turns off power to the system power supply by releasing all PHASEn+C lines to the PDU, including RELAY.PICK+C.

4.5.1.8 VCP-V Power Systems Support

The VCP-V controls and monitors the computer's entire power system. The VCP-V controls sequencing of the Power Distribution Unit, monitors and controls the Uninterruptible Power Supply (UPS) and Memory Battery Backup Unit (MBBU), monitors the system power supplies, and handles voltage margining and soft shutdown operations.

VCP-V support for the following system components and functions is described in the subsections below:

- Power Distribution Unit (PDU)
- Uninterruptible Power Supply (UPS)
- Memory Battery Backup Unit (MBBU)
- System Power Supplies
- Soft Shutdown

4.5.1.8.1 PDU Support

The Model 4050/4150 system has a two-channel PDU that distributes ac power to all system power supplies. The VCP-V uses the following control lines to drive each of the channels:

- RELAY.PICK+C - This signal is generated by the VCP-V. When TRUE (LOW), it allows the first channel of the PDU to begin supplying power to either the Memory 7778 power supply or the MBBU. Once +5 V is delivered to the VCP-V, it begins executing self-verification software, including PDU sequencing routines.

- PHASEn-C - The value of n in this signal is 4 in Model 4050/4150 systems. During PDU sequencing by the VCP-V, each control line is driven low to turn on a separate channel of the PDU and energize each system power supply. The following message is displayed on the system console during this phase of system power-up:

  DPM020: Sequencing PDU. Please wait.

When all PDU channels are sequenced, the VCP-V checks the status of each power supply by testing BBUREQ, ACLOW, and DCLOW (refer to Power Supply Support in this section for detailed descriptions of these control lines). If any power supply indicates it is not powered, the VCP-V retries the sequencing routine three times before signalling a fatal error, printing an error message, and releasing RELAY.PICK to shut down the system.

If a retry is successful, the following message is displayed on the system console:

WRN504: Retry occurred during the sequencing of the PDU.

The VCP-V then completes is self-verification tests. At any point prior to completion of self-verification, pressing the ON/INITIATE SHUTDOWN switch on the control panel releases the RELAY.PICK line and shuts down the entire system.

Once self-verification completes, the VCP-V turns on a hardware driver on the board to hold RELAY.PICK low. This permits the VCP-V to take control of power down functionality from the control panel switch. At this point, pressing the ON/INITIATE SHUTDOWN switch initiates the power-down sequence, instead of directly shutting down system power.

The VCP-V checks PDURDY-C to determine if any external PDUs are sequenced correctly. PDURDY-C is a control line connected to the PDU Out port on the last PDU in a daisy chain of cabinets. If the line is active, all PDUs are sequenced correctly. If the line is inactive, at least one PDU has failed to sequence properly. The following message is displayed on the system console:

WRN503: External PDU not responding.

4.5.1.8.2 UPS Support

The VCP-V supports an uninterruptible power supply (UPS) system through a nine-pin connector on the system bulkhead. The pinout for the D connector is listed in Table 4-9. Although the VCP-V also supports up to three Battery Backup Units (BBU A, BBU B, and BBU C), the signals for the UPS and BBU A are shared. Therefore, either a UPS or BBU A can be configured at any one time.

TABLE 4-9: UPS CONNECTOR PINOUT

SIGNAL	PIN	UPS FUNCTION
ACFAIL-C	1	UPS has lost ac input
GND	2	Ground
LOWBATA-C	3	UPS has low battery
TRKCHGA-C	4	Not Used
ONBYPASS-C	5	Not Used
FAULTA-C	6	UPS has a fault
UPSOTEMP-C	7	Not Used
HIGHCHGA-C	8	Not Used
BBUSTARTA-C	9	Not Used

The VCP-V monitors the following three inputs from the UPS: ACFAIL-C, LOWBATA-C, and FAULTA-C. Signals ACFAIL-C and LOWBATA-C must be listed in the loaded configuration table for VCP-V monitoring. The signals are defined as follows:

- ACFAIL-C - Indicates that the UPS has lost ac input. When ACFAIL-C becomes active, the UPS begins supplying power to the system. An internal counter in non-volatile memory is incremented to track the power fail (see STAT control panel command in Chapter 3 of this manual). The VCP-V then logs a message on the history disk and system console.

- LOWBATA-C - Indicates that the UPS batteries are low. The VCP-V begins a soft-shutdown sequence when this signal is active. After a five-minute timeout period, the VCP-V releases RELAY.PICK to shut off system power. If ACFAIL-C becomes inactive before LOWBATA-C becomes active, external power has returned to the system and an information message is logged on the history disk and the system console.

- FAULTA-C - Indicates that the UPS has a fault. The fault can be a shorted or open cell.

4.5.1.8.3 MBBU Support

The VCP-V supports up to three BBUs: BBU A, BBU B, and BBU C. BBU C is the Memory Battery Backup Unit (MBBU) for memory ride-through during an external power failure. Only BBU C is supported in the Model 4050/4150. Hardware support for the BBU consists of four control lines received by the VCP-V and one control line driven to the BBU.

Table 4-10 lists BBU signals and their functions.

TABLE 4-10: BBU SIGNAL DEFINITIONS

SIGNAL	BBU FUNCTION
LOWBATn-C	BBU has low battery
TRKCHGn-C	BBU in trickle charge
FAULTn-C	BBU has a fault
HIGHCHGn-C	BBU in high charge
BBUSTARTn-C	Turn on the BBU

The signals are defined as follows:

- LOWBATn-C - Indicates that the UPS batteries are low. The VCP-V begins a soft-shutdown sequence when this signal is active. After a five-minute timeout period, the VCP-V releases RELAY.PICK to shut off system power.

- TRKCHGN-C - Indicates that the BBU is in trickle charge, which means the batteries are fully charged. When this signal becomes active, the following message is displayed on the system console:

DPM501: Battery Backup Unit is in trickle charge.

- FAULTA-C - Indicates tht the BBU has a fault. The fault can be a shorted or open cell.
- HGHCHGn-C - Indicates that the BBU is in high charge, which means the batteries are not fully charged. When this signal becomes active, the following message is displayed on the system console:

  DPM500: Battery Backup Unit is in high charge.

- BBUSTARTn-C - Instructs the BBU to begin supplying power to the system. This signal indicates an external power failure. This signal is turned off when the system is recovering from a power failure.

For BBU C (Memory Battery Backup Unit), the VCP-V monitors the HGHCHGC-C and TRKCHGC-C inputs from BBU C. FAULTC-C is not monitored. The VCP-V prints an error, warning, or informational message whenever a signal line changes state. Use the STAT control panel mode command to determine the state of BBU A battery charging (high or trickle). The monitoring of these lines is not affected by the system configuration table.

The MBBU automatically turns on its battery backup when recovering from a power failure and does not received the BBUSTARTC-C signal. The low battery signal, LOWBATA-C, is monitored only when listed in the system configuration table.

The MBBU interfaces with the VCP-V through the backplane.

4.5.1.8.4 Power Supply Support

The VCP-V controls and monitors each of the system's power supplies, including Model 7778 supplies and a MBBU unit, if one is configured.

In error or informational messages that concern a power supply, the VCP-V references each power supply by number. Model 4050/4150 power supply numbering conventions are listed in Table 4-11.

TABLE 4-11: POWER SUPPLY NUMBERING CONVENTIONS

MESSAGE REFERENCE	POWER SUPPLY
Power Supply 1	MBBU
Power Supply 2	CPU 7778
Power Supply 3	I/O 7778

The VCP-V's power supply control and monitoring functions are as follows:

- Voltage Monitoring
- Power Failure Detection
- Power Failure Recovery
- Fault Detection
- Margin Control

These functions are described in the subsections that follow.

VOLTAGE MONITORING

The VCP-V supports voltage reading ports for each system power supply. An A/D converter translates the voltage into a digital number, which is compared to an ideal voltage stored in the configuration table. Use the VSENS control panel mode command to check power supply voltages (refer to CP Mode Commands in Chapter 3 of this manual for operating instructions).

The VCP-V monitors each power supply's operating voltages every 2.5 seconds. If the VCP-V detects a voltage greater or lower than the ideal voltage plus an allowable voltage difference, the system logs the following warning message on the history disk and the system console:

WRN500: Voltage out of range for power supply n.

If the VCP-V detects a normal operating voltage after a voltage warning message is issued, the system logs the following recovery message on the history disk and the system console:

DPM510: Voltage in range for power supply n.

If the VCP-V detects a voltage greater or lower than the ideal voltage plus an allowable voltage difference, the system logs an error message on the history disk and the system console, then shuts itself down by releasing all PHASEn-C lines to the PDU, including RELAY.PICK. The error message is as follows:

ERR430: Voltage critical for power supply n.

POWER FAILURE DETECTION

The VCP-V can detect an imminent power failure from different sources (i.e., a power supply or ac line voltage) by monitoring the signals BBUREQ, ACLOW, and DCLOW generated by each system power supply. The signals are defined as follows:

- BBUREQ - When active (low), BBUREQ informs the VCP-V that ac mains has failed and the VCP-V should turn on a Battery Backup Unit or Uninterruptible Power Supply, if one is available and functional. This signal is generated true 20 milliseconds before ACLO becomes true. This allows sufficient time for a BBU to begin supplying power to the system via the system power supply's high voltage dc bus.

- ACLOW - This was the HPWRFL- signal used on 1051 power supplies. ACLOW, when active (low), indicates that a power supply has lost its internal high voltage dc source.
- DCLOW - This was the HSYSCLR- signal used on the 1051 power supplies. DCLOW is active (low) when dc output voltages are below rated values, or not present. DCLOW may also become active when a fault (active temperature sensor, overvoltage condition, or overcurrent condition) is detected within the power supply.

If the VCP-V detects BBUREQ active (low), it performs the following actions:

1. Asserts then releases WPWRFL-C and CPWRFL+C to the CPU and the I/O cabinet.
2. PRIMOS suspends all disk operations. PRIMOS looks for a second power fail signal after a designated time period. If no second signal is detected, the operating system assumes that a power glitch occurred and resumes normal operation.
3. Turns on an external Battery Backup Unit (BBU), if one exists.
4. Flashes the BBU AVAILABLE LED on the control panel to indicate that the system is operating from the BBU. If no BBU exists the LED does not flash, since the system looses power first.
5. Increments the RECOVERABLE power fails counter stored in non-volatile memory to keep track of the number of times BBUREQ becomes active.

If ac power returns to the system within 20 milliseconds, causing BBUREQ to become inactive (high), the VCP-V performs the following actions:

1. Turns off the external BBU.
2. Stops flashing the BBU AVAILABLE LED.
3. Logs a recovery message on the history disk and the system console.
4. Returns to the exact state that the VCP-V was at prior to the activation of BBUREQ.

If the VCP-V detects that ACLOW has become active (low) while any BBUREQ is active, it performs the following actions:

1. Asserts then releases WPWRFL-C and CPWRFL+C to the CPU and the I/O cabinet.
2. Primos realizes that an actual power fail has occurred and begins its power fail routine to save its current state for a possible warmstart. Primos will eventually halt.
3. Increments the NON-RECOVERABLE power fails counter stored in non-volatile memory to keep track of the number of times BBUREQ

becomes active.

4. Decrements the internal counter for RECOVERABLE power failures that was incremented when BBUREQ was asserted to capture power glitches.

5. Waits for PRIMOS to halt. After the halt, the CPU Mode Lines (AMODEn+c) are set to BBU mode (000). The VCP-V then turns off the PDU's PHASEn-c lines, except RELAY.PICK.

6. Monitors the first power supply (either the MBBU or a 7778 on BBU) to determine when power returns.

7. Resequences the PDU once power returns.

If the VCP-V detects that DCLOW has become active (low) while both ACLOW and BBUREQ are active, it performs the following actions:

1. Asserts the SYSCLR line to the CPU and the I/O cabinet.

2. The CPU Mode Lines (AMODEn+c) are set to BBU mode (000). The VCP-V then turns off the PDU's PHASEn-c lines, except RELAY.PICK.

3. Monitors the first power supply (either the MBBU or a 7778 on BBU) to determine when power returns.

4. Resequences the PDU once power returns.

FAULT DETECTION

The assertion of DCLOW (loss of dc output or regulation) while BBUREQ is inactive indicates a fault in the 7778 power supply. The fault can be either overtemperature or overcurrent. The VCP-V performs the following actions:

1. Increments the FAULT counter stored in non-volatile memory to keep track of the number of times that DCLOW has been asserted.

2. Logs the following message on the history disk and on the system console:

   ERR424: Diagnostic Processor detects a fault in power supply n.

3. Waits for the CPU to halt within a designated time period (0 seconds).

4. Overrides the ON/INITIATE SHUTDOWN switch on the control panel.

5. Turns off system power by releasing all PHASEn-C lines, including RELAY.PICK

NOTE

The power failure and fault counters can be accessed by the user via the CP mode STATUS command. For more information, refer to CP Mode Commands in Chapter 3 of this manual.

POWER FAIL RECOVERY

In systems equipped with a BBU or MBBU, the VCP-V monitors the first power supply's BBUREQ control line for the return of ac power. When the power supply's BBUREQ line becomes inactive (high), the VCP-V performs the following actions:

1. Waits one second then tests BBUREQ again as a glitch detection measure. If BBUREQ is still inactive, the VCP-V continues with the power failure recovery routine. Otherwise, it continues to monitor BBUREQ.

2. Resequences the PDU.

3. Turns off all BBUs.

4. Logs a recovery message on the history disk and the system console.

5. Reloads the default configuration table from the logical device.

6. Sets the CPU Mode Lines to the correct mode.

7. Enters control panel mode.

NOTE

The VCP-V does not support automatic warmstart. The WARMSTART command must be used separately. The WARMSTART command automatically reloads the Control Store and Decode Net after a power fail.

MARGIN CONTROL

The VCP-V diagnostic processor can exercise the circuits in any system power supply through the MARGIN command. The power supply's output can be margined 5 percent high or low by this command. Margin control is useful when troubleshooting intermittent voltage-related failures in the power supply or in any device.

NOTE

You must halt the CPU before using the MARGIN command.

The syntax for the MARGIN command is as follows:

```
MARGIN [ :L  :H  :O  :N] [Supply]
```

where:

- L Option - Decreases the voltage output 5%.
- H Option - Increases the voltage output 5%.
- O Option - Turns the power supply off.
- N Option - Returns the power supply output to normal.

- Supply - Indicates the power supply number as follows: PS1 is the MBBU, PS2 is the CPU power supply, and PS3 is the I/O power supplt.

Execution of the MARGIN command causes the margin low (MARGLOWn-C) and margin high (MRGHGHn-C) signals to change. Table 4-12 is a truth table showing the state of the two signals for each option.

TABLE 4-12: MARGIN SIGNALS TRUTH TABLE

MRGHGHn-C	MARGLOWn-c	RESULT
0	0	Supply is off
0	1	5% undervoltage
1	0	5% overvoltage
1	1	Normal operation

4.5.1.9 Soft Shut-Down Support

When VCP-V detects an INITIATE SHUTDOWN request via the control panel switch it performs an orderly shutdown of PRIMOS and then shuts down the PDU, removing ac power to the system.

Pressing the INITIATE SHUTDOWN switch causes the SHTDNREQ- signal to become active (low) on the VCP-V. The soft shutdown sequence is as follows:

1. The VCP-V displays the following warning message on the system console:

   WRN401: Diagnostic Processor detects soft shutdown request.

2. Flashes the ON/INITIATE SHUTDOWN LED on the status panel to indicate that the VCP-V is shutting down the system.

3. The VCP-V sends a processor check (10 hex) to the CPU. This step occurs only if the CPU is running.

4. PRIMOS performs an LO ALL and a SH ALL to shut itself down. The VCP-V waits for the CPU to halt, or for a five minute timeout period to expire.

5. Displays the following on the system console:

   WRN400: Diagnostic Processor shutting down the system power.

6. The VCP-V releases all PHASEn-C lines to the PDU, including RELAY.PICK.

4.5.1.10 Time of Day Clock

The VCP-V diagnostic processor time of day clock is provided by a battery backed up Real Time Clock component. The component uses CMOS technology and contains 64 bytes of RAM. Fourteen bytes are used for timing functions and the other 50 are used as scratch locations. The battery is constantly trickle charged when the VCP-V diagnostic processor is powered up. When fully charged, the battery maintains the time of day clock for about 800 hours.

4.5.2 VCP-V SELF-VERIFICATION TESTS AND POWER-UP PROCEDURES

The VCP-V Diagnostic Processor performs a series of self-verification tests at power-up or when initiated by the Control Panel Mode VIRY command (refer to Control Panel Opertions Commands in Chapter 3 of this manual). Four VCP-V status LEDs identify a failing test. The self-tests performed at power-up or by the VIRY command are as follows:

- VCP-V System Memory Test
- Initial Environmental Sensors Test
- Initial System Power Supplies and PDU Sequencing Test
- Second Environmental Sensors Test
- Floppy Drive Interface Test
- System Validation Test and VCP-V Application Software Load
- Initial Time of Day Clock Test

In addition to the above tests, the VCP-V performs the following tests and procedures only at power-up. They cannot be initiated by the VIRY command. The four VCP-V status LEDs do not indicate a failure in these tests:

- System Configuration File Load
- Second System Power Supplies Test
- Time of Day Clock Test
- CPU Control Store Verification Test

VCP-V self-tests and power-up procedures are described in detail in the following subsections. Refer to VCP-V Error and Warning Messages in Chapter 6 of this manual for VCP-V self-test and power-up troubleshooting information.

4.5.2.1 VCP-V Memory Test

The VCP-V memory test is a three part test. The first part of this test verifies the contents of the Diagnostic Processor (VCP-V) PROM (VCP-V board location 25E). If the result is incorrect, the following error message is displayed on the system console and, the VCP-V halts with 0010 in the LED array.

ERR000: Diagnostic Processor memory error.
Diagnostic Processor halted.
Refer to your CPU handbook.

The second part of this test verifies the operation of the VCP-V system RAM by writing and verifying a sliding ones pattern through the RAM memory space. If an error is detected, the following message is displayed on the system console, and the VCP-V halts with 0011 in the LED array.

ERRXXX: Diagnostic Processor memory error.
Diagnostic Processor halted.
Refer to your CPU handbook.

In the above error message, XXX can have the following values denoting the failing memory component.

000	EPROM Chip Failure	25E
001	RAM Chip Failure	28E
002	RAM Chip Failure	31E
003	RAM Chip Failure	34E
004	RAM Chip Failure	37E
005	RAM Chip Failure	40E
006	RAM Chip Failure	43E
007	RAM Chip Failure	46E

The final part of this test verifies the operation of the VCP-V system RAM by writing and verifying each memory location with its address. If an error is detected the same error message as shown above is displayed and the VCP-V halts with 0100 in the LED array.

4.5.2.2 Initial Environmental Sensor Test

This is the first of two environmental sensor tests. A second test is performed after PDU sequencing and power supply tests. The VCP-V first tests its own board temperature. If temperature is normal, the VCP-V checks the next sensor. If an overtemperature is detected, the system halts with 0101 in the LED array, the following message is displayed, and the system shuts itself down:

ERR070: Diagnostic Processor detects overtemperature on its own board.
Diagnostic Processor halted.
Refer to your CPU Handbook.

The VCP-V then checks the digital temperature sensor associated with the CPU board set. The sensor is located on the CMI board. If the sensor indicates proper temperature, the self-test continues. If the sensor indicates high CPU board temperature, the system halts with 0101 in the LED array, the following message is displayed, and the system shuts itself down:

ERR073: Diagnostic Processor detects CPU A board 1 overtemperature.
Diagnostic Processor halted.
Refer to your CPU Handbook.

4.5.2.3 System Power Test

This test verifies that all power supplies in the central processor system are properly sequenced by monitoring three control lines: BBUREQ, ACLOW, AND DCLOW. If all three lines are inactive, the PDU and the two power supplies are running correctly and VCP-V self-tests continue. If one or more lines are asserted true, a power supply is generating a power fail.

The VCP-V tries three times to re-sequence the PDU. If a re-try is successful, the following message is displayed and self-verification tests continue:

WRN504: Retry occurred during the sequncing of the PDU.

If a power supply control line is still active after the third retry, the following error message is displayed and the VCP-V halts with 0110 in the LED array:

```
ERR08n: Diagnostic Processor detects a power supply failure.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.
```

In the error message, "n" indicates the number of the failing power supply.

4.5.2.4 Second Environmental Sensor Test

This is the second of two environmental sensor tests. The VCP-V first tests its own board temperature. If temperature is normal, the VCP-V checks the next sensor. If an overtemperature is detected, the system halts with 0111 in the LED array, the following message is displayed, and the system shuts itself down:

```
ERR070: Diagnostic Processor detects overtemperature on its own board.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.
```

The VCP-V then checks the two digital temperature sensors associated with the CPU board set. The sensors are located on the CMI board. If the sensor indicates proper temperature, the self-test continues. If the sensor indicates high CPU board temperature, the system halts with 0111 in the LED array, the following message is displayed, and the system shuts itself down:

```
ERR073: Diagnostic Processor detects CPU A board 1 overtemperature.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.
```

The VCP-V checks the digital air flow sensor in the main cabinet. This air flow sensor was not tested during the initial environmental test because the Model 4050/4150 blower takes about 30 seconds to reach operating speed. If the sensor indicates sufficient air flow, the VCP-V continues with its self-test. If an improper air flow is detected, the system halts with 0111 in the LED array, the following message is displayed, and the system shuts itself down:

ERR077: Diagnostic Processor detects improper air flow.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.

4.5.2.5 Floppy Disk Check Sector Test

This test reads and verifies the disk check sector of floppy drive 0, which is the default device at system power up and during execution of the VIRY command. The check sector of the disk should have the bytes numbered consecutively from 0 to 255. The check sector resides on track 34, sector 31 on 40 track drives, and track 74, sector 31 for 80 track drives.

If no errors are detected, the system continues with self-verification. If an error is detected, the VCP-V displays the following message:

ERR030: Diagnostic Processor floppy disk read error.
        Diagnostic Processor halted.
        Refer to System Operator's guide.

If the VCP-V option switches are configured for a second floppy disk drive, the following message is displayed:

WRN000: Verification continuing trying next consecutive device.

The VCP-V repeats the sector check using floppy device 01. If no errors are detected, self-verification continues. If an error is detected, the system halts with 1000 in the LED array, the following message is displayed, and the system shuts itself down:

ERR030: Diagnostic Processor floppy disk read error.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.

4.5.2.6 System Validation and VCP-V Application Software Load

This test validates the floppy drive, then reads the application software file into memory.

First, the header sector from the floppy device is read to verify that the Device Format Identifier and Required Diagnostic Processor Revision fields are valid. If a file read error or header file error is detected, the following message is displayed and the VCP-V halts with 1001 in the LED array:

ERR03x: Diagnostic Processor floppy disk read error.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.

In the above error message, decode X as follows:

1 - Nonrecoverable File Read Error

2 - Format Identifier Field Error

3 - Revision Level Field Error

If no errors occur, the VCP-V reads the Diagnostic Processor Application Software file into VCP-V memory from the floppy device. If an error is detected, the VCP-V displays an appropriate error message and halts with 1010 in the LED array. Two of the most common error messages are as follows:

```
ERR040: Diagnostic Processor floppy disk read error.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.

ERR041: Diagnostic Processor floppy disk read error.
        Diagnostic Processor halted.
        Refer to your CPU Handbook.
```

ERR040 occurs if a file read error is detected. ERR041 occurs if the Diagnostic Processor software is not found on the floppy device.

4.5.2.7 Initial Time of Day Clock Test

This test checks the Time of Day Clock's battery to make sure that it has not failed while the system was shut down. It also checks the time and date to make sure that they fall within correct bounds (e.g., March 41 is not valid). If an error is detected the following message is displayed:

```
ERR800: Diagnostic Processor time of day clock not valid.
        Date initialized to: 01 Jan 01:01:01 Sunday
```

The time and date are set to a known value so that the clock can be used as a timer by the VCP-V software.

At this point the actual self-verification of the VCP-V is complete and the following message is displayed on the system console:

```
DPM001: Diagnostic Processor Self Verification Completed.
        [Time and Date]
```

If the self-verification test was initiated by the VIRY command from CP mode, the VCP-V issues a SYSCLR command and returns to CP mode. However, if the self verification was part of the power up sequence, the VCP-V continues with the tests and procedures described in the following subsections as part of the autoboot procedure.

4.5.2.8 System Configuration File Load

This procedure loads the system configuration file off the floppy device into the VCP-V's memory. The configuration file contains an exact list of the inputs the VCP-V monitors during system operation. A configuration number stored in non-volatile memory indexes the configuration table that matches the configuration of the particular system.

The VCP-V tries to read the configuration file from the floppy device. If the file is found, the file is loaded into memory. If the file is not found, the VCP-V tests and supports only its own temperature sensor and soft shutdown mechanism. This problem should be corrected before extensive system use. The following message is logged on the history disk and displayed at the system console, and the VCP-V continues with the autoboot process:

ERR140: Configuration File not found.

Once the configuration file is located, the table number is read from non-volatile memory. If the number is outside the valid range (0-15) the following message is logged on the history disk and displayed at the system console, and the VCP-V continues withs the autoboot process:

ERR141: Invalid Configuration Table Entry.

The configuration number is then cleared to 0 to force the VCP-V to use the base configuration table. Because the base table is being used, certain specific inputs may not be monitored or supported.

NOTE

> If ERR141 occurs, load the correct configuration table using the control panel command CONFIG. Refer to Control Panel Mode Commands in Chapter 3 of this manual.

If the configuration number is valid, the correct configuration table for the particular system is loaded into the VCP-V memory, the autoboot process continues, and the following message is displayed:

DPM350: Loading Configuration Table n

If the configuration number loaded is higher than the number of tables in the file, the following message is logged on the history disk and displayed at the system console, and the VCP-V continues with the autoboot process:

ERR142: Invalid Configuration Table loaded.

If an invalid configuration table is loaded, the VCP-V tests and supports only its own temperature sensor and soft shutdown mechanism. This problem should be corrected before extensive system use.

If, during the reading of the floppy device, the VCP-V detects an incorrect match between the floppy device and the system ID PROM, the following message is logged on the history disk and and displayed at the system console, and the VCP-V continues with the autoboot process:

ERR143: Configuration Table not loaded.

If a configuration table is not loaded, the VCP-V tests and supports only its own temperature sensor and soft shutdown mechanism. This problem should be corrected before extensive system use.

4.5.2.9 Second System Power Supplies Test

Each system power supply identified in the loaded configuration table is tested for the following:

- POWER DOWN - This test checks that the power-down sequence correctly generates ACLOW and DCLOW.

- POWER UP - This test checks that the power-up sequence correctly generates ACLOW and DCLOW.
- MARGIN LOW - This test checks that margining the power supply low generates the proper voltage.
- MARGIN HIGH - This test checks that margining the power supply high generates the proper voltage.
- VOLTAGE - This test checks that the correct voltages are present when the power supply is running normally.
- PDU SEQUENCING - This test checks that the system PDU is properly sequenced.

When the System Power Supplies Test begins, the following message is displayed on the system console:

DPM021: System Power Supplies and PDU are being tested, please wait.

Each test is described in detail in the paragraphs that follow.

4.5.2.9.1 Power Down Test

Each supply in the system is tested for a proper power down sequence in the following test. A bit in a special variable in the configuration table indicates if the power supply can be powered off. This prevents the VCP-V from shutting down power to its own power supply. The power down test performs the following steps:

1. The VCP-V determines if the power supply can be powered down. If it cannot be powered off, the next power supply is tested.
2. The VCP-V turns off the power supply by asserting (low) both margin control lines to the power supply.
3. The VCP-V waits for the supply's DCLOW and ACLOW to become active (low). BBUREQ remains inactive because the supply still has ac input. If both control lines become active, the next test begins.
4. If the power supply fails to properly power down, the following message is logged on the history disk and displayed on the system console, and the system is powered down:

   ERR433: Error detected during power down sequence of power supply n.

   The value of "n" indicates the failing power supply.

4.5.2.9.2 Power Up Test

Each supply in the system is tested for a proper power up sequence in the following test. If the power supply was powered down in the previous test, the power up sequence test is performed. Otherwise, the next power supply is tested. The power up test performs the following steps:

1. The VCP-V turns on the power supply be releasing (high) both margin control lines to the power supply.

2. The VCP-V waits for the supply's DCLOW and ACLOW to become inactive (high). BBUREQ remains inactive because the supply still has ac input. If both control lines become inactive, the next test begins.

3. If the power supply fails to properly power up, the following message is logged on the history disk and displayed on the system console, and the system is powered down:

   ERR434: Error detected during power up sequence of power supply n.

   The value of "n" indicates the failing power supply.

4.5.2.9.3 Margin Low Test

Each supply in the system is tested for a proper voltage when the power supply is margined low by five percent. A bit in a special variable in the configuration table indicates in the power supply can be margined low. This prevents the VCP-V from margining power to its own power supply. The margin low test performs the following steps:

1. The VCP-V determines if the power supply can be margined. If it cannot be margined, the next power supply is tested.

2. The VCP-V margins low the power supply by asserting the margin low line and releasing the margin high control line to the power supply.

3. The actual voltage is read from the power supply and passed through the A/D converter. The actual voltage is compared to the required voltage stored in the configuration table. If the actual voltage is within ±5% of the required voltage, the next test begins.

4. If the actual voltage is within ±10% of the required voltage, the following message is displayed on the system console and logged on the history disk, and the next test begins:

   WRN502: Low Voltage out of range for power supply n
           Actual Voltage XXXX
           Required Voltage YYYY

5. If the actual voltge is beyond ±10% of the required voltage, the following message is displayed on the system console and logged on the history disk, and the system shuts itself down:

   ERR432: Low Voltage critical for power supply n
           Actual Voltage XXXX
           Required Voltage YYYY

4.5.2.9.4 Margin High Test

Each supply in the system is tested for proper voltage when the power supply is margined high by 5%. A bit in a special variable in the configuration table indicates that the power supply can be margined high, thus preventing the VCP-V from margining power to its own power supply. The margin high test performs as follows:

1. The VCP-V determines if the power supply can be margined. If it cannot be margined, the next power supply is tested.

2. The VCP-V margins high the power supply by asserting the margin high line and releasing the margin low control line to the power supply.

3. The actual voltage is read from the power supply and passed through the A/D converter. The actual voltage is compared to the required voltage stored in the configuration table. If the actual voltage is within ±5% of the required voltage, the next test begins.

4. If the actual voltage is within ±10% of the required voltage, the following message displays on the system console and logs on the history disk, and the next test begins:

```
WRN501: High Voltage out of range for power supply n
        Actual Voltage XXXX
        Required Voltage YYYY
```

5. If the actual voltage is beyond ±10% of the required voltage, the following message displays on the system console and is logged on the history disk, and the system shuts itself down:

```
ERR431: High Voltage critical for power supply n
        Actual Voltage XXXX
        Required Voltage YYYY
```

4.5.2.9.5 Voltage Test

Each supply in the system is tested for a proper voltage when the power supply is running normally. The voltage test performs as follows:

1. The VCP-V determines if the power supply is present by checking the configuration table. If it is not present, the next power supply is tested.

2. The VCP-V releases both the margin high and margin low control lines to the power supply.

3. The actual voltage is read from the power supply and passed through the A/D converter. The actual voltage is compared to the required voltage stored in the configuration table. If the actual voltage is within ±5% of the required voltage, the next test begins.

4. If the actual voltage is within ±10% of the required voltage, the following message is displayed on the system console and logged on

the history disk, and the next test begins:

WRN500: Voltage out of range for power supply n
        Actual Voltage XXXX
        Required Voltage YYYY

5. If the actual voltge is beyond $\pm 10\%$ of the required voltage, the following message is displayed on the system console and logged on the history disk, and the system shuts itself down:

ERR430: Voltage critical for power supply n
        Actual Voltage XXXX
        Required Voltage YYYY

When all power supplies are tested, the next test begins.

4.5.2.9.6 PDU Sequencing Test

When the PDU is sequenced, the last phase line activated by the VCP-V is also sent to an external PDU. All external PDUs are daisy chained together. The last PDU sends its control line back to the VCP-V, which uses the line to check if all external PDUs have sequenced.

If the VCP-V finds the signal inactive (high), the following message is logged on the history disk and displayed on the system console, and the autoboot process continues:

WRN503: External PDU not responding.

4.5.2.10 Time Of Day Clock Test

This time of day clock test makes sure the clock is actually running by checking the seconds timer against a timed loop. If the seconds counter increments within the timed loop, the clock is running and the autoboot sequence continues.

If the seconds counter does not increment, the following message is logged on the history disk and displayed on the console, and the autoboot sequence continues:

ERR800: Diagnostic Processor time of day clock not valid

4.5.2.11 CPU Control Store Test

The CPU control store test ensures that the CPU control store is operational before loading microcode images into the CPU. The test writes a known image into the control store then reads it back.

When the test begins, the following message is displayed on the system console:

DPM800: Sizing Control Store RAM.

The VCP-V first sizes the control store by writing known data to a boundary address and reading it back. The boundary between correct data and faulty data indicates the apparent control store size. If no correct data is read back, the following message is logged on the history disk and displayed on the system console.

ERR701: Can't determine the Control Store size.

The autoboot process is terminated. The following message is logged on the history disk and is displayed on the console, and the VCP-V enters control panel mode:

WRN100: Autoboot Sequence terminated, entering Control Panel Mode.

If at least one correct datum is ready back from the control store, one of the following messages is displayed, depending upon the results of the test:

DPM801: 4K control store available.

DPM802: 8K control store available.

DPM803: 16K control store available.

The VCP-V then checks the control store by writing and reading a data pattern based on the control store address. The following message is displayed during this phase of the test:

DPM807: Beginning control store address verification.

If no verification errors occur, the following message is displayed:

DPM808: Verification completed.

The autoboot then continues normally with SYSVERIFY and functional microcode loading.

If a verification error does occur, the VCP-V displays the following message on the console:

```
ERR704: Control store verification error at location.
        Data received: aaaa bbbb cccc dddd
        Data expected: eeee ffff gggg hhhh
```

The autoboot process is terminated. The following message is logged on the history disk and is displayed on the console, and the VCP-V enters control panel mode:

WRN100: Autoboot Sequence terminated, entering Control Panel Mode.

4.6 POWER DISTRIBUTION UNIT

AC power entering the mainbay and peripheral cabinets flows through a power distribution unit (PDU) to system power supplies or peripheral device power supplies. The PDUs used in the Model 4050/4150 system provide the following protection and control services:

- Cabinet-level overcurrent protection.
- EMI filtering to limit electrical interference to and from external power sources.

history disk and displayed on the system console.

ERR701: Can't determine the Control Store size.

The autoboot process is terminated. The following message is logged on the history disk and is displayed on the console, and the VCP-V enters control panel mode:

WRN100: Autoboot Sequence terminated, entering Control Panel Mode.

If at least one correct datum is ready back from the control store, one of the following messages is displayed, depending upon the results of the test:

DPM801: 4K control store available.

DPM802: 8K control store available.

DPM803: 16K control store available.

The VCP-V then checks the control store by writing and reading a data pattern based on the control store address. The following message is displayed during this phase of the test:

DPM807: Beginning control store address verification.

If no verification errors occur, the following message is displayed:

DPM808: Verification completed.

The autoboot then continues normally with SYSVERIFY and functional microcode loading.

If a verification error does occur, the VCP-V displays the following message on the console:

```
ERR704: Control store verification error at location.
        Data received: aaaa bbbb cccc dddd
        Data expected: eeee ffff gggg hhhh
```

The autoboot process is terminated. The following message is logged on the history disk and is displayed on the console, and the VCP-V enters control panel mode:

WRN100: Autoboot Sequence terminated, entering Control Panel Mode.

4.6 POWER DISTRIBUTION UNIT

AC power entering the mainbay and peripheral cabinets flows through a power distribution unit (PDU) to system power supplies or peripheral device power supplies. The PDUs used in the Model 4050/4150 system provide the following protection and control services:

- Cabinet-level overcurrent protection.
- EMI filtering to limit electrical interference to and from external power sources.

- A lamp to indicate that power is present in the PDU.
- A switch-closure to control one or more remote PDUs.
- A control interface to activate the PDU by a remote switch.
- A control interface to sequence activation of the PDU's receptacles by the VCP-V Diagnostic Processor.

Four different PDUs are used in Model 4050/4150 systems and peripheral cabinets. They are as follows.

- ESA10233-001 - Central Processor PDU (208 Vac, 60 Hz)
- ESA10233-002 - Central Processor PDU (240 Vac, 50 Hz)
- ESA10296-001 - Peripheral Cabinet PDU (120 Vac, 60 Hz)
- ESA10296-002 - Peripheral Cabinet PDU (240 Vac, 50 Hz)

The central processor and peripheral cabinet PDUs are described in the paragraphs that follow.

4.6.1 CENTRAL PROCESSOR PDU

The Central Processor PDU consists of four power receptacles, two contactors, a locking ac power inlet connector, a circuit breaker, a printed circuit board containing a power supply and power sequencing logic, an indicator lamp, a filter, and a series of signal-level interface connectors.

Power sequencing is controlled by the ON/INITIATE SHUTDOWN on the system control panel and by the VCP-V. Three of the four receptacles are switched. The fourth receptacle, used to support the optional Memory Battery Backup Unit (MBBU), is non-switched.

The mainbay PDU for domestic use accepts 208Vac (4-wire single phase). The device converts this voltage to 120Vac for use by the system's two Model TLA10113 power supplies. The power-in connector is rated at 20 amps.

The mainbay PDU for international use accepts 240Vac (single phase).

4.6.2 PERIPHERAL CABINET PDU

The peripheral cabinet PDU is similar to the mainbay unit. It also contains a circuit breaker and four recepticles for disk and tape devices.

4.7 TLA10113 POWER SUPPLIES

The Model 4050/4150 system uses two TLA10113 power supplies for its main source of power. The power supply is described in the subsections that follow:

4.7.1 SYSTEM POWER SUPPLY DESCRIPTION

The system power supply is a full-bridge ac/dc switching power supply that uses a bidirectional, full wave transformer. It is housed in slot 0 of the card cage and provides 130A current with a maximum power output of 850W (when margined to 5.25V). The outputs generated are as follows:

- +5V at 130A (max)
- +12V at 7.0A (max)
- -12V at 7.0A (max)

NOTE

> The system power supply does not provide 16V to the backplane for support of 4K and 16K dynamic RAMs (DRAMs).

The outputs are generated with safety extra low voltage (SELV) technology that prevents all power supply outputs from exceeding 30Vrms or 42.4V dc. A logical schematic of the power supply is provided in Figure 4-12.

The system power supply consists of a main power board, a control board, a boost converter board, I/O connectors, and diagnostic LEDs.

4.7.2 POWER INPUTS

The system power supply provides the following two power inputs on its front panel (shown in Figure 4-13):

- AC Input Connector
- Battery Backup Unit (BBU) Connector

4.7.2.1 AC Input Connector

The ac input connector is an IEC type connector that provides an input for ac line voltage to the power supply. The connector contains three lugs, HOT, NEUTRAL, and GROUND, and is part of the power supply line filter.

4.7.2.2 BBU Connector

The BBU connector (J9) is not used in the Model 4050/4150 system. J9 is a four-pin molex connector that is used as input from the power supplies High Voltage dc (HVDC) bus. An output and return for the BBUREQ signal is also provided on the connector. The BBU connector provides a 250 to 350 Vdc input to the HVDC bus from an optional BBU across VBUS+ and VBUS-. The BBUREQ signal is used to turn the external BBU on and off.

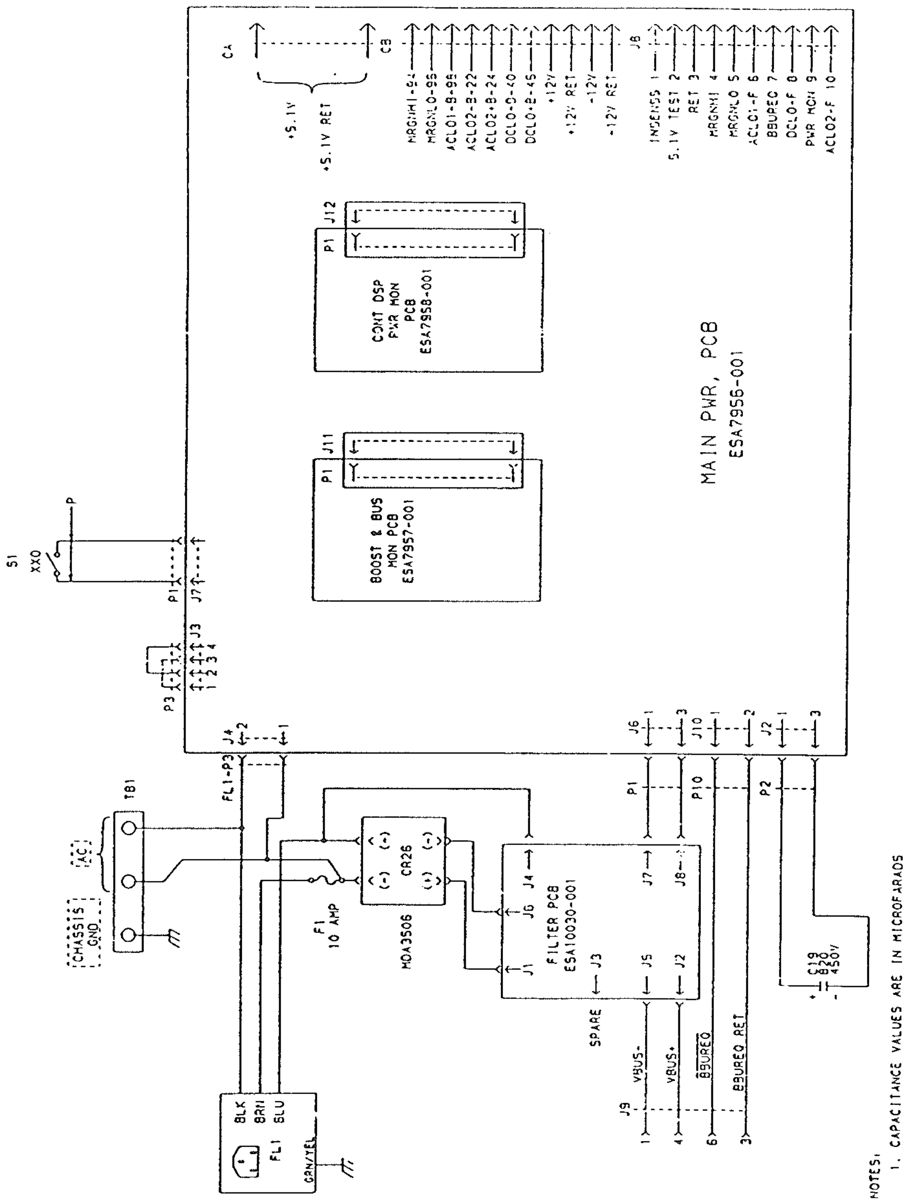


FIGURE 4-12: TLA10113 POWER SUPPLY SCHEMATIC

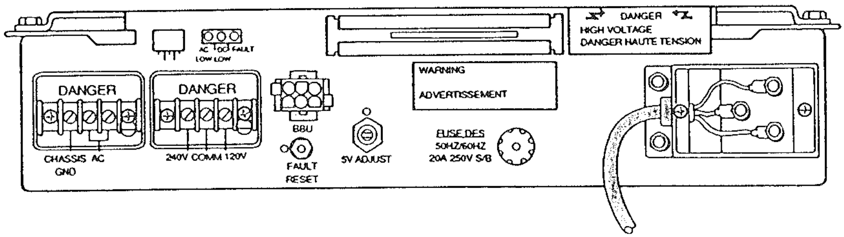


FIGURE 4-13: TLA10113 POWER SUPPLY FRONT PANEL

If the ac line voltage fails, the HVDC bus is discharged to a predetermined level causing the BBU request signal (BBUREQ) to become active (LOW). A 250 V to 350 Vdc input is then supplied to the BBU connector, providing a dc input current of 4A (at 300 Vdc) to the supply. When the ac line voltage is returned, BBUREQ becomes inactive (high) and the BBU stops supplying power to the system.

CAUTION

BBUREQ is a SELV signal and must not be connected directly to any non-SELV circuits within the BBU.

4.7.3 POWER SUPPLY FRONT PANEL CONNECTOR

The power supply front panel connector (J8) is not used in the Model 4050/4150 system. J8 provides the VCP-V with a way to monitor the power supply status via the BBUREQ, ACLO2-, and DCLO- signals. The MRGNLO- and MRGNHI- signals, which originate on the VCP-V, are received by the power supply at this connector. These signals are also present at the backplane.

	1	2	TEST5+
RET	3	4	MRGNHI-
MRGNLO-	5	6	
BBUREQ	7	8	DCLO-
	9	10	ACLO2-

4.7.4 POWER SUPPLY SIGNAL INPUTS

Two software controlled input signals can be applied to the system power supply from the VCP-V diagnostic processor through the power supply front panel connector. The two input signals are margin low (MRGNLO-) and margin high (MRGNHI-). These inputs enable the output to be modified under control of the VCP-V (see MARGIN control panel command in Chapter 3 of this manual).

This feature is useful when troubleshooting intermittent failures. Modification of the voltage output by ±5% can bring out failures on the power supply and any system board or peripheral device using the output. A description of each signal is provided in the following paragraphs:

- MRGNLO- - A TRUE (LOW) signal applied from the VCP-V diagnostic processor to this input decreases the main output voltage by 5 MRGNHI- input signal is FALSE (HIGH). If the MRGNHI- signal is also TRUE (LOW), the power supply is disabled and all power outputs are shut down. If no signal is applied, the input is internally pulled HIGH.

- MRGNHI- - A TRUE (LOW) signal also applied from the VCP-V diagnostic processor to this input increases the main output voltage by 5 the MRGNHI- input signal is FALSE (HIGH). If no signal is applied, the input is internally pulled HIGH.

4.7.5 POWER SUPPLY SIGNAL OUTPUTS

The system power supply provides status information to the VCP-V via the power supply front panel connector (J8). A description of each status signal is provided in the following paragraphs:

- BBUREQ - When active (low), BBUREQ informs the VCP-V that ac mains has failed and the VCP-V should turn on a Battery Backup Unit or Uninterruptible Power Supply, if one is available and functional. This signal is generated true 20 milliseconds before ACLOW becomes true. This allows sufficient time for a BBU to begin supplying power to the system via the system power supply's high voltage dc bus.

- ACLOW - This was the HPWRFL- signal used on 1051 power supplies. ACLOW, when active (low), indicates that a power supply has lost its internal energy.

- DCLOW - This was the HSYSCLR- signal used on the 1051 power supplies. DCLOW is active (low) when dc output voltages are below rated values, or not present. DCLOW, may also become active when a fault (active temperature sensor, overvoltage condition, or overcurrent condition) is detected within the power supply.

- TEST5 - This is an analog voltage test point, connected to the main power output. It is not monitored by the VCP-V. The signal may be used for measurement of the +5 Vdc output voltage without accessing the backplane.

4.7.6 DIAGNOSTIC LEDS

The system power supply contains four LED indicators on the front panel (see Figure 4-13). The LEDs are used to diagnose power supply voltage failures. The three green LEDs illuminate when the corresponding voltages (+5, +12, and -12V) reach their correct operating levels. They remain illuminated unless the particular voltage drops below its minimum voltage limit. The voltages each LED monitors and their minimum limits are provided in Table 4-13.

TABLE 4-13: POWER SUPPLY LED VOLTAGES

LED	Voltage/Signal Monitored	Minimum Voltage Limit
+ 5	+ 5 Vdc	+ 4.7 Vdc
+12	+12 Vdc	+11.4 Vdc
-12	-12 Vdc	-11.4 Vdc

The amber LED monitors the DCLO- signal status. It is illuminated after the power supply's dc output voltages have stabilized. The LED remains on until one or more of the power supply output voltages drop below its minimum limit, or an internal power supply fault is detected.

In addition to indicating nominal voltage, if an overcurrent condition is detected on either the +12 Vdc or -12 Vdc supply, the respective LED indicator for that voltage blinks until the overcurrent condition is removed.

4.7.7 POWER SUPPLY PROTECTION

The TLA10113 power supply contains overvoltage, overcurrent, and overtemperature protection features. A description of each is provided in the subsections that follow.

4.7.7.1 Overvoltage Protection

Overvoltage protection is provided in the power supply through a cross coupled network circuit between the +12V and -12V voltage supplies. A capacitor combination is tied between the plus (+) side of the +12V output and minus (-) side of the -12V output, and another combination of capacitors between the reference of the outputs. Whatever one side of the coupled circuit does, the other side counters by reacting in the opposite direction.

Due to the coupling between the two outputs, an out of specification voltage condition occurs when one output supply attempts to correct any fault condition.

4.7.7.2 Overcurrent Protection

All power outputs on the TLA10113 power supply provide high current which neccesitates tight limits on output current draw. The main output of the power supply is limited to 133A and auxiliary outputs are limited to 7.5A.

Overcurrent protection is provided for both outputs through three current sense transformers (T1, T2, & T3) tied into a full wavelength circuit. The following two levels of overcurrent protection are provided through this circuit:

- 132A Switch - Permanently shuts down the power supply if a fault condition is detected
- 10A Switch - Limits the duty cycle of the power supply if a fault conditon is detected during system start-up

4.7.7.3 Overtemperature Protection

A normally closed temperature sensor, set to open between 85-95 degrees C, is mounted in the +5V output rectifer heat sink. If this sensor becomes active the power supply asserts the DCLO- signal to the VCP-V diagnostic processor, indicating a fault. The VCP-V responds by shutting down the system.

4.8 FLOPPY DISK DRIVES

The Model 4050/4150 system is configured with two 5.25 inch half-height 96 Tracks Per Inch (TPI) mini-diskette drives with dual speed and dual density capability. Disk Unit 0 is used for microcode and microdiagnostic diskette support. Disk Unit 1 supports a system history disk that logs CPU events. The maximum storage capacity of each drive is 1.6 Mb.

A diskette drive functional description is provided in the following sections:

- Operating Modes
- Physical Description
- Electrical Description

4.8.1 OPERATING MODES

The drive has two modes of opertion: high density mode and normal density mode. While in high density mode, the drive has the same storage capacity as an eight-inch floppy drive. In normal density mode, the drive has the same functions as the two-sided double-density 96 TPI floppy drive.

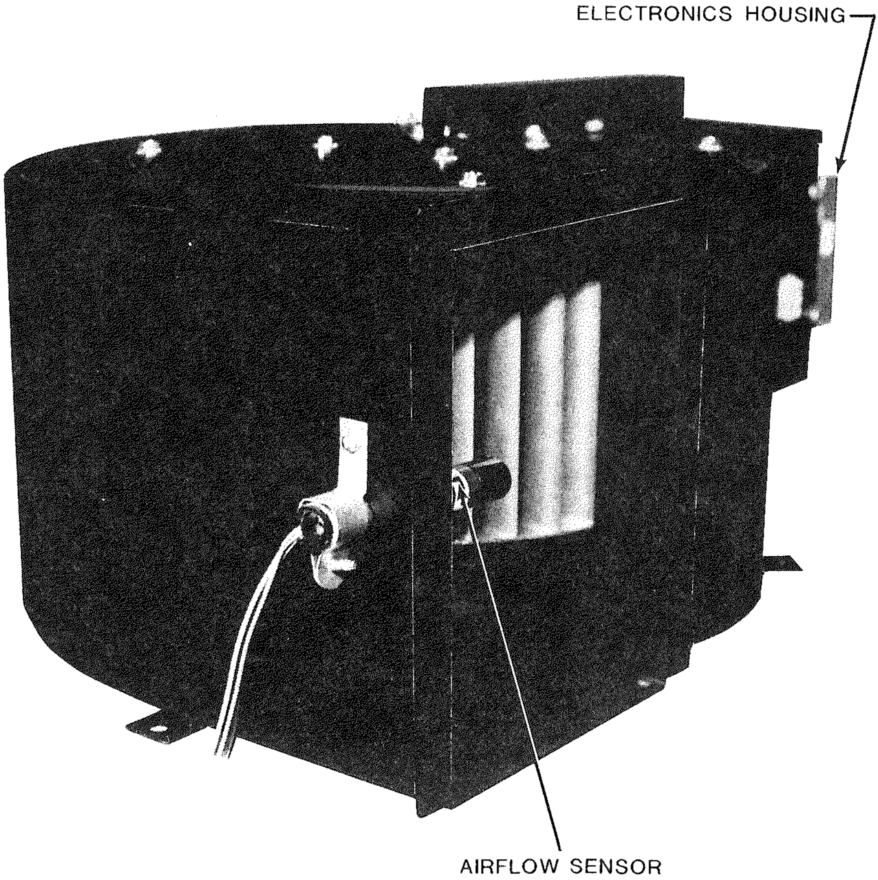


FIGURE 4-14: SYSTEM BLOWER

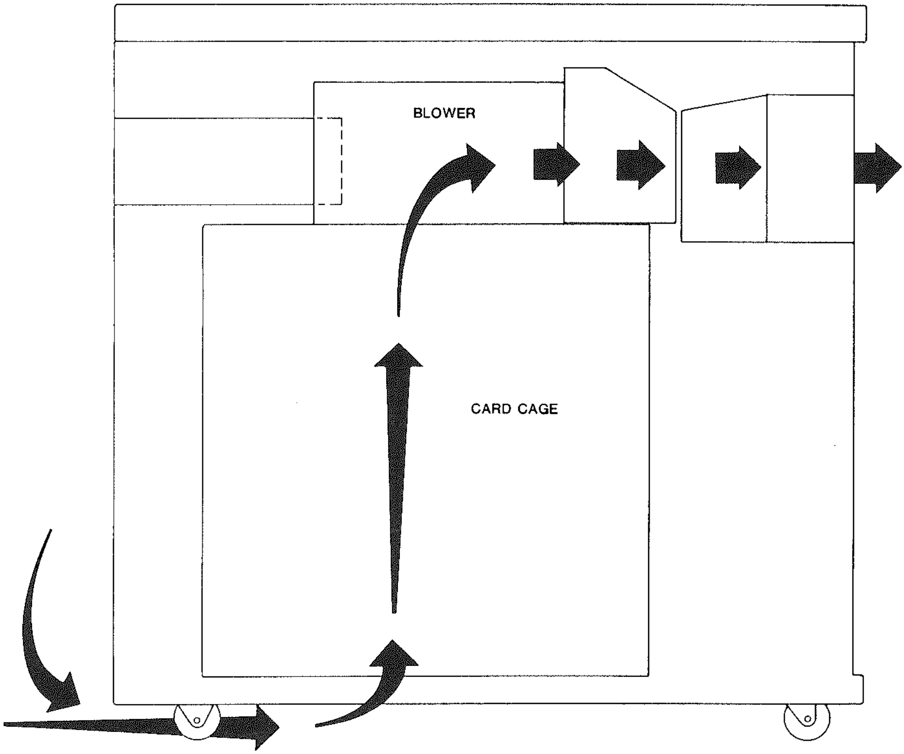


FIGURE 4-15: COOLING SYSTEM DIAGRAM

In addition to boards in the card cage, the blower system also cools Line Adapter Cards (LACs) in the Intelligent Communications Subsystem Model 3 (ICS3) card cage in mainbay installations. This eliminates the need for a separate ICS3 fan tray when the communications subsystem is installed in the Model 4050/4150 mainbay.

NOTE

> An ICS3 fan tray is required in Model 4050/4150 peripheral cabinet installations. Refer to Installing the ICS3 Card Cage in Chapter 2 of this manual for fan tray installation information.

4.9.2 BLOWER SPEED CONTROL

Blower speed is controlled by a thermal sensor connected to the drive circuitry in the drive electronics housing (see Figure 4-14). The blower can deliver a nominal air flow rate of 340 cfm with the speed control thermal sensor reading 44 degrees C.

Blower start up time from system coldstart is 30 seconds.

4.9.3 BLOWER BYPASS SWITCH

The drive circuitry is equipped with an auxiliary input to override the speed control unit. The auxiliary input is connected to the front panel bypass switch (SWT10029-001) (see Figure 4-16). The bypass switch senses when the front panel is open, which degrades system cooling efficiency.

Opening the front panel while the system is running sends an open circuit to the auxiliary input. The open circuit overrides the speed control unit and defaults the blower motor to full operating speed (340 cfm).

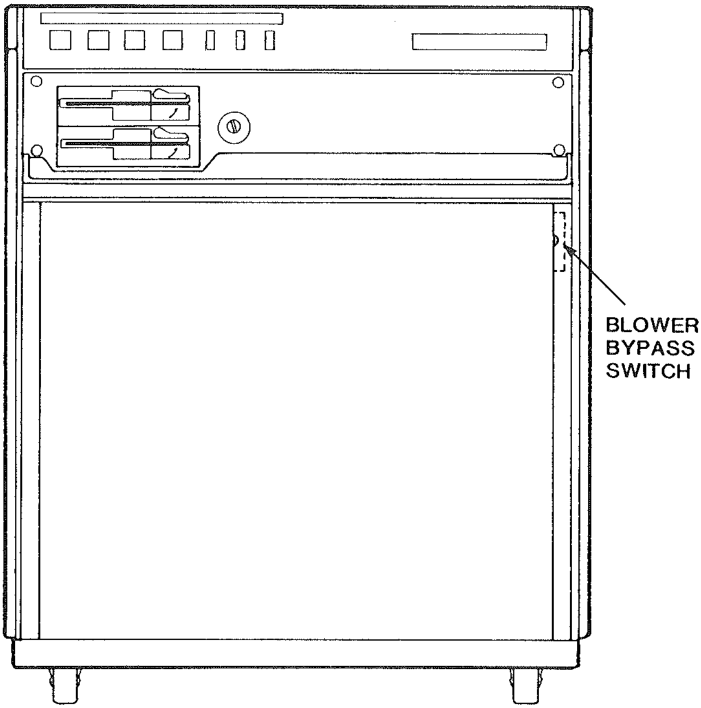


FIGURE 4-16: BLOWER BYPASS SWITCH

4.9.4 BLOWER POWER REQUIRMENTS

The blower derives its power from the CPU 7778 power supply (PS2). via the backplane. The unit operates at 24 Vdc ±5 percent. The voltage is delivered from +12 Vdc and -12 Vdc connected in series, with neutral representing the common connection between supplies.

Pin assignments for the blower power cable is shown in Table 4-15.

TABLE 4-15: BLOWER POWER CABLE PIN ASSIGNMENTS

PIN	POWER INPUT
1	+12.0 Vdc
2	Ground
3	-12.0 Vdc

4.10 UNINTERRUPTIBLE POWER SUPPLY

Prime does not currently install or support an uninterruptible power supply (UPS). However, Prime recommends the UPS as an alternative to poor electrical conditions. The customer must arrange for purchase, installation and maintenance support of a UPS.

The VCP-V provides support for the UPS facility. The VCP-V recognizes the loss of main power and subsequent UPS auxiliary backup. The VCP-V also recognizes when the UPS can no longer maintain the system and takes appropriate action.

The uninterruptible power supply (UPS) maintains ac power if a system's main power source is shut off. The UPS is normally used when the customer's power source is subject to blackouts, brownouts or power fluctuations. The UPS transforms a relatively unstable power source into a well-regulated and uninterrupted source, capable of supplying a computer with the high quality power it requires. Essentially, the UPS takes ac power from the power line, converts it to dc and then reconverts it back to ac.

The UPS consists of three major components:

- Rectifier
- Batteries
- Inverter

The rectifier converts the power line voltage to dc, thereby continually charging the batteries. The inverter converts the dc voltage back into the proper ac line voltage for the computer system. In general, the rectifier regulates all power to the system and isolates it from power fluctuation. A UPS provides uninterrupted regulated ac power, based on battery reservoir energy, to an entire system or parts of a system.

UPS operation has been integrated into Prime hardware and software. When the ac power goes down, the UPS switches to its batteries to maintain power to the system. During this transition, CPU and memory operation is not disturbed. Then the UPS notifies PRIMOS that power has been lost. PRIMOS shuts down the system in the normal manner (as if HPWRFL was detected) and waits for power to return. The CPU and memories remain powered up during the outage.

When ac power returns, the UPS notifies PRIMOS that ac power has been restored. PRIMOS generates a master clear, to initialize the CPU and controllers. A Warm Start is performed and normal processing continues. Peripheral processes will receive errors. If the outage exhausts the UPS batteries, the operator must cold start the system when power is restored.

The support capability of a single UPS is dependent on the size of the power supply and ranges from a minimum of one CPU with memory to a complete system with associated peripherals. Depending on the number and capacities of the batteries purchased, ac power backup can last from twenty minutes to several hours.

Refer to VCP-V Power Systems Support in this chapter for a description of the diagnostic processor's UPS support functionality.

4.11 DISTRIBUTED SYSTEM MANAGEMENT (DSM)

Prime's Distributed System Management (DSM) is a group of system commands and services that help manage and operate Prime systems. DSM is designed primarily for networked systems, but can be used on single-node systems. DSM allows systems to be administered from any convenient point on the network. DSM is used primarily by system administrators and senior operations staff.

DSM provides the following systems management facilities:

- Networked System Status Monitoring: System Information Metering (SIM) commands can be used to display the status of devices, communications and system resources on a network of machines. SIM produces a concise, forms-based output for terminal display or permanent storage in log files.

- Remote Systems-level Machine Control: Remote System User (RESUS) allows access to system console facilities on any machine, from any terminal on the network. DSM's own access control mechanism provides an additional level of security to protect against misuse.

- Networked Event Message Handling: DSM's Unsolicited Message Handler (UMH) directs event messages such as alarms and warnings to log files, users or assigned devices, according to preset criteria. In conjunction with DSM logging, it provides a powerful and flexible event logging mechanism that implements system and network event logging at Rev. 21.

- A Networked Message Logging Service: The DSM logging service allows messages and information from all DSM applications to be recorded in private or system logs anywhere on the network. Command-based utilities allow DSM logs throughout the network to be administered, displayed and printed on any system.

NOTE

> To use event logging, you must first install DSM. See Chapter 5 of this manual for instructions on using the DSM logs.

For detailed information on DSM, refer to the DSM USER'S GUIDE (DOC10061-1LA). The following sections provide information on the Unsolicited Message Handler (UMH).

Figure 4-17 is an example of how access to DSM facilities might be partitioned among different user groups, and shows the administrator's position in the hierarchy.

```
-------------------------------------------------------------------------
|                                                                       |
|                A D M I N I S T R A T O R                              |
|                                                                       |
-------------------------------------------------------------------------
:            |                                                          |
:            |        O P E R A T O R S                                 |
:            |                                                          |
:            ------------------------------------------------------------
:            :                                 |                        |
:            :                                 | T I M E - S H A R E    |
:            :                                 |      U S E R S         |
:            :                                 --------------------------
:            :                                 :                        :
:            :                                 :                        :
:            :                                 :                        :
:            :                                 :                        :
:            :                                 :                        :
:            :                                 :                        :
-------------------------------------------------------------------------
|            | REMOTE   |           |          |          | STATUS     |
|    DSM     | SYSTEM   |    UMH    | SYSTEM   | PRIVATE  | METERING   |
|  CONFIG'N  | USER     | CONFIG'N  | LOGGING  | LOGGING  |            |
|            | (RESUS)  |           |          |          |   (SIM)    |
-------------------------------------------------------------------------
```

FIGURE 4-17: DSM HIERARCHY

4.11.1 ADMINISTRATION AND ACCESS CONTROL

User access to DSM facilities is controlled by a networked security mechanism that operates within the following groups, as defined by the system administrator.

- Configuration Group - groups of PRIMENET nodes
- Roles - User access rights as defined by the administrator.

DSM recognizes both PRIOS user names and ACL groups.

4.11.2 UNSOLICITED MESSAGE HANDLING

The Unsolicited Message Handler (UMH) is a general, DSM-controlled facility that filters and routes event messages in a distributed environment. System administrators can distribute asynchronous messages automatically to log files, users and assignable devices throughout the configuration group.

The main use of the UMH is to handle messages such as alarms and warnings from software modules, subsystems, and applications that periodically generate systems management data. The UMH might also handle messages from software products that gather diagnostic accounting or statistical information.

4.11.3 DSM LOGGING

DSM logging service comprises a facility for logging DSM messages in private or system logs anywhere on the network, along with utilities for administering and displaying those logs.

The administrator can determine the route of all unsolicited messages by defining <u>selections</u> based on products, severities, and destinations. Unsolicited messages with no specific destination, and those that fail to be delivered are sent to two special logs.

At Rev. 21.0, PRIMOS uses UMH and DSM logging to route all system and network messages to DSM-controlled system logs on the directory DSM*>LOGS.

Using DISPLAY_LOG, you can view the contents of logs at your terminal, or write them to a disk file. Command line options allow you to select messages of a particular type, origin and severity, and display them in different formats. See Chapter 5 for details on how to access the logs.

CHAPTER 5
PREVENTIVE MAINTENANCE

This chapter contains preventive maintenance (PM) instructions and procedures for the Model 4050/4150 systems. Preventive maintenance consists of reviewing the product's history and performing certain maintenance tasks.

The Customer Service Representative (CSR) is responsible for performing the Model 4050/4150 systems preventive maintenance procedures outlined in this chapter.

Perform PM on Model 4050/4150 systems once every three months if the system is operating in a computer room environment. If the system is operating in an office environment, then perform PM on the systems once every two months.

Preventive maintenance can be divided into three major tasks:

- Reviewing the system's history, including the system logbook, the history disk, and system and network event loggers.

- Performing the actual preventive maintenance, including a routine cleaning and inspection, certain adjustments if necessary, and a final checkout

- Completing a preventive maintenance schedule form

These tasks are described in the sections that follow:

5.1 REVIEWING SYSTEM HISTORY

A product's history refers to information concerning system configuration, events, and trends in system performance. This information is available via the system logbook, history disk, and the event logger. These sources are discussed in the following subsections.

5.1.1 CHECKING THE SYSTEM LOGBOOK

The system logbook is used to report information on system status and operation. The logbook should contain the following information:

- Hardware

  - System configuration, including model and serial numbers
  - Changes to the original configuration (additions, deletions, alterations, or substitutions)
  - Changes to the operating status (failures)

- Environmental

  - Room temperature at the time of PM.
  - Abnormal temperatures
  - Unusual conditions (smoke, dust, or chemical spillage)
  - Unauthorized access to the computer room or to the system by remote login

  - Loss or damage to the equipment
  - Duration of, and any actions to correct, the above problems.

- Software

  - PRIMOS.COMI (C_PRMO) system startup file
  - CONFIG data file
  - CMNDC0 command directory contents and LIB library directory contents
  - RING0.MAP and RING3.MAP memory loadmaps
  - All shared memory segment numbers
  - Any addition, replacement, or alteration of the above

- Operations

  - System startups and shutdowns
  - Use of the FIX_DISK utility with the name of the physical device number, partition, and the results of the operation
  - Any disk formatting
  - Backups, including partition name, copy date, type of copy, and media type
  - Restoration of files or directories of the system
  - Archiving of directories

- Halts

  - System status messages
  - Startup procedure after halt
  - Functioning of system after restart

The system administrator decides what information is contained in the logbook. The system operators are responsible for entering the information. The entered information should be numbered, dated, and signed by the operator making the entry.

5.1.2 CHECKING THE HISTORY DISK

One of the two floppy disk drives in the Model 4050/4150 systems is a history disk for Customer Service use (see Figure 5-1). During normal system operation, the Diagnostic Processor prints out many error and warning messages to the system console. Some of these messages are also recorded on the history disk. Review the history disk each time a PM is performed.

The history disk contains a record of the following types of messages:

- Failure of a SYSV or UDIAG to execute
- Failure of CPU to initialize
- Power supply voltage out of specification
- Power fail conditions
- Usage of MBBU
- Temperature sensor trips
- CPU halts
- Power Shutdown requests

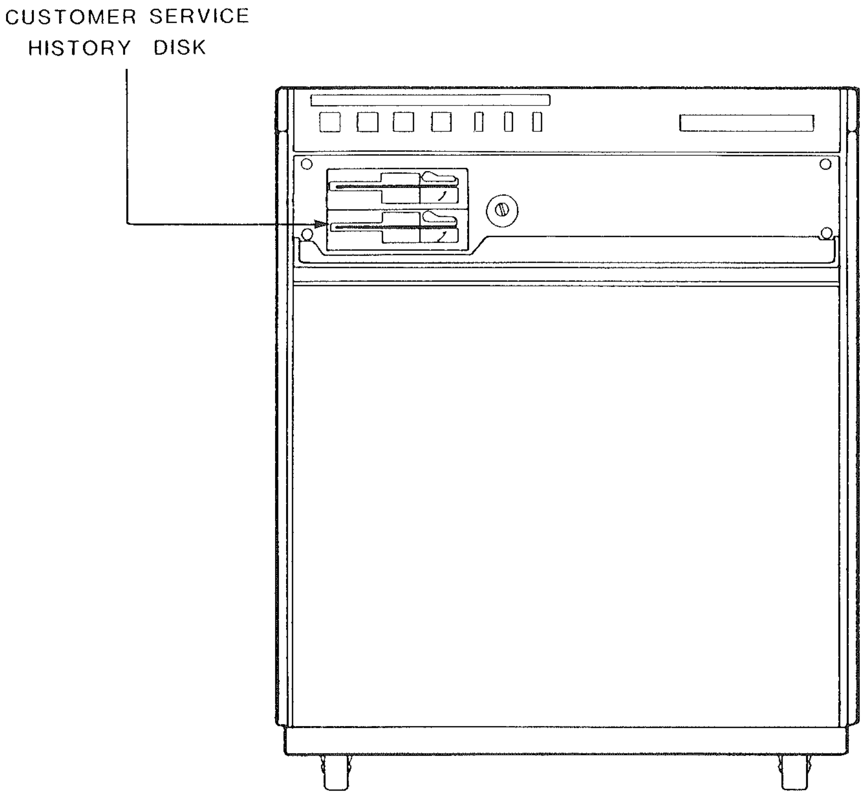


FIGURE 5-1: CUSTOMER SERVICE HISTORY DISK

NOTE

For a complete list of error and warning messages recorded on the history disk refer to System Error and Warning Messages in Chapter 6 of this manual.

Review the history disk by using the HISTORY command from the VCP-V Control Panel mode. Refer to Chapter 3 for Control Panel mode operating instructions. Using options available in the HISTORY environment, you can perform the following tasks:

- Read any valid entries anywhere on the disk
- Format a new history disk
- Add a comment for any history disk entry

By adding comments to the history disk entry, you can note the reason for a particular error, write down dates that the system was serviced, or include any pertinent comments about the system.

5.1.3 CHECKING THE EVENT LOGGERS

Event loggers record information about significant system or network events in an internal buffer. Beginning at PRIMOS Rev. 21, a new event logger, the Distributed System Management (DSM), will be implemented. Figure 5-2 provides an overview of the REV. 21 and pre-REV. 21 event loggers. The loggers are described in the sections that follow.

5.1.3.1 System Event Logger, Rev. 20.2.3

The system event logger records major system events, including cold and warm starts, machine checks, and disk read/write errors. Use one of the following two methods to enable and disable the logger:

- The CONFIG file directive, LOGREC (at system startup)

- The command, EVENT_LOG -[OFF] (when the system is running)
  -[ON]

Enabling the event logger opens a file in the UFD LOGREC*. The file name is LOG.mm/dd/yy. The mm/dd/yy represents the month, day, and year logging was enabled. The file contains a binary-encoded log of system events. The SET_QUOTA command allocates the logging file's maximum disk space.

Each time a PM is performed, examine the system log file using the PRINT_SYSLOG utility. This utility analyzes the system log file and produces a formatted output file which chronicles system events represented in the file.

Invoke the PRINT_SYSLOG utility by the command line:

```
PRINT_SYSLOG [output-filename] [options]
             [      TTY       ]
```

The output-filename names the system log output file. TTY displays the output file to the user's terminal. If either output-filename or TTY is not specified, the system output file is placed into the filename, LOGLST. A sample output file is illustrated in Figure 5-3.

EVENT LOGGERS

REV. 20.2.3 & EARLIER

REV.21

FILE NAME

REV. 20.2.3 & EARLIER:

Ø>LOGREC>LOG.mm/dd/yy
Ø>PRIMENET*>NET_LOG.mm/dd/yy

REV.21:

DSM*>LOGS>PRIMOS>LOGREC
DSM*>LOGS>NETWORKS>NETREC

NOTE: THESE ARE DEFAULT FILES. REV.21 EVENT LOGGERS ARE CONFIGURABLE BY SYS. ADMIN.

ENABLING / DISABLING

REV. 20.2.3 & EARLIER:

LOGREC (IN CONFIG FILE)
NETREC (IN CONFIG FILE)
OR, WHILE SYSTEM IS RUNNING:
EVENT_LOG [OFF]
[ON]
EVENT_LOG-NET [OFF]
[ON]

REV.21:

START_DSM (IN PRIMOS.COMI)

STOP_DSM (FROM SYSTEM TERMINAL)

REVIEWING LOGS

REV. 20.2.3 & EARLIER:

PRINT_SYSLOG [OUTPUT FILENAME]
[OPTIONS] [TTY]

PRINT_NETLOG [OUTPUT FILENAME]
[OPTIONS] [TTY]

REV.21:

DISPLAY_LOG [FILENAME]
(PRIMOS>LOGREC)
(PRIMOS>NETREC)

FIGURE 5-2: REV. 21 AND PRE-REV. 21 EVENT LOGGERS

```
***** <0>LOGREC*>LOG.09/27/87, 11:55:52 MON 28 SEP 1987 *****

08:36:00 MON 28 SEP 1987

PRIORITY ACL SET ON DISK MASTER BY USER SYSTEM (#1 )

08:37:00 MON 28 SEP 1987

PRIORITY ACL SET ON DISK INSTRT BY USER SYSTEM (#1 )

08:38:00 MON 28 SEP 1987

PRIORITY ACL SET ON DISK DATA BY USER SYSTEM (#1 )

08:39:00 MON 28 SEP 1987

PRIORITY ACL SET ON DISK PUPILS BY USER SYSTEM (#1 )

PRIORITY ACL SET ON DISK SFTWRE BY USER SYSTEM (#1 )

PRIORITY ACL SET ON DISK SFT-II BY USER SYSTEM (#1 )


TYPE   NUMBER
TIMDAT 4
PACL   6

***** END OF FILE -- 6 ENTRIES, 6 PROCESSED *****
```

FIGURE 5-3: PRINT_SYSLOG SAMPLE FILE

In the UFD LOGREC*, multiple system log input files may exist. The option, [-INPUT treename], is used with the PRINT_SYSLOG utility to select a specific system log input file. If [-INPUT treename] is not defined, the most recent log file is selected as an output file. If no system log input files exist, the PRINT_SYSLOG utility prompts for an input filename. Table 5-1 lists and defines all options available for PRINT_SYSLOG. Tables 5-2 and 5-3 lists all System Event Types and Network Event Types respectively.

TABLE 5-1: PRINT_SYSLOG AND PRINT_NETLOG OPTIONS

OPTION	DESCRIPTION*
-HELP	Prints a list of PRINT_SYSLOG options. PRINT_SYSLOG must be retyped after the options are printed.
-INPUT treename	Specifies the input log file's treename to be processed. If this option is not presented on the command line, the most recent input log file is processed.
-FROM [mmddyy] [hhmm] [TODAY]	Processes files from the specified date to the most recent date. TODAY processes the input log file with today's date. [hhmm] specifies the time of the date to be processed.
-TYPE type type...	Processes entries of the types specified. System Event types are listed in Table 5-2. Network events are listed in Table 5-3.
-SPOOL	Spools the output file after processing is complete.
-DELETE	Deletes the output file after processing is finished. This option is used only with the -SPOOL option.
-PURGE	Empties the specified event log input file when processing is complete. If the event file is the most recent input file and it is not disabled, the empty file continues to record system or network events.
-CENSUS	Totals the event types in the input file and writes the totals to an output file or user's terminal. Zero totals are not displayed.
-CONTINUE	Allows processing to continue after an illegal entry has halted PRINT_SYSLOG. The next valid entry is located to continue the process.

* For PRINT_NETLOG options, replace all PRINT_SYSLOG reference with PRINT_NETLOG.

TABLE 5-1: PRINT_SYSLOG AND PRINT_NETLOG OPTIONS (CONT.)

OPTION	DESCRIPTION*
-DEBUG	Causes PRINT_SYSLOG to read entries from the terminal and to test formatting of entry types. Each entry is entered as a series of tokens. Octal tokens are converted to binary while all others are read as ASCII strings. To exit this mode enter a Q, q, or null line.
-REMARK text	Allows text to be entered directly into the input file. The text can be 80 characters maximum and cannot be surrounded by apostrophes.
-DUMP	Processes the input file and dumps each processed entry in octal.

* For PRINT_NETLOG options, replace all PRINT_SYSLOG references with PRINT_NETLOG.

TABLE 5-2: SYSTEM EVENT TYPES

TYPE	DESCRIPTION
COLD	Cold start
WARM	Warm start
TIMDAT	Time/date entry*
CHECKS	Machine checks (including memory parity)
POWERF	Power fail checks
DISK	Disk errors
DISKNAM	ADDISK entry
OVERFL	LOGBUF overflow entry
SHUTDN	Operator shutdown
CHK300	P300 machine check
PAR300	P300 memory parity checks
MOD300	P300 missing memory module checks
TYPE10	Entry for type 10
TYPE11	Entry for type 11
TYPE12	Entry for type 12
TYPE13	Entry for type 13
TYPE14	Entry for type 14
TYPE15	Entry for type 15
QUIET	Machine check mode now quiet

*The time/date stamps associated with selected entries are not processed unless TIMDAT is explicilty selected. If TIMDAT is specified in conjunction with one or more types, only the specified alone, all time/date stamps are processed. If -TYPE option is not specified, all entries are processed.

TABLE 5-2: SYSTEM EVENT TYPES (CONT.)

TYPE	DESCRIPTION
SETIME	Operator issued a SETIME command
REMARK	Operator remark
PACL	Priority ACL set
SENSOR	Sensor check
ECCULO	User logged out due to Error Correction Code Uncorrectable (ECCU)

*The time/date stamps associated with selected entries are not processed unless TIMDAT is explicitly selected. If TIMDAT is specified in conjunction with one or more types, only the specified types' time/date is processed. If TIMDAT is specified alone, all time/date stamps are processed. If -TYPE option is not specified, all entries are processed.

5.1.3.2 Network Event Logger, Rev. 20.2.3

The network event logger records major network events, such as operator shutdowns, event buffer overflow, and out-of-sequence packets. Use one of the following two methods to enable and disable the network event logger:

- The CONFIG file directive, NETREC (at system startup)
- The command, EVENT_LOG -NET -[OFF] (when the system is
  [ON] running)

When network logging is enabled, a file is opened in the UFD PRIMENET*. The filename is NET_LOG.mm/dd/yy. The mm/dd/yy represents the month, day, and year that the logger was enabled. The SET_QUOTA command allocates the logging file's maximum disk space.

Each time a PM is performed, examine the network log file by using the PRINT_NETLOG utility. This utility analyzes the network input log file and produces a formatted output file that chronicles network events.

Invoke PRINT_NETLOG by the following command line:

```
PRINT_NETLOG [output-filename] [options]
             [      TTY       ]
```

The output-filename names the output file. If TTY is specified, the output file is displayed on the user's terminal. If the output-filename or TTY is not specified, the output is written to the file, NETLST. An output file sample is illustrated in Figure 5-4.

```
** <0>PRIMENET*>NET_LOG.09/27/87, 11:56:20 MON 28 SEP 1987 **

14:42:00 MON 28 SEP 1987

COLD START

TOKEN INSERTED INTO THE RING NETWORK

TOKEN INSERTED INTO THE RING NETWORK

15:31:12 MON 28 SEP 1987

NPX>R$CALL>R$CONN UNKNOWN CIRCUIT STATUS - NODE: 001005

      VC STATE(1): 000004
      VC STATE(2): 000372

17:30:44 MON 28 SEP 1987

CIRCUIT RESET - LOCALLY ORIGINATED - RING NODE: 1

      CIRCUIT STATE: 5

RING NODE: 1 NOT ACCEPTED XMITS. XMIT STAT IS: 020300

RING NODE: 1 NOT ACCEPTING XMITS. XMIT STAT IS: 100300
```

TYPE	NUMBER
COLD	1
TIMDAT	2
RESET	1
RING1	2
RING2	1
RING3	2
NPXCON	2

FIGURE 5-4: PRINT_NETLOG SAMPLE FILE

In the UFD PRIMENET*, multiple network log output files may exist. The option [-INPUT treename] is used with the PRINT_NETLOG utility to select a specific network log input file. If this option is not defined, the most recent log file is selected as the output file. If no network log input files exist, the PRINT_NETLOG utility prompts for an input filename. Table 5-3 defines and lists all options available for PRINT_NETLOG.

TABLE 5-3: NETWORK EVENT TYPES

TYPE	DESCRIPTION
COLD	Cold Starts
WARM	Warm Starts
TIMDAT	Time/Date Entries (see Table 5-2)
RESET	Circuit Resets
BADSEQ	Packets out of sequence
OVERFL	NETBUF overflow entries
SHUTDN	Operator Shutdowns
LPE	Local procedure errors
RING1	Tokens inserted into the ring
RING2	Ring dims out of receive blocks
RING3	Ring nodes not accepting transmits
NETDMP	NETDMP calls
SMLC1	SMLC status errors
SMLC2	SMLC--no STX preceding ETX
SMLC3	No system blocks for SMLC protocol message
SMLC4	SMLC resets
HOSTDN	Level III protocol down
PWFAIL	Power fail checks
INCREQ	Incoming call request
OUCREQ	Outgoing call request
REMARK	Operator message
NPXTHR	NPX throttled on transmit/receive
NPXRCV	NPX unexpected receiver status
NPXCLR	NPX master circuit was cleared
NPXSEQ	NPX message out of sequence
NPXCON	NPX unknown circuit status
NPXRLS	NPX bad virtual circuit clearing
RNGRCV	PNC spurious receive interrupt
RNGHRD	PNC hardware failure
RNGRES	Resource failure

5.1.3.3 Event Loggers, Rev. 21

At Rev. 21, the new PRIMOS Distributed System Management (DSM) utility handles event logging and system management. Event messages formerly logged in fixed log files under LOGREC* and PRIMENET* are now logged through DSM, via the Unsolicited Message Handler (UMH) selections LOGREC and NETREC. LOGREC and NETREC direct messages to the system logs PRIMOS>LOGREC and NETWORKS>NETREC respectively.

DSM features a single log file for system events and another for network events. Unlike pre-Rev. 21 software, where new files are opened at each coldstart, DSM appends messages to system and network files indefinitely. Both system and event logs are created with default attributes at installation.

NOTE

> PRINT_SYSLOG and PRINT_NETLOG utilities are still available under DSM, but can be used only to display pre-Rev. 21 logs.

Rev. 21 event logging information is presented in the following sections:

- Enabling/Disabling Event Logging
- Reviewing Log Files

5.1.3.3.1 Enabling and Disabling Event Logging

DSM must be installed on the customer's system before enabling the event logger. Refer to Chapter 2 of this manual for installation instructions.

The command START_DSM activates the logging of both system and network events. The STOP_DSM command deactivates system and network event logging. Chapter 3 explains the operation of these two commands.

5.1.3.3.2 Reviewing Log Files

Each time a PM is performed, examine the log file. Use the new DISPLAY_LOG command to display and print LOGREC and NETREC. This command replaces the PRINT_SYSLOG and PRINT_NETLOG commands at Rev. 21.

DISPLAY_LOG allows you to display all or part of a log at your terminal, or to write the log to a file. Figures 5-5 and 5-6 provide sample LOGREC and NETREC output files.

The format for this command is:

```
DISPLAY_LOG [input_log_file] [options]
            {-HELP}
            {-H}
            {-USAGE}
```

Except when using the -HELP and -USAGE options, you must always give an input log file name, as in the following example.

OK, <u>DISPLAY LOG PRIMOS.LOG</u> [DISPLAY_LOG Rev. 21.0 Copyright (c) 1987, Prime Computer, Inc.]

*** Message from product LOG_COLD, generated by SYSTEM on SYS6

(Severity Information, occurred at 04 Aug 87 10:48:32 Friday) COLD START PRIMOS REV 21.0 CPU TYPE = 4050 MICROCODE REV = 5 PROCESSOR ID = 000000 000000 000000 000000 (OCT)

*** Message from product LOG_MISC, generated by SYSTEM on SYS6

(Severity Information, occurred at 04 Aug 87 10:48:32 Friday) DISK MOUNT: COMDEV ON 001260 (OCT)

FIGURE 5-5: LOGREC FILE SAMPLE

```
OK, DISPLAY_LOG NETWORK.LOG
[DISPLAY_LOG Rev. 21.0 Copyright (c) 1987, Prime Computer, Inc.]

*** Message from product PRIMENET, generated by SYSTEM on SYS6
    (Severity Information, occurred at 04 Aug 87 10:48:32 Friday)
COLD START PRIMOS REV 21.0

*** Message from product LOG_MISC, generated by SYSTEM on SYS6
    (Severity Information, occurred at 04 Aug 87 10:48:32 Friday)
LEVEL III PROTOCOL DOWN - LOOP BACK
```

FIGURE 5-6: NETREC FILE SAMPLE

5.2 PERFORMING PREVENTIVE MAINTENANCE

Model 4050/4150 systems PM procedure is provided in the following subsections:

- System Shutdown
- Cleaning and Inspection
- System Adjustments
- Peripherals Maintenance
- Environmental Checkout
- System Startup

5.2.1 SYSTEM SHUTDOWN

To shut down the system prior to routine PM, follow these steps:

1. Discuss system operation with the customer/operator. Take note of any complaints.

2. Inspect the system for obvious malfunctions.

3. Verify that you have reviewed the system history disk, and spooled and reviewed the system and network event logs as described in Reviewing System History in this chapter.

4. If the system is up, have the operator bring it down.

5. Check for proper blower motor operation and airflow in the cabinets.

6. Cycle down the peripherals, then press the ON/INITIATE SHUTDOWN button on the status panel.

7. Throw the PDU circuit breaker to the OFF position (left) to remove ac power to the system, then disconnect the ac power cord from the external power source.

CAUTION

DO NOT attempt to perform the preventive maintenance operations described in this chapter with power applied to the system.

5.2.2 CLEANING AND INSPECTING MODEL 4050/4150 SYSTEMS

To properly service and maintain the Model 4050/4150 systems, perform the following tasks:

1. Verify that the system is powered down.

2. Replace the cabinet poly-foam air filters (HWD10078-001). Refer to Removing and Replacing the Air Filter in Chapter 7 of this manual for details. The filter may be used again after it is washed, dried and sprayed with filter coat.

CAUTION

Do not operate a 4050/4150 system after replacing the air filter until the air filter stop is moved into place. This stop prevents the air filter from vibrating out of place.

3. Vacuum loose dust and dirt from the insides of the cabinets.

4. Remove any visible dirt from the outside of the cabinets using a Kim-wipe dampened with household cleaner.

5. Check for loose power and cable connections.

5.2.3 MODEL 4050/4150 SYSTEMS ADJUSTMENTS

Adjustments of the Model 7778 power supplies may be required during PM. To check and adjust the 7778 power supplies, refer to Power Supply Adjustments in Chapter 6 of this manual. No other system adjustments are necessary.

5.2.4 PERIPHERALS MAINTENANCE

Clean the peripheral cabinets in the same manner as the mainbay. Refer to Table 5-4 for the appropriate Service Manual or Service Procedures Manual for specific PM and adjustments.

TABLE 5-4: INDEX OF MANUALS

DEVICE(S)	PART NUMBER
Kennedy Magnetic Tape	SMN020
Data Printer 300/600 LPM	SMN060
Printronix Model 300 Printer	SMN110
CDC 300 Mbyte SMD	SMN120
Telex 6250 BPI Tape	SMN130
NEC Spinwriter	SMN140
Dataproducts Printer 300/600 LPM	SMN160
CDC 160 Mbyte MMD	SMN170
GE Terminet 2030	SMN180

TABLE 5-4: INDEX OF MANUALS (CONT.)

DEVICE(S)	PART NUMBER
CDC 675 Mbyte FMD	SMN220
PRIME System Terminal (PST100)	SMN240
Magnetic Streaming Tape Subsystem	SMN280
300 Megabyte Fixed Module Disk	SMN320
Letter Quality Printer (3185)	SMN340
Model 6580 Intelligent Disk Controller	SMN501
770 Megabyte Fixed Storage Disk Subsystem	SPM390
4590 GCR Magnetic Tape Subsystem	SPM430
496 Megabyte Fixed Module Disk Subsystem	SPM470
Model 4587 Tape Drive (Quad-density)	SPM920

5.2.5 ENVIRONMENTAL CHECKOUT

Inspect the office or computer room for compliance with Model 4050/4150 systems environmental specifications listed in Chapter 2 of this manual. If the environment does not conform to specification, notify the customer. Upon returning to the office, notify the Branch Manager, who will follow-up with the customer to resolve the problem.

5.2.6 SYSTEM STARTUP

Once PM is completed, have the system operator bring up the machine normally. Operate all peripherals to ensure that they are working properly. If any problems arise when bringing up the system, refer to the troubleshooting procedures in Chapter 6 of this manual.

5.3 COMPLETING A PM SCHEDULE

Figure 5-7 is a sample PM schedule for a system. When used in conjunction with a similar schedule for each device, the Branch Manager can tailor and maintain the PM schedule for each system according to configuration usage and environment. The schedule is based on monthly PMs: an average usage of less than 60 hours a week power-on time (with users). The schedule can be used to record PMs for one year. Each column indicates one month.

Perform PM on Model 4050/4150 systems once every three months if the system is operating in a computer room environment. If the system is operating in an office environment, then perform PM on the systems once every two months.

All peripherals require some PM each month, if only cleaning and inspecting. The peripheral PM schedule has space for the Branch Manager to list the peripherals on a system.

Peripheral PMs can be scheduled to coincide with the Model 4050/4150 systems PMs. Performing peripheral and Model 4050/4150 systems PMs together aids in staggering the Extended (extra time required) PMs that are periodically required on each peripheral. Note the use of STD (standard) and EXT (extended) PM for this purpose on example schedule Figure 5-7.

Customer XYZ Company System SN 2345

Address 123 Main Street MA # 0678

Downtown, USA

PM TASKS	Ref[3]	CIRCLE AVG. OR HIGH[1] USAGE: Avg.	High	MONTHLY RECORD - ENTER DATE AND CHECK[2] TASKS PERFORMED: Date	Date	Date	Date	Date	Date	Date	Date	Date	Date	Date	Date	Est. Time
INSPECTION																
Check Blower Operation	5-1	1	1	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	.1 hrs
Check for System Malfunctions	5-1	1	1	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	OK	.1 hrs
CLEANING																
Vacuum Cabinets	5-2	1	1	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	DONE	.2 hrs
Clean/Replace Filters[4]	5-2	1	1	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	C/R	.2 hrs
ADJUSTMENTS																
Check Pwr Sup Voltages	6-	6	3	OK			OK			OK			OK			.2 hrs
PERIPHERAL PM SCHEDULE[5]																
MHD Unit 0 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM						Due			Due			Due			Due	
MHD Unit 1 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM					Due			Due			Due			Due		
MAG TAPE Unit 0 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM				Due		Due		Due		Due		Due		Due		
MAG TAPE Unit 1 STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM					Due		Due		Due		Due		Due		Due	
LINE PRINTER STD. PM				Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	Due	
EXT. PM				Due						Due						
Customer Service Rep. Initials																

[1] Based on usage of device, Branch Manager establishes number of months between PM TASKS (Avg. usage is 60 hrs/wk or less; high usage is more than 60 hrs/wk) by circling appropriate usage number.

[2] Circle TASKS status if problem encountered. Record data and action taken on back.

[3] References are to pages in this manual.

[4] Circle C for clean, R for replace.

[5] Branch Manager fills in this part of schedule (peripherals shown are only for example).

FIGURE 5-7: SAMPLE PM SCHEDULE

The schedule is quick and easy to complete at the site. Enter the date in the appropriate column, check off the task status for those tasks performed and initial the bottom box. If a problem is discovered, circle the task status instead of the check. Enter the date and a brief (one line) explanation of action taken on the back of the schedule.

The Branch Manager should refer to the appropriate service manuals to aid in peripheral PM scheduling.

CHAPTER 6
CORRECTIVE MAINTENANCE

This chapter is a troubleshooting guide for Model 4050/4150 Computer Systems. Figure 6-1 presents an organizational overview of Chapter 6, and suggestions on how to use the information provided in this chapter.

6.1 EVALUATING THE PROBLEM	• Use the checklist provided to collect information about the problem
6.2 PERFORMING GENERAL TROUBLESHOOTING PROCEDURES	• <u>IMPORTANT</u> Observe ESD procedures, safety procedures, and other troubleshooting routines listed in this chapter.
6.3 ISOLATING AND CORRECTING THE PROBLEM	• Use the overview flowchart to isolate a problem to the FRU level, and correct it.
6.4 TROUBLESHOOTING WITH DIAGNOSTIC MESSAGES AND LEDS	• Use console messages, diagnostic messages and LED readouts to isolate and correct the problem.
6.5 TROUBLESHOOTING WITH DIAGNOSTICS	• Use this guide to to run microdiagnostics and diagnostics on the system.

FIGURE 6-1: HOW TO USE THE TROUBLESHOOTING CHAPTER

6.1 EVALUATING THE PROBLEM

Evaluating the problem is the first step in troubleshooting. Evaluation includes the following routines:

- Checking system messages and LEDs
- Gathering information about the problem
- Categorizing the problem with the Main Troubleshooting Flowchart

6.1.1 CHECKING SYSTEM DIAGNOSTIC MESSAGES AND LEDS

Check the available system messages and diagnostic LEDs to help evaluate the problem. Also check the history disk and event logs for messages. The section on troubleshooting with messages and LEDs, later in this chapter, provides the following:

- A detailed list of diagnostic processor messages, and suggested corrective actions
- A detailed list of LED readouts and what they indicate

Refer to Troubleshooting With Diagnostic Messages and LEDs if the system console or the diagnostic LEDs of any unit in the system reports an error.

6.1.2 GATHERING INFORMATION ABOUT THE PROBLEM

Gather as much system information as possible before using the troubleshooting flowcharts. Check the following:

- Microcode revision
- PRIMOS revision
- Halt location messages or applicable failure information
- Whether or not microdiagnostics were run
- Configuration information:
  - Software:
    - PRIMOS Revision, and if modified
  - Hardware:
    - Configuration list:
      - board type
      - revision level
      - serial number
      - slot number
    - CPU microcode revision
    - Peripherals
    - Any specials

6.1.3 CATEGORIZING THE PROBLEM

Use the overview flowchart in Figure 6-2 to categorize the type of problem (i.e., power problem, memory problem, etc.). Then go to the detailed troubleshooting flowcharts, as directed, for final isolation of the faulty FRU.

6.2 PERFORMING GENERAL TROUBLESHOOTING ROUTINES

Several routine precautions must be observed to prevent damage to the system. Before troubleshooting, review the following precautions:

WARNING

Observe the routine precautions in this section to prevent equipment damage or personal injury.

- Do NOT use heat guns or freeze spray to find any bad parts. Some components run hot. Using heat guns or freeze spray may create more problems.
- Maintain adequate air flow over the CPU and memory components at all times.
- Do not run the system for more than three minutes with the front panel removed. Removing the front panel disrupts airflow to the system cardcage.
- NEVER pull boards in and out of the chassis while the power is still on. Always completely shut down the system by switching the circuit breaker on the Power Distribution Unit to the OFF position.
- Remove the system ac power cord from the external power source.
- Return all parts and boards to their original locations after the faulty part has been replaced.
- Always use an Electro Static Discharge Kit when handling any circuit board assembly.
- Always wear protective safety glasses when working on any equipment.
- If a problem persists, call the Support Center.

6.3 ISOLATING AND CORRECTING THE PROBLEM

Use the flowcharts in this section to isolate the problem to the Field Replaceable Unit (FRU). Table 6-1 is an index of the troubleshooting flowcharts, and the section in which they appear.

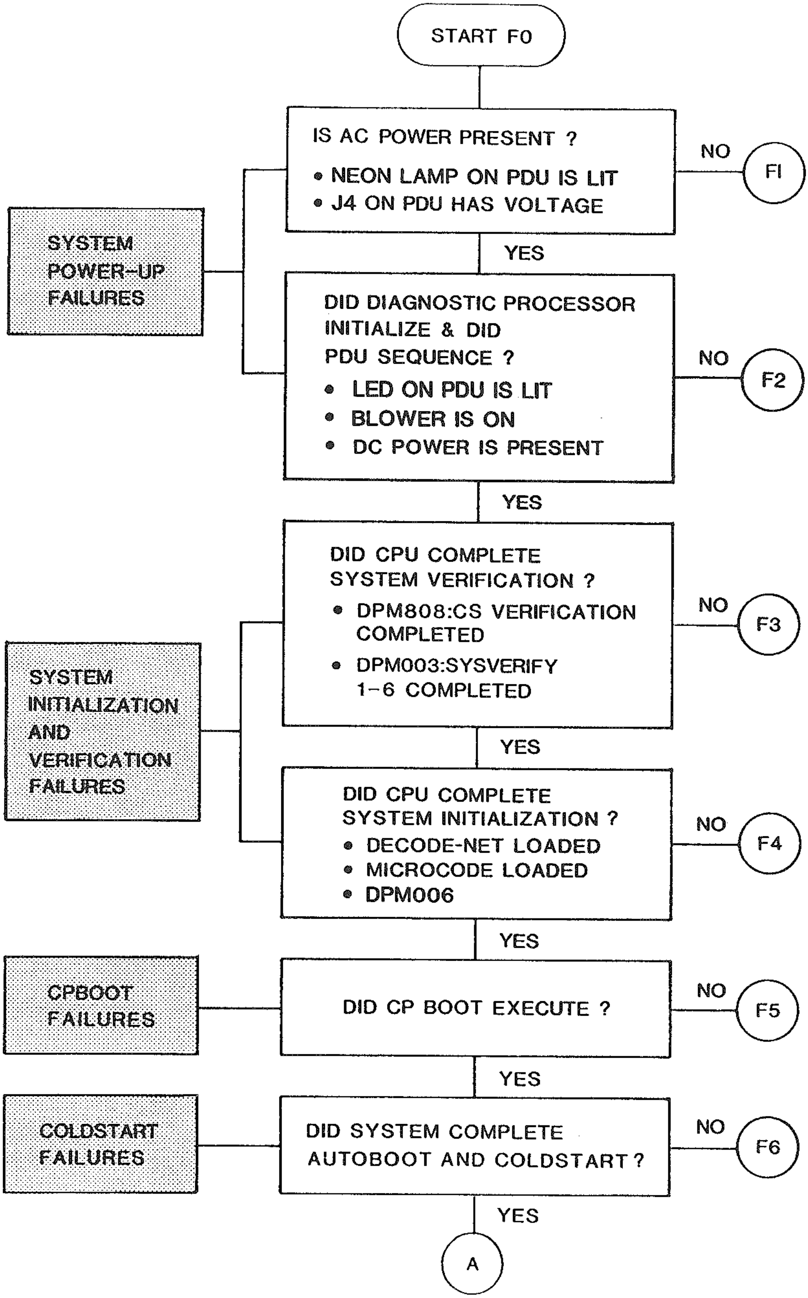


FIGURE 6-2: CATEGORIZING THE PROBLEM (F0)

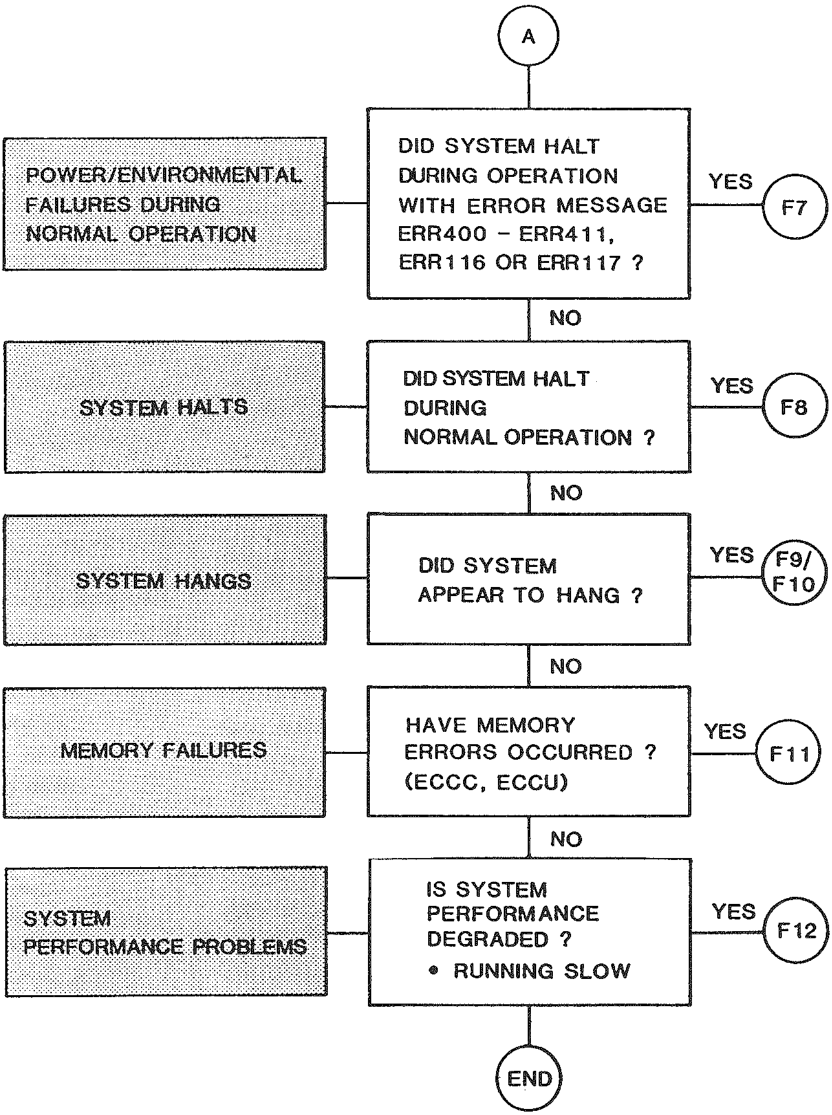


FIGURE 6-2: CATEGORIZING THE PROBLEM (F0) (CONT.)

TABLE 6-1: TROUBLESHOOTING FLOWCHART INDEX

FLOWCHART	DESCRIPTION	SECTION	FIGURE
F0	Categorizing the Problem	6.1.3	6-2
F1	AC Power Problems	6.3.1	6-3
F2	Power-up Problems	6.3.1	6-4
F3	CPU Verification Failure	6.3.2	6-7
F4	CPU Initialization Failure	6.3.2	6-8
F5	CPBOOT Failures	6.3.3	6-9
F6	Coldstart Failures	6.3.3	6-10
F7	Power/Environmental/VCP Failures	6.3.4	6-11
F8	System Halts	6.3.5	6-12
F8-A	Isolating System Halts	6.3.5	6-13
F9	System Hangs	6.3.6	6-14
F10	Determining the System Is Hung	6.3.6	6-15
F11	Memory Problems	6.3.7	6-16
F12-A	Slow System Flowchart A	6.3.9	6-22
F12-B	Slow System Flowchart B	6.3.9	6-23
F12-C	Slow System Flowchart C	6.3.9	6-24

6.3.1 TROUBLESHOOTING POWER-UP FAILURES

The Model 4050/4150 power-up sequence consists of two stages:

1. Standby State: when the main ac circuit breaker is on, ac power is applied to the PDU and ac voltage is present at the BBU outlet.

2. PDU Sequencing: when the ON/INITIATE SHUTDOWN button on the front panel is depressed, PDU sequencing begins under control of the Diagnostic Processor (VCP-V).

Included in this section are the following troubleshooting flowcharts and procedures:

- AC Power Problems Flowchart
- Power-Up Sequence Problems Flowchart
- Verifying AC Mains Voltages
- Measuring Backplane Voltages

NOTE

> When troubleshooting system power problems, complete the steps in flowchart F1 first to verify proper ac voltages at the site, proper operation of the ac power cable, and correct operation of the PDU relays. If F1 fails to locate the problem, complete the steps in F2.

6.3.1.1 AC Power Problems

When the ac circuit breaker is turned on, the NEON light on the PDU should come on and remain on, indicating that the PDU is in a standby state. A failure could be caused by a building power problem, a faulty power cord, or a bad PDU. Refer to Figure 6-3 and Table 6-2 if the system ac fails to power up to a standby state.

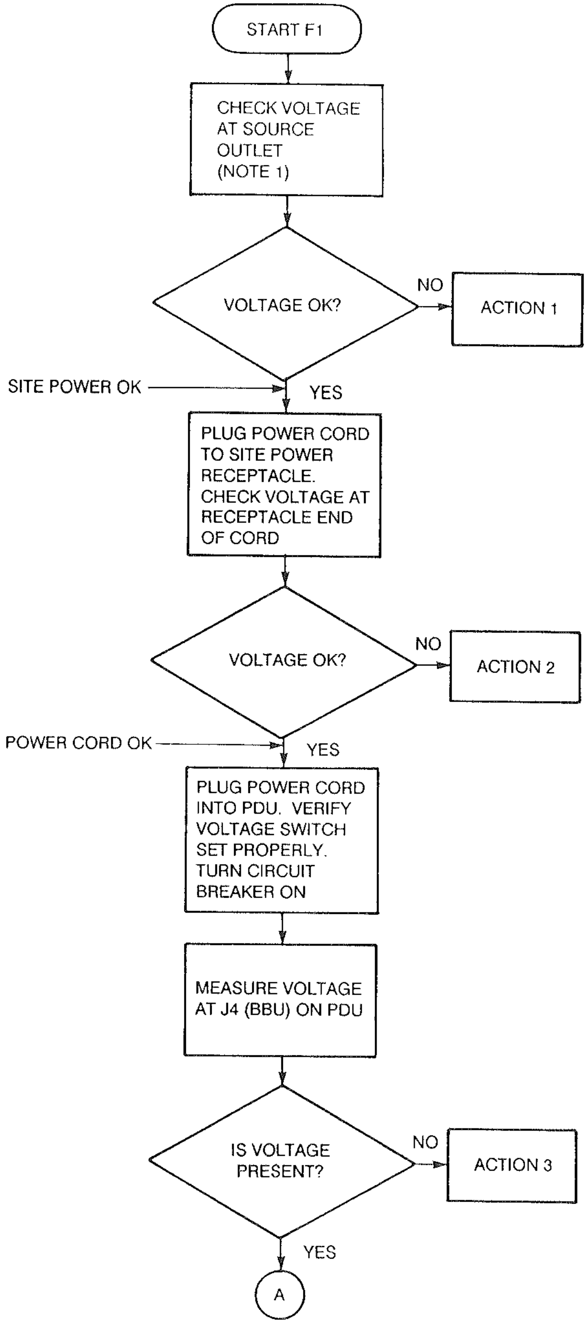


FIGURE 6-3: AC POWER PROBLEMS FLOWCHART (F1)

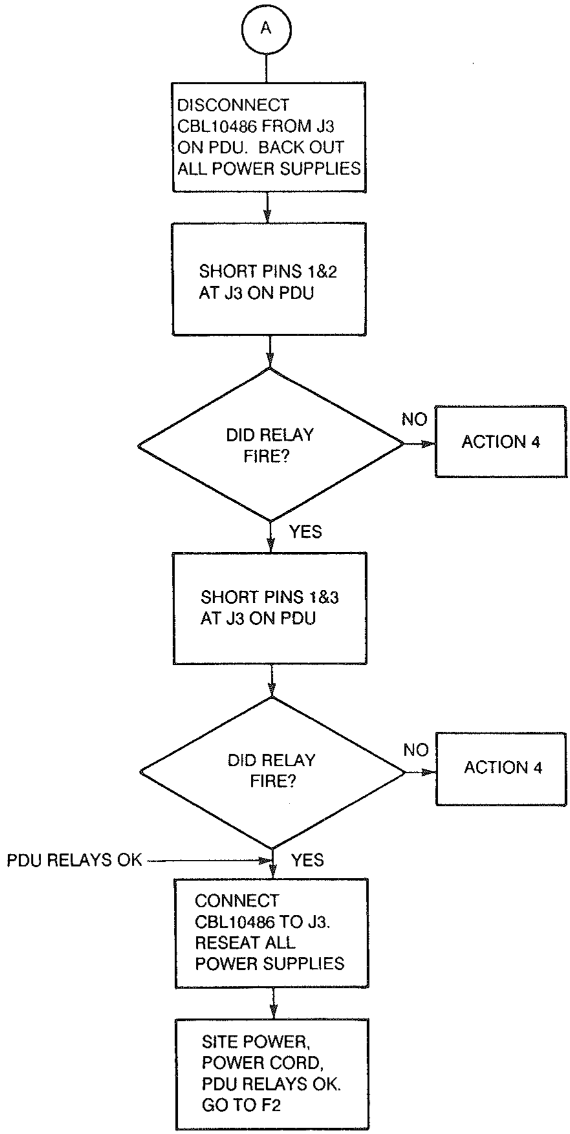


FIGURE 6-3: AC POWER PROBLEMS FLOWCHART (F1) (CONT.)

NOTE

Failure of the PDU NEON light was detected in some early shipments.

TABLE 6-2: AC POWER PROBLEMS (F1)

CONDITIONS	
1. The PDU indicator is off. 2. No LEDs on the status panel. 3. No data on the system console. 4. Blower not on.	
ACTIONS	**NOTES**
1. Suspect the incoming ac power at the site. Notify the customer. 2. Replace ac power cable. 3. Check PDU internal fuse. If the fuse is ok, replace the PDU. 4. Replace the PDU.	1. Domestic Installations should measure between 156 and 228 Vac phase-to-phase; 120 Vac (nominal) between Hot and Ground, and 0 Vac between Ground and Neutral. International installations should measure between 208 and 254 Vac between Hot and Neutral; between 208 and 254 Vac between Hot and Ground, and 0 Vac between Ground and Neutral. Refer to "Verifying the AC Mains Voltage" in this chapter for a verification procedure.

6.3.1.2 Power-Up Sequence Problems

During the power-up sequence, the Diagnostic Processor (VCP-V) tests and initializes itself, checks system power supplies, and sequences the PDU.

Failure of this sequence to execute can be traced to the status panel, the VCP-V/PDU/status panel interface cable, the VCP-V, a 7778 power supply, the MBBU, or the power shunt board. Refer to Figure 6-4 and Table 6-3 if the power-up sequence does not complete.

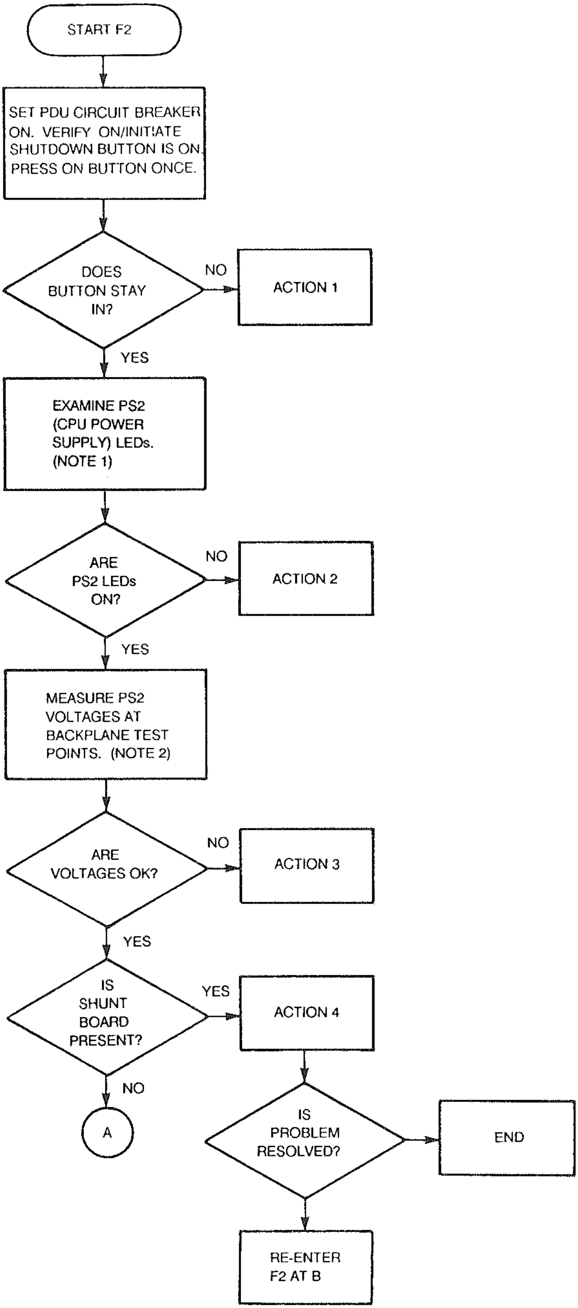


FIGURE 6-4: POWER UP PROBLEMS FLOWCHART (F2)

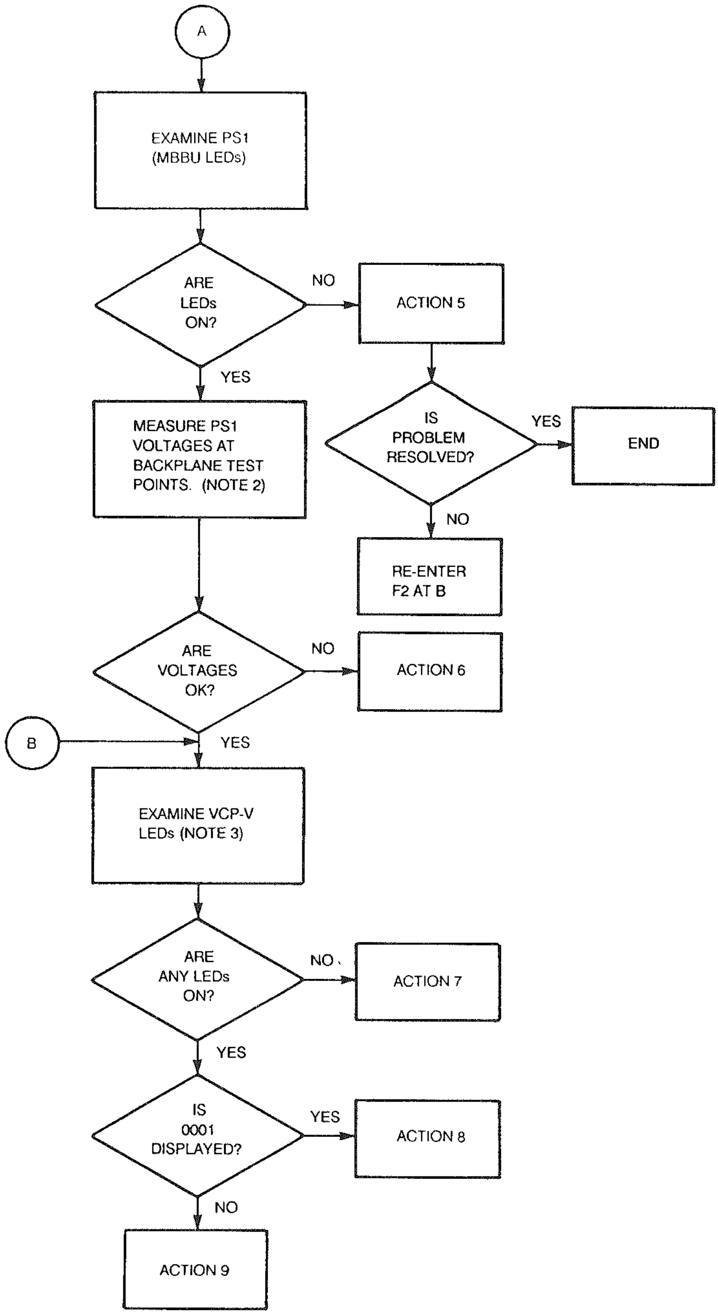


FIGURE 6-4: POWER UP PROBLEMS FLOWCHART (F2) (CONT.)

TABLE 6-3: POWER-UP SEQUENCE PROBLEMS (F2)

CONDITIONS
1. Site power, power cord, PDU relays OK via F1. 2. The PDU NEON is on. 3. No LEDs on the status panel. 4. Blower not on.

ACTIONS	NOTES
1. Replace the status panel.	1. Refer to Diagnostic LEDs On the Model 7778 Power Supplies in this chapter for diagnostic information.
2. Visually examine all cabling to the PDU and VCP-V. Verify that the power cable to PS2 is connected to J7 on the PDU and that the control cable is firmly seated into PDU connector J3. If the problem persists, replace PS2.	2. Refer to Measuring Backplane Voltages in this chapter for a voltage measurement procedure.
3. Follow the procedure described in Model 7778 Power Supply Adjustments in this chapter. If the voltage cannot be brought to specification, replace PS2.	3. Refer to VCP-V Self-Verify Messages in this chapter for diagnostic information.
4. Verify that the shunt board is installed in Slot PS1 and that the arrow on the board stiffener is pointing up. If the board is in PS1, try reseating the board.	
5. Verify that the MBBU is installed in Slot PS1. Try reseating the unit. Verify that the power cable is firmly seated in the connector marked AC In on the MBBU and J4 on the PDU. Verify that the voltage select switch is set correctly for the available voltage. If the problem persists, replace the MBBU, or remove the MBBU and install the power shunt board.	

TABLE 6-3: POWER-UP SEQUENCE PROBLEMS (F2) (CONT.)

ACTIONS	NOTES
6. Adjust the voltage. If the voltage cannot be brought to specification, replace the MBBU.	
7. Verify that the VCP-V is correctly seated in slot DP. Verify that that VCP-V/PDU interface cable is properly connected. If the problem persists, try swapping out the VCP-V. If the system still fails to power-up, replace the VCP-V/PDU interface cable.	
8. Replace the VCP-V/PDU interface cable.	
9. Replace the VCP-V.	

6.3.1.3 Verifying the AC Mains Voltage

Refer to the subsections that follow and Figure 6-5 when following this ac mains voltage verification procedure.

6.3.1.3.1 Domestic Installations

To verify ac mains voltage in domestic installations:

1. Use a voltmeter set to ac volts, measure the phase-to-phase voltage at the receptacle that provides power to the system. This voltage should be between 156 and 228 Vac RMS, with 208 Vac being optimal.

2. Measure the voltage between Ground and Hot (R, S, or T). The reading should be 120 Vac.

6.3.1.3.2 International Installations

To verify ac mains voltage in international installations:

1. Use a voltmeter set to ac volts, measure the voltage between each Hot and Neutral at the receptacle that provides ac power to the system. This voltage should be between 208 and 254 Vac RMS, with 240 Vac being optimal.

2. Measure the voltage between Ground and Hot. The reading should be 240 Vac.

3. Measure the voltage between Ground and Neutral. The reading should be 0 Vac since there should be no difference of potential between these two points.

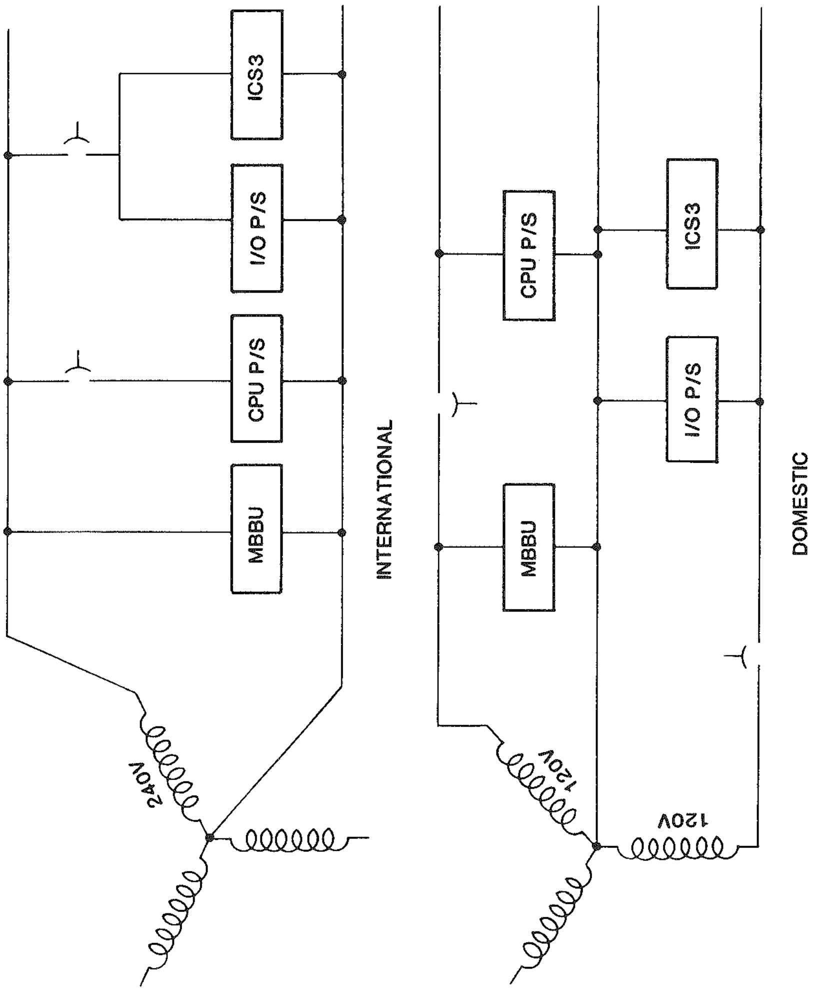


FIGURE 6-5: VERIFYING AC MAINS VOLTAGE

If voltages do not meet the specifications, notify the customer.

6.3.1.4 Measuring Backplane Voltages

Four voltage test points are located on the backplane of Model 4050/4150 systems for each system power supply (refer to Figure 6-6). Use these points to measure the +5 and ±12 volt supplies.

To measure backplane voltage, follow these steps:

1. Verify that the system is shut down and the main ac circuit breaker is OFF.

2. Remove the protective backplane cover and locate the test points for CPU power supply PS2.

3. Turn on the ac circuit system and press the ON/INITIATE SHUTDOWN button on the status panel to power up the system.

4. Using a voltmeter set to dc volts, measure the voltage between the +5 Vdc test point and the GND test point. The voltage measured should be between +4.75 Vdc and +5.25 Vdc with a +5.03 volts optimal. If this voltage is not within specification refer to Model 7778 Power Supply Adjustments in this chapter. If the voltage output cannot be brought to specification, replace the power supply.

5. Using a voltmeter, measure the voltage between the +12 Vdc lug and the GND lug. The measured voltage should be between +11.4 Vdc and +12.6 Vdc with +12.0 Vdc optimal. If this voltage is not within specification, replace the power supply.

6. Use a voltmeter and measure the voltage between the -12 Vdc lug and the GND lug. The measured voltage should be between -11.4 Vdc and -12.6 Vdc with -12.0 Vdc optimal. If this voltage is not within specification, replace the power supply.

7. Use a scope to measure backplane voltage ripple. Follow the procedure described in Model 7778 Power Supply Adjustments in this chapter. If the power supply cannot be brought within the specifications, replace the power supply.

8. Repeat steps 4 through 7 for I/O power supply PS3 or the MBBU power supply PS1. The MBBU should measure +5.1 Vac.

9. Shut down the system by pressing the ON/INITIATE SHUTDOWN button on the front panel, and turning the ac circuit breaker off.

10. Replace the backplane cover.

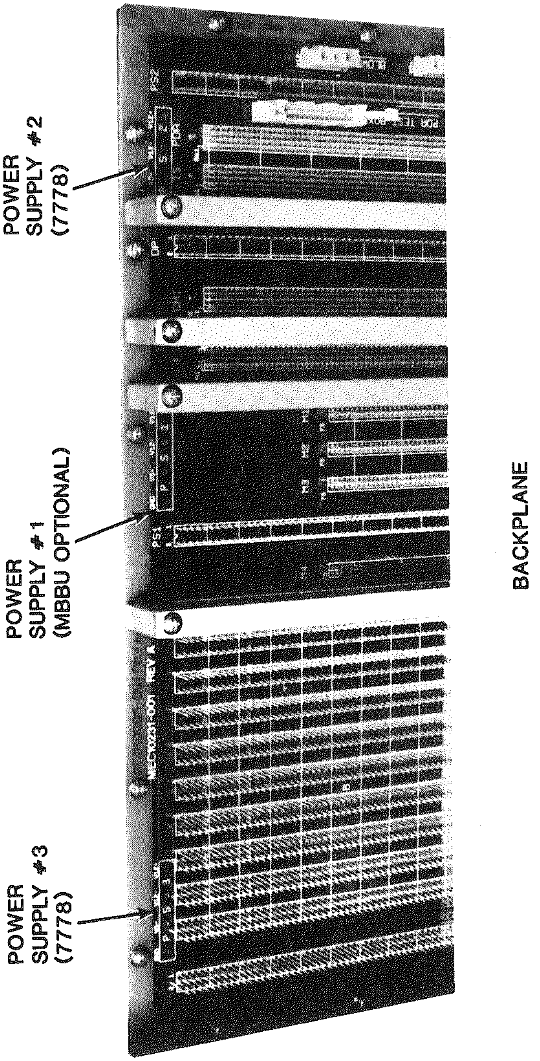


FIGURE 6-6: MEASURING BACKPLANE VOLTAGE

6.3.2 TROUBLESHOOTING SYSTEM VERIFICATION AND INITIALIZATION FAILURES

At system power-up the Model 4050/4150 performs a system verification and initialization routine before beginning the boot process.

During system verification, the CPU SYSVERIFY microcode is loaded into the CPU and executed. During system initialization, Control Store and Decode_Net are loaded and verified.

This section contains the following flowcharts:

- CPU Verification Failure
- CPU Initialization Failure

6.3.2.1 CPU Verification Failure

Refer to Figure 6-7, and Table 6-4 if a CPU fails to verify.

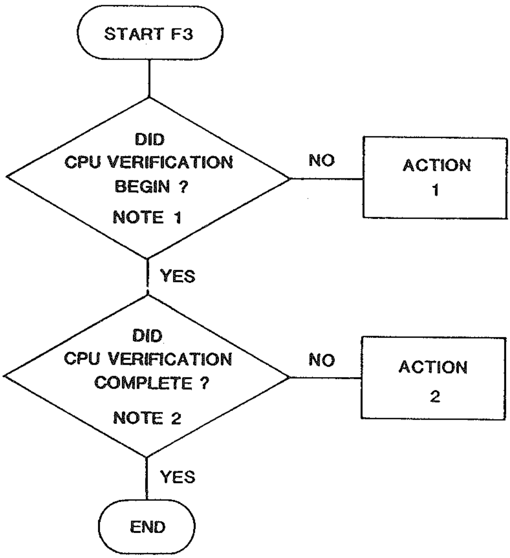


FIGURE 6-7: CPU VERIFICATION FAILURE FLOWCHART (F3)

TABLE 6-4: CPU VERIFICATION FAILURE (F3)

ACTIONS	NOTES
1. Verify the floppy diskette with a known good one. If the problem persists, suspect: • CMI Board • VCP-V Diagnostic Processor • Diskette Drive or cables	1. The following message displays: DPM002: Beginning Central Processor Verification.
2. Manually run the SYSVERIFY tests. Replace the ORU (Optimal Replaceable Unit) according to message sent by failed SYSVERIFY test.	2. The following message displays: DPM004: Central Processor system verified.

6.3.2.2 CPU Initialization Failure

Following an initialization failure, the Diagnostic Processor tries to reload Control Store three times before returning to CP mode. Refer to Flowchart F4 (Figure 6-8) and Table 6-5 if the system fails to initialize.

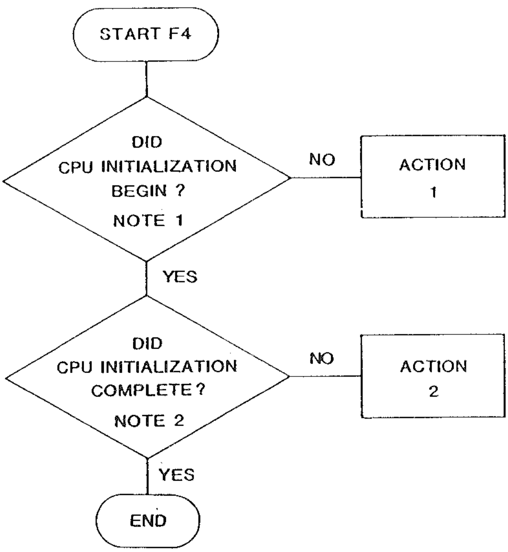


FIGURE 6-8: CPU INITIALIZATION FAILURE FLOWCHART (F4)

TABLE 6-5: CPU INITIALIZATION FAILURE (F4)

ACTIONS	NOTES
1. Verify the floppy diskette with a known-good diskette. If the system boots, replace the floppy diskette. If the problem persists, suspect: • VCP-V • CPU • CPU/VCP-V interface cable	1. When CPU microcode load begins, the following message displays: DPM005: Beginning Central Processor initialization, please wait.
2. Run Microdiagnostics and replace the ORU. (Optimal Replaceable Unit) If problem persists, replace the VCP-V.	2. The following message displays: DPM006: Central Processor initialization complete.

6.3.3 TROUBLESHOOTING BOOT AND COLDSTART FAILURES

The following sections are included for troubleshooting Boot and coldstart failures:

- CPBOOT Failure Flowchart
- System Coldstart Failure Flowchart
- System Messages during BOOT operation

6.3.3.1 CPBOOT Failure

During CPBOOT operations in Model 4050/4150 systems, the boot file is loaded from the floppy disk into the CPU, and verified. Refer to Flowchart F5 (Figure 6-9) and Table 6-6 if CPBOOT errors occur.

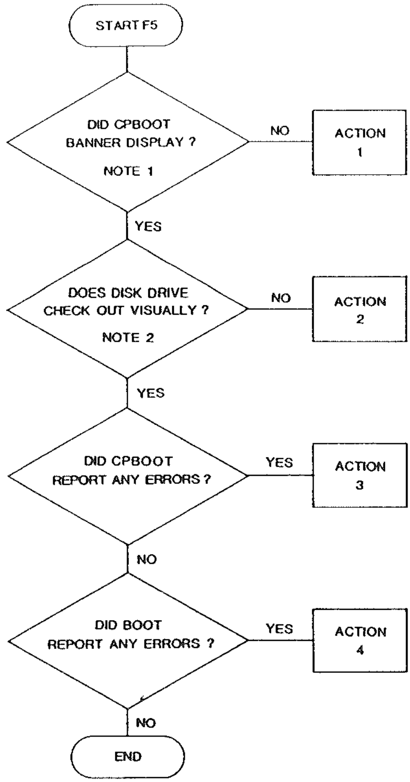


FIGURE 6-9: CPBOOT FAILURE FLOWCHART (F5)

TABLE 6-6: CPBOOT FAILURES (F5)

ACTIONS	NOTES
1. Verify the integrity of all CPU boards.	
2. Verify the Floppy Diskette with a known-good diskette. If the system boots, replace the floppy diskette. If the problem persists, suspect the memory boards, the VCP-V, the CPU, and the disk controller	1. If CPBOOT fails to load, one of the following messages can display: ERR116, ERR200 WRN001, or WRN002. Suspect the floppy drive.
3. If the disk drive does not check out visually, refer to the service manual for the drive.	
4. Refer to Table 6-8, CPBOOT Errors and Corrective Actions, in this chapter, for a description of the error message and possible corrective action.	2. Retry Boot options using Sense Switch 2000 (BOOT 14114 2000) Determine from messages which disk controller was being accessed.
5. Refer to Table 6-9, BOOT Halt Location Code Numbers, and Table 6-10, BOOT.SAVE Error Messages, for a description of the error message and possible corrective actions.	

6.3.3.2 System Coldstart Failure

If the system fails to coldstart, refer to Flowchart F6 (Figure 6-10) and Table 6-7.

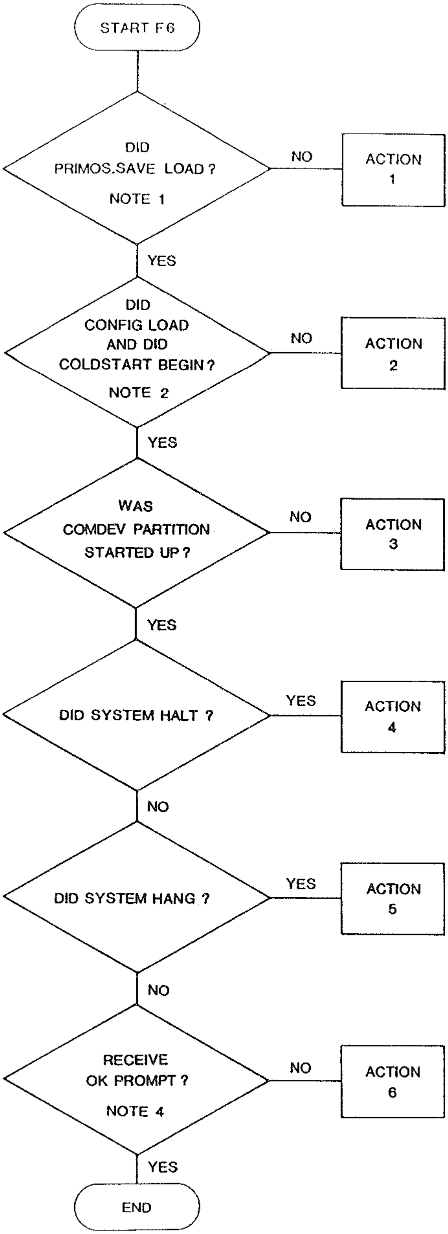


FIGURE 6-10: COLDSTART FAILURE FLOWCHART (F6)

TABLE 6-7: COLDSTART FAILURES (F6)

ACTIONS	NOTES
1. Refer to Table 6-11 PRIMOS.SAVE Error Messages for a description of the error messages and possible corrective actions. Visually check the disk drive. If disk drive appears faulty, refer to the appropriate service manual.	1. There should be a Console Message: Booting from XXXXXX PRIRUN>PRIMOS.SAVE If this message is not displayed, suspect the disk drive or cable.
2. Check the system parameters, and the CONFIG file. See PRIMOS error messages.	2. Console message: CONFIG - DATA CONFIG COLSTARTING PRIMOS. XXXXK BYTES MEMORY IN USE.
3. Check disk drive and system parameters.	3. Console message: -Starting Up Rev. 21 partition "COMDEV"
4. Check Disk drive and system parameters. If they're OK, swap first & second memory boards. If problem persists, go to Flowchart F8, (Figure 6-12) Troubleshooting System Halts.	4. At this point of Coldstart, an error message should be received if any problem occurs.
5. Check the last message displayed on the sytem console. If the communications controller has not successfully booted, the problem could be related to PRIMOS, or to the communications controller. If problem persists, go to Flowchart F9, System Hangs.	
6. Refer to the error message received on the console, and take the appropriate corrective action.	

6.3.3.3 System Messages During Boot Operations

During the autoboot to PRIMOS sequence, the system may send one of the following types of messages:

- CPBOOT Error Messages
- Boot Halts with Location Code Numbers
- BOOT.SAVE Halts with Error Messages
- PRIMOS.SAVE Error Messages

6.3.3.3.1 CPBOOT Error Messages

When CPBOOT detects an error, the system displays an error message at the system console and halts. To continue CPBOOT, execute the CP mode RUN command. Results, however, can be unpredictable. In cases where the RUN command is not permitted after the error message, the user is prompted with the message 'SYSCLR Required'.

Table 6-8 lists error messages that can be displayed by the CPBOOT, and a list of corrective actions. Note that this error list can change with different revisions of CPBOOT.

TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS

ERROR NUMBER	ERROR MESSAGE/ CORRECTIVE ACTION
1.	[Failure Report] Testing: Existence of controller: '0000xx Actual: ABSENT Expected: PRESENT 1. Verify that controller at address '0000xx is installed and properly configured. 2. Replace Controller.
2.	[Failure Report] Testing: Microverify. Controller: '0000xx Actual: FAIL Expected: PASS 1. Verify that controller at address '0000xx is installed and properly configured. 2. Replace controller.

TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS (CONT.)

ERROR NUMBER	ERROR MESSAGE/ CORRECTIVE ACTION
3.	[Failure Report] Testing: OTA ready. Actual: TIME OUT Expected: READY 1. Boot with message display turned on (data switches = 2000). Determine from message display which controller was being accessed. 2. Verify that controller is installed and configured properly. 3. Suspect controller device and CPU.
4.	[Failure Report] Testing: Controller '0000xx, Unit 00000x, STATUS Actual: 100000 Expected: 100000 1. Verify that Unit 00000x, attached to controller address '0000xx, is installed and properly configured. 2. Decode the actual status and compare it against the expected status. 3. If Unit 00000x is a disk drive, boot DTS (SAM) from tape and use IO.DISK to verify drive and controller. 4. If Unit 00000x is a tape drive, boot DTS (SAM) from disk and use IO.TAPE.MSTC to verify drive and controller. 5. Suspect Unit '00000x and Controller at address '0000xx.
5.	[Failure Report] Testing: BOOT Record Header. [address '000760 - '000763] Actual: 000000 000000 000000 000000 Expected: 000000 000000 000000 000001 1. If booting from disk, try remaking the disk, then suspect the disk drive, controller, cables, and memory boards. 2. If booting from tape suspect tape media, tape drive, controller, cables, and memory boards.

TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS (CONT.)

ERROR NUMBER	ERROR MESSAGE/ CORRECTIVE ACTION
6.	[Failure Report] Testing: 64V Two Word Indirect. Indirect Pointer: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
7.	[Failure Report] Testing: BOOT Revision Compatibility. Actual: INCOMPATIBLE Expected: COMPATIBLE
8.	[Failure Report] Testing: MTBOOT Revision Compatibility. Actual: INCOMPATIBLE Expected: COMPATIBLE
9.	[Failure Report] Testing: 64V Base Register Relative Indirect. Initial A-Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
10.	[Failure Report] Testing: 64V Two Word Indexed by Y. Y-Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
11.	[Failure Report] Testing: INA ready. Actual: NOT READY Expected: READY 1. Boot with message display turned on (data switches = 2000). Determine from message display which controller was being accessed. 2. Verify that controller is installed and configured properly. 3. Suspect controller device and CPU.

TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS (CONT.)

ERROR NUMBER	ERROR MESSAGE/ CORRECTIVE ACTION
12.	[Failure Report] Testing: Sense Switch setting. Must be at least '100000 1. Reboot using correct sense switch setting.
13.	[Failure Report] Testing: Memory. Address: 000000 Actual: 000000 Expected: 000000 1. Decode DSWSTAT and DSWRMA. Replace the indicated RAM (refer to ECCC Error Handling Guide in this chapter). 2. Replace the memory board.
14.	[Failure Report] Testing: Base Registers. Base Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
15.	[Failure Report] Testing: Machine Check Flag Actual: SET Expected: RESET DSWSTAT: 000000/000000 DSWPARITY: 000000/000000 DSWPARITY2: 000000/000000 DSWRMA: 000000/000000 1. Decode DSWSTAT, DSWPARITY, DSWPARITY2 and DSWRMA (refer to Machine Check Error Handling Guide in this chapter and take appropriate action).
16.	[Failure Report] Testing: MACHINE CHECK Program Counter: 000000 DSWSTAT: 000000/000000 DSWPARITY: 000000/000000 DSWPARITY2: 000000/000000 DSWRMA: 000000/000000 1. Decode DSWSTAT, DSWPARITY, DSWPARITY2 and DSWRMA (refer to Machine Check Error Handling Guide and take appropriate action).

TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS (CONT.)

ERROR NUMBER	ERROR MESSAGE/ CORRECTIVE ACTION
17.	[Failure Report] Testing: 64V Two Word Indirect Preindexed by X. X-Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
18.	[Failure Report] Testing: 64V Two Word Indirect Postindexed by X. X-Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
19.	[Failure Report] Testing: Register File Address: 000000 Actual: 000000 Expected: 000000
20.	[Failure Report] Testing: Address Trap Mechanism. Address: 000000 Actual: 000000 Expected: 000000 1. Suspect the CPU CMI-Board. 2. Suspect the CPU E-Board.
21.	[Failure Report] Testing: 64V Base Register Relative Indirect Preindexed. X-Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.
22.	[Failure Report] Testing: 64V Procedure Relative Indirect Postindexed. X-Register: 000000 Actual: 000000 Expected: 000000 1. Suspect CPU.

TABLE 6-8: CPBOOT ERRORS AND CORRECTIVE ACTIONS (CONT.)

ERROR NUMBER	ERROR MESSAGE/ CORRECTIVE ACTION
23.	[Failure Report] Testing: MEMORY PARITY Program Counter: 000000 DSWSTAT: 000000/000000 DSWPARITY: 000000/000000 DSWPARITY2: 000000/000000 DSWRMA: 000000/000000 1. Decode DSWSTAT, DSWPARITY, DSWPARITY2 and DSWRMA (refer to ECCU Error Handling Guide in this chapter) and replace the failing component.
24.	[WARNING] Controller '0000xx has failed microverify. 1. Verify that controller at address '0000xx is properly configured. 2. Replace controller.

6.3.3.3.2 BOOT Halts With Location Code Numbers

Halts with location code numbers occur when the BOOT encounters errors at addresses greater than 0/000100. This type of halt occurs when you execute the BOOT command. The following message is displayed on the system terminal:

HALT LOCATION: XXX

Table 6-9 lists and defines the possible codes that are displayed, and also provides corrective actions.

TABLE 6-9: BOOT HALT LOCATION CODE NUMBERS

DISPLAY CODE	DEFINITION	CORRECTIVE ACTION
100	Memory parity error on the first board	Dump DSWSTAT and DSWRMA. Locate failing board and memory RAM.
101	Machine check	Dump DSWSTAT, DSWPARITY, DSWPARITY2, DSWRMA and take appropriate action.
102	You entered a non-octal number	Re-enter BOOT command using octal values.

TABLE 6-9: BOOT HALT LOCATION CODE NUMBERS (CONT.)

DISPLAY CODE	DEFINITION	CORRECTIVE ACTION
103	A bad or nonsupported boot device type was specified in the PDEV or the sense switches	Reboot using correct parameters.
104	I/O error when booting from disk. When all of BOOT is later read in, I/O errors print a message	Replace disk controller.
105	Bad Record ID - Bad CRA Record to be read address does not match the record address boot read	Boot from another disk or from magtape.
106	Boot records are not internally consistent. One page is from one rev. and another is from another rev.	Update the boot on the media that failed.
107	<file> Not Found	
108	Memory Test Failure	

6.3.3.3.3 BOOT.SAVE Halts with Error Messages

If a recoverable BOOT halt occurs, an error message is displayed.

NOTE

> If the BOOT does halt during one of these errors (e.g., a halt caused by a recoverable memory parity error or when attempting to Boot a T&M), the error can be stepped over by issuing a RUN command.

Table 6-10 lists alphabetically and explains the halt error message, and provides corrective action.

TABLE 6-10: BOOT.SAVE ERROR MESSAGES

BAD RECORD ID ASKED XXXXXX XXXXXX FOUND XXXXXX XXXXXX Record address given does not match the record address contained in the record read. Corresponds to a boot halt with 105 in the lights. Disk media is corrupt. Boot from another disk, or from magtape, and attempt to recover. DISK ERROR STATUS: XXXXXX A disk I/O error has occurred during an attempt to boot. This error corresponds to a BOOT halt 104. Suspect disk drive. Refer to appropriate service manual for the disk drive. EMPTY FILE The BOOT RUN FILE specified contains less than 11 words and cannot be used as a BOOT RUN FILE. Reboot specifying another BOOT RUN FILE. If necessary, boot from magtape and restore the required file from tape. FILE NOT FOUND The BOOT RUN FILE specified was not found. Verify that the correct treename was used (remember MAKE is now MAKE.SAVE, COPY_DISK is COPY_DISK.SAVE, and *DOS64 is DOS.SAVE). Reboot using the correct BOOT RUN FILE treename. ILLEGAL FILENAME The BOOT RUN FILE specified contains an invalid character or contains a syntax error. The offending character is displayed. Re-enter the data. INVALID R-VEC SA XXXXXX EA XXXXXX PC XXXXXX The BOOT RUN FILE specified contains an invalid R-VEC. Reboot using the correct filename. This error occurs if an attempt is made to boot an EPF (.RUN) file instead of a .SAVE file, a SEGDIR, a UFD, or DOS>*DOS64 (Remember the name of *DOS64 is now DOS.SAVE.) MACHINE CHECK: DSWPB: XXXXXX XXXXXX DSWRMA: XXXXXX XXXXXX DSWSTAT: XXXXXX XXXXXX A machine check has been generated. Decode DSWSTAT, DSWPARITY, DSWPARITY2 and DSWRMA. Refer to the Machine Check Handling Guide, and take appropriate action.

TABLE 6-10: BOOT.SAVE ERROR MESSAGES (CONT.)

MEMORY TEST MISMATCH, Location XXXXXX XXXXXX
The location displayed was found to generate an error during memory test. RUN MEM.TEST8 and take appropriate action. Suspect the first memory board.
MT# OR OCTAL ONLY
An error has been made entering the PDEV number. Reboot using the correct number. Remember, OCTAL ONLY!
NOT A MINIMAL CONFIGURATION, NEED AT LEAST 256K WORDS
A Missing Memory Module check was generated. PRIMOS Rev. 20 and greater requires at least 256KW (512Kb) of memory. Suspect the first memory board.
PARITY ERROR: DSWPB: XXXXXX XXXXXX DSWRMA: XXXXXX XXXXXX DSWSTAT: XXXXXX XXXXXX
A memory parity error has been generated. Decode DSWSTAT, DSWPARITY, DSWPARITY2 and DSWRMA. Refer to the ECCC Error Handling Guide, and take appropriate action.
TAPE ERROR STATUS: XXXXXX XXXXXX
A tape I/O error has occurred during an attempt to boot. This error corresponds to a BOOT halt 104. Refer to Troubleshooting Disk/Tape Subsystem Failures. Refer also to appropriate peripheral service manual.
TOO MANY CHARACTERS INPUT, START AGAIN
An attempt was made to enter a command line longer than the maximum of 128 characters. Re-enter the data.

6.3.3.3.4 Halts During PRIMOS.SAVE Execution

PRIMOS recovers from a number of configuration errors, particularly those attempting to use non-existent devices, or specify paging in incorrect places. When an error occurs, an error message is displayed on the system terminal. Refer to Table 6-11 for an explanation of the error messages and corrective actions.

TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES

CANNOT ADD BOOT DEVICE XXXXXX

The boot device, if it is a disk, is not a valid file system. Boot from another disk or from magtape.

NO AVAILABLE CMDNC0 ON XXXXXX

PRIMOS.SAVE could not find the UFD CMDNC0 on the boot device. If error persists boot from another disk drive or boot from magtape and attempt to recover COMDEV. Try booting from disk with SS1 set to recover COMDEV.

FIRST COMMAND MUST BE CONFIG

The first command in PRIMOS.COMI file was not the CONFIG command. PRIMOS.SAVE prompts for COMDEV, PAGING, and NTUSR. Enter correct parameters and then use NSED to verify PRIMOS.COMI.

ERROR ACCESSING CONFIG FILE

An error occurred while trying to access the file specified by the CONFIG -DATA <filename> command in PRIMOS.COMI. PRIMOS.SAVE prompts for COMDEV, PAGING, and NTUSR. Enter the correct parameters and then verify PRIMOS.COMI and CONFIG.

MISSING PAGING

The PAGING directive is missing from the CONFIG file. PRIMOS.SAVE prompts for COMDEV, PAGING, and NTUSR. Enter correct parameters and then use NSED to correct CONFIG file.

MISSING COMDEV

The COMDEV directive is missing from the CONFIG file. PRIMOS.SAVE prompts for COMDEV, PAGING, and NTUSR. Enter correct parameters and then use NSED to correct CONFIG file.

MISSING NTUSR

The NTUSR directive is missing from the CONFIG file. PRIMOS.SAVE prompts for COMDEV, PAGING, and NTUSR. Enter correct parameters and then use NSED to correct CONFIG file.

TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES (CONT.)

ILLEGAL PAGING DEVICE SIZE FOR PAGING XXXXXX IGNORED

A zero or negative PAGING size was entered in the CONFIG file. PRIMOS uses the entire partition for paging. If you don't want to use the entire partition for paging...STOP! Boot from magtape and use NSED to correct the CONFIG file.

ILLEGAL PAGING DEVICE SIZE FOR ALTDEV XXXXXX IGNORED

A zero or negative ALTDEV size was entered in the CONFIG file. PRIMOS uses the entire partition for paging. If you don't want to use the entire partition for paging...STOP! Boot from magtape and use NSED to correct the CONFIG file.

SYSTEM NOT CONFIGURED WITH MAXIMUM POSSIBLE MEMORY:
ONLY USING XXXXK BYTES WHEN XXXXK BYTES ARE AVAILABLE

The MAXPAG value does not allow the use of all available memory. This message is a warning only. Use ED to correct the value of MAXPAG in the CONFIG file.

ALTDEV XXXXXX CONFLICTS WITH PAGDEV

The ALTDEV specified in CONFIG is the same as, or overlaps, the PAGING PARTITION is ignored. Use ED to correct ALTDEV in the CONFIG file.

INSUFFICIENT PAGING RECORDS AVAILABLE TO PAGE PRIMOS ON
PAGING XXXXXX

An insufficient number of records to page PRIMOS has been entered. PRIMOS.SAVE requests a new PAGDEV.

PRXXXX DOES NOT EXIST

A PRXXXX file, located in PRIRUN, was not found. Boot from magtape and restore the missing file(s), then reboot the system from disk.

ERROR PRE-PAGING PRIMOS FILES

An unrecoverable disk read or write error occurred while PRIMOS.SAVE was paging PRXXXX files onto either PAGDEV or ALTDEV. Use MAKE.SAVE to rebuild the PAGDEV and ALTDEV.

EXPECTED FILE MARK NOT FOUND

The magtape being used to boot is defective. Boot from another tape.

TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES (CONT.)

BAD RECORD ID, ASKED: XXXXXX FOUND: XXXXXX

Record address given does not match the record address contained in the record read. Corresponds to a boot halt with 105 in the lights. Disk media is corrupt. Boot from another disk, or from magtape, and attempt to recover.

NON-ZERO T$MT RETURN CODE: XXXXXX

An error was returned by the tape driver (T$MT) to PRIMOS.SAVE.

TAPE ERROR, STATUS: XXXXXX XXXXXX

An unrecoverable error was returned by the MSTC to the tape driver (T$MT). The boot halts. Verify that the tape drive is ONLINE. Break down tape status words I and II (refer to Tape Status Words in this chapter) and take appropriate action.

PAGING XXXXXX IS NOT A VALID PAGDEV

The PDEV number specified does not point to a valid paging device. PRIMOS.SAVE prompts for the correct PDEV. Verify the PAGING directive in the CONFIG file. If necessary boot from magtape and use NSED to make corrections.

ALTDEV XXXXXX IS NOT A VALID ALTDEV

The PDEV number specified does not point to a valid ALTDEV. PRIMOS.SAVE prompts for the correct PDEV. Verify the ALTDEV directive in the CONFIG file.

COMDEV XXXXXX IS NOT A VALID COMDEV

The PDEV number specified does not point to a valid COMDEV. PRIMOS.SAVE prompts for the correct PDEV. Verify the COMDEV directive in the CONFIG file. If necessary boot from magtape and use NSED to make corrections.

SEEK ERROR ON PAGING XXXXXX. DISK NOT READY

The initial seek to cylinder 0 on the primary paging device failed. PRIMOS.SAVE assumes that the PDEV entered in the CONFIG file is incorrect and prompts for the correct PAGDEV. Verify PAGDEV in CONFIG file. If parameters are correct, suspect the disk drive.

TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES (CONT.)

SEEK ERROR ON ALTDEV XXXXXX. DISK NOT READY

The initial seek to cylinder 0 on the alternate paging device failed. ALTDEV is ignored and the boot continues. Verify ALTDEV in CONFIG file. If parameters are correct, suspect the disk drive.

SEEK ERROR ON COMDEV XXXXXX. DISK NOT READY

CANNOT READ DSKRAT OF COMDEV XXXXXX

A disk read error occurred on record 1. Verify that correct PDEV number was specified in CONFIG file COMDEV directive. If correct, suspect disk drive.

CANNOT READ DSKRAT OF PAGDEV XXXXXX

A disk read error occurred on record 1. Verify that correct PDEV number was specified in CONFIG file PAGDEV directive. If correct, suspect disk drive and controller.

CANNOT READ DSKRAT OF ALTDEV XXXXXX

A disk read error occurred on record 1. Verify that correct PDEV number was specified in CONFIG file ALTDEV directive. If correct, suspect disk drive and controller.

COMDEV XXXXXX IS AN OLD PARTITION WHICH IS NOT SUPPORTED.

The disk partition is not supported. Boot from PRIMOS from magtape and use FIX_DISK.SAVE to convert partition.

PAGDEV XXXXXX IS AN OLD PARTITION WHICH IS NOT SUPPORTED.

Boot MAKE.SAVE from magtape and rebuild PAGDEV.

ALTDEV XXXXXX IS AN OLD PARTITION WHICH IS NOT SUPPORTED.

Boot MAKE.SAVE from magtape and rebuild ALTDEV.

THE COMDEV PDEV OF XXXXXX SHOULD POINT TO A YY HEAD PARTITION BUT POINTS TO A ZZ HEAD PARTITION.

The number of heads specified by the PDEV number for the COMDEV directive disagrees with the number of heads that are in the partition according to DSKRAT. PRIMOS.SAVE prompts for the correct COMDEV. Verify that the COMDEV directive is entered correctly in the CONFIG file.

TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES (CONT.)

THE PAGING PDEV OF XXXXXX SHOULD POINT TO A YY HEAD PARTITION BUT POINTS TO A ZZ HEAD PARTITION.

The number of heads specified by the PDEV number for the PAGING directive disagrees with the number of heads that are in the partition according to DSKRAT. PRIMOS.SAVE prompts for the correct PAGDEV. Verify that the PAGDEV directive is entered correctly in the CONFIG file.

THE ALTDEV PDEV OF XXXXXX SHOULD POINT TO A YY HEAD PARTITION BUT POINTS TO A ZZ HEAD PARTITION.

The number of heads specified by the PDEV number for the ALTDEV directive disagrees with the number of heads that are in the partition according to DSKRAT. PRIMOS.SAVE prompts for the correct ALTDEV. Verify that the ALTDEV directive is entered correctly in the CONFIG file.

PAGING XXXXXX IS NOT A SPLIT DISK AND CONFLICTS WITH COMDEV

The PDEV number specified in the PAGING directive is the same as or overlaps COMDEV and this is not a split partition.

ALTDEV XXXXXX IS NOT A SPLIT DISK AND CONFLICTS WITH COMDEV

The PDEV number specified in the ALTDEV directive is the same as or overlaps COMDEV and this is not a split partition.

PAGING XXXXXX, PARTITION XXXXXX HAS NOT PREVIOUSLY BEEN USED FOR PAGING

This message is displayed the first time PRIMOS Rev. 20.2.3 attempts to page on a non-split paging partition that has never been used for paging, or has just been made by MAKE.SAVE. If you are CERTAIN that this is a valid paging partition answer YES to the prompt 'ARE YOU SURE YOU WANT TO PAGE ON PAGING XXXXXX?'.

ALTDEV XXXXXX, PARTITION XXXXXX HAS NOT PREVIOUSLY BEEN USED FOR PAGING

This message is displayed the first time PRIMOS attempts to page on a non-split paging partition that has never been used for paging, or has just been made by MAKE.SAVE. If you are CERTAIN that this is a valid paging partition answer YES to the prompt 'ARE YOU SURE YOU WANT TO PAGE ON ALTDEV XXXXXX?'.

TABLE 6-11: PRIMOS.SAVE ERROR MESSAGES (CONT.)

COMDEV XXXXXX DOES NOT POINT TO BEGINNING OF A VALID FILE SYSTEM PARTITION
The PDEV number specified in the COMDEV directive does not point to an area with a valid file system header. PRIMOS.SAVE prompts for the correct PDEV number of COMDEV.
PAGING XXXXXX DOES NOT POINT TO BEGINNING OF A VALID FILE SYSTEM PARTITION
The PDEV number specified in the PAGING directive does not point to an area with a valid file system header.
ALTDEV XXXXXX DOES NOT POINT TO BEGINNING OF A VALID FILE SYSTEM PARTITION
The PDEV number specified in the ALTDEV directive does not point to an area with a valid file system header.
ERROR WRITING DSKRAT ON PAGING XXXXXX
A disk write error occurred while attempting to update the DSKRAT. Verify that disk is not write protected.
ERROR WRITING DSKRAT ON ALTDEV XXXXXX
A disk write error occurred while attempting to update the DSKRAT. Verify that disk is not write protected.

6.3.4 TROUBLESHOOTING POWER/ENVIRONMENTAL/VCP-V FAILURES DURING NORMAL OPERATION

Refer to the following sections, Figure 6-11 and Table 6-12 to troubleshoot power problems:

- Power/Environmental/VCP Failures Flowchart
- Sensor Check Troubleshooting
- Model 7778 Power Supply Adjustments
- Using the STATUS Command to Monitor Power Problems

6.3.4.1 Power/Environmental/VCP Failures Flowchart

Refer to Figure 6-11 and Table 6-12 to troubleshoot system power problems.

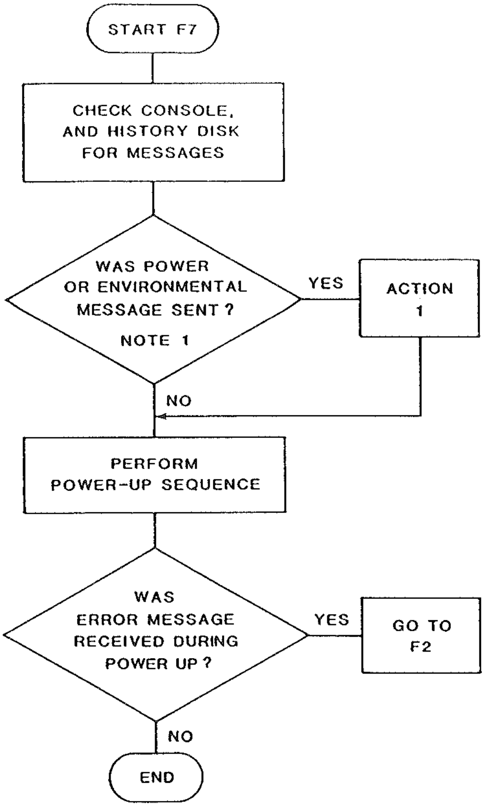


FIGURE 6-11: POWER/ENVIRONMENTAL/VCP FAILURE FLOWCHART (F7)

TABLE 6-12: POWER/ENVIRONMENTAL/VCP FAILURES DURING OPERATION (F7)

ACTIONS	NOTES
1. Replace supply <n> indicated. See Tables 6-42 and 6-43 for ERR & WRN messages and corrective actions. If the problem is not a power/environmental problem, the VCP-V could be faulty.	1. Power and environmental messages include: - power supply <n> fault - inadequate airflow - board overtemperature

6.3.4.2 Sensor Check Troubleshooting

The Diagnostic Processor supports the following sensors in Model 4050/4150 systems:

- Air Flow
- CPU Board Temperature (on CMI board)
- VCP-V Board Temperature

The environmental sensor hardware is described in detail in Chapter 4. If the Diagnostic Processor detects an active signal, it initiates a shutdown.

If an airflow failure occurs with a properly functioning blower assembly, suspect the indicated sensor first, and then the VCP-V and any associated cables. Use the following procedures to verify the air flow sensor:

1. Unplug the sensor's molex connector and insert a jumper between pins 2 and 3.

2. Cycle system power to reinitiate the VCP-V self-verification.

3. If the failure recurs, the VCP-V or associated cable is at fault. If the failure does not recur, the airflow sensor is at fault.

6.3.4.3 TLA10113 Power Supply Adjustments

The +5.1V adjustment is the only manual adjustment that can be made in the field on the TLA10113 power supplies. The adjustment is required if the power supply has been replaced or if the +5.1V output is out of specification.

To complete the power supply +5.1V adjustment:

1. Place the Diagnostic Processor (VCP-V) into Control Panel mode, and use the VSENS command to check the voltages of each power supply. The following is an example of the VSENS command.

VSENS [1....8][C]

The power supplies are numbered:

1 = Memory Battery Backup Unit (MBBU) (PS1)
2 = CPU (PS2)
3 = I/O (PS3)

2. If a voltage is out of specification, locate the +5 Vdc adjustment screw on the power supply front panel. Loosen the locknut and adjust the +5 Vdc to proper specification. Tighten the locknut and recheck the voltage for proper specification. If the +5 Vdc cannot be adjusted to specification go to step 3.

3. If the power supply voltage is not within the specifications provided in Table 6-13 and 6-14, complete the following procedure:

   A) Power down the system.

   CAUTION

   Never apply power to the system with part of the CPU unplugged from the backplane. When performing Step B, make sure all three CPU boards are firmly seated in their proper slots.

   B) Unplug all PCBs (except two for a minimum load) from the backplane serviced by the power supply (PS2 services the CPU and VCP-V; PS3 services memory and I/O. If an MBBU is present, it provides most memory and VCP-V power).

   C) Apply power to the system and check the voltage. If it is now good, isolate the board that is loading down the system voltage and replace the bad board.

   D) If the voltage is still faulty, power down and unplug the two remaining boards. Plug in two others, power up and recheck the voltage. If the voltage is still faulty, replace the power supply (refer to Removing and Replacing the TLA10113 Power Supply in Chapter 7 of this manual).

TABLE 6-13: TLA10113 POWER SUPPLY SPECIFICATIONS

VOLTAGE (Vdc)	REGULA-TION (V)	AMPS LOAD MIN/MAX	OVERCURRENT CUTOUT (A)	UNDERVOLTAGE (STL)	OVERVOLTAGE CUTOUT
+ 5.1	5.0±0.05	3.0 130	135.0±5.0	4.45±.04	6.0±0.3V
+12.0	12.0±0.60	0.0 7	10.0±0.5	11.27±.06	13.8±0.5V
-12.0	-12.0±0.60	0.0 7	10.0±0.5	-11.27±.06	-13.8±0.5V

TABLE 6-14: TLA10113 POWER SUPPLY RIPPLE

VOLTAGE	RIPPLE
+ 5.1 Vdc	50m V peak to peak
+12.0 Vdc	150m V peak to peak
-12.0 Vdc	150m V peak to peak

6.3.4.4 Using the STATUS Command to Monitor System Power

The Diagnostic Processor monitors the voltage of each power supply in the system. When it detects a supply's voltage moving out of a specific range, it displays a warning message. If the voltage eventually leaves the warning range, the Diagnostic Processor shuts down the system.

The Diagnostic Processor also maintains a count of the power supply faults, and Recoverable and Non-recoverable power fails. Use the Status command (described in Chapter 3) to display the status information on the system console:

```
OK, ESCAPE ESCAPE
CP1> STATus
```

Recoverable power failures include ac glitches that are shorter than the ride-through of the system power supplies and actual ac power failures that do not affect system operation because an MBBU is used to back up the system. If a substantial number of recoverable failures occur, suspect ac mains or the PDU.

Nonrecoverable power failures include ac glitches that are longer than the ride-through of the system power supply and actual ac failures. If a substantial number of nonrecoverable failures occur, suspect ac mains or the PDU.

Faults include power supply overcurrent and overtemperature conditions and the loss of one or more dc outputs. If a substantial number of faults occur, suspect a faulty power supply.

6.3.5 TROUBLESHOOTING SYSTEM HALTS

This section provides the following procedures and troubleshooting tools for handling system halts:

- Troubleshooting Halts Flowcharts
- PRIMOS Halts
- Hardware Diagnostic Status Registers
- General Machine Check Handling

6.3.5.1 Troubleshooting Halts Flowcharts

If the system halts, refer to Flowcharts F8 and F8-A (Figures 6-12 and 6-13) and Tables 6-15 and 6-16.

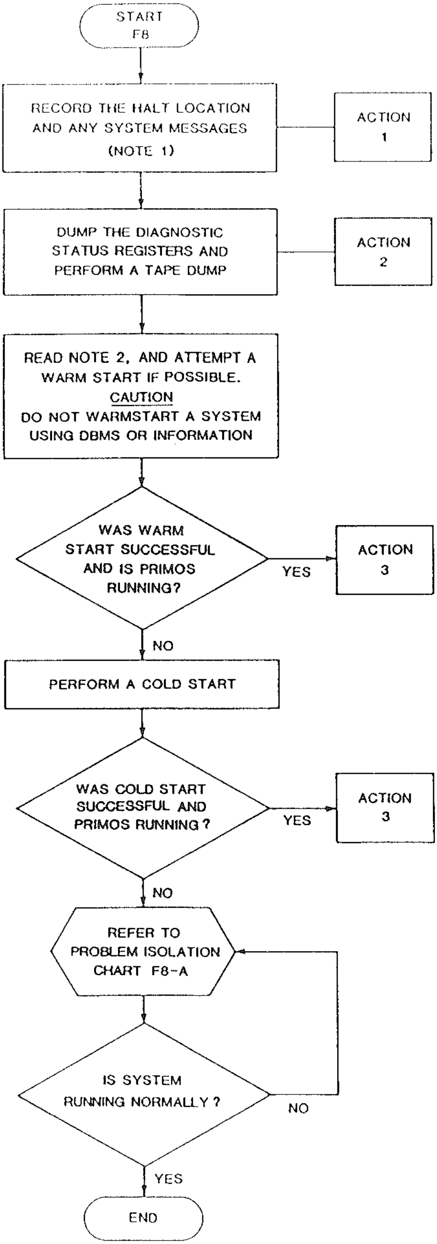


FIGURE 6-12: SYSTEM HALTS FLOWCHART (F8)

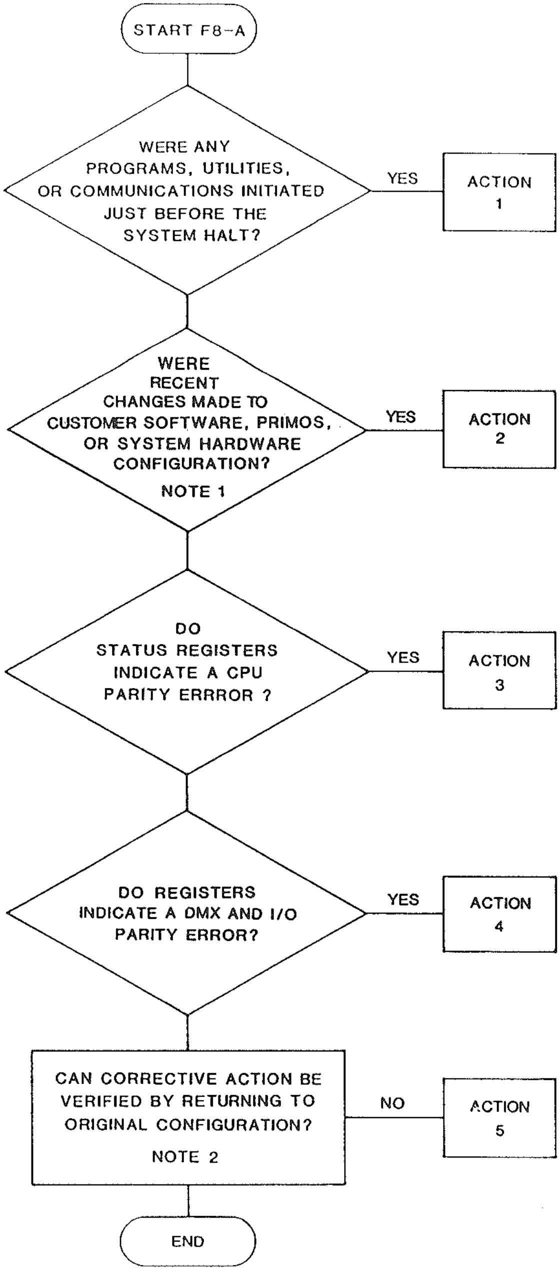


FIGURE 6-13: ISOLATING SYSTEM HALTS FLOWCHART (F8-A)

TABLE 6-15: SYSTEM HALTS (F8)

ACTIONS	NOTES
1. If Halt or Error messages are for power fail or environmental problems, refer to Flowchart F7.	1. Check the History Disk for messages. Also check messages on the console that may not be written to the History Disk. 2. At Rev. 21 PRIMOS, include the "TPDUMP YES" directive in the CONFIG file.
2. Dump registers DSWSTAT DSWPARITY, DSWPARITY2 DSWPB, DSWRMA, and perform a tape dump. Decode the registers. If registers indicate an ECCC, ECCU, or MMOD error, refer to the Memory Failures Flowchart (F11). Otherwise, continue with Flowchart F8.	3. CAUTION: Warmstart can damage a data base using ROAM-based applications (DBMS, PRIMEWAY, PRISAM). If damage occurs, a long recovery process is necessary. Perform a Coldstart if such applications are being used. DO NOT WARMSTART AFTER A SLOW HALT. Refer to "Machine Check Handling", later in this section.
3. Check event log for any entries from disk errors tape errors, or PRIMOS errors. Refer to the Problem Isolation Chart (F8-A). Perform FIX_DISK if necessary.	

TABLE 6-16: ISOLATING SYSTEM HALTS (F8-A)

ACTIONS	NOTES
1. Analyze the tape dump to determine if any of these activities are related to the system halt.	1. The problem could be related to the modifications.
2. Isolate the problem further to confirm if the Halt was caused by the modifications.	2. Before replacing any hardware or software, confirm that the symptoms and corrective actions were appropriate by analyzing the tape dump and returning the system to the original configuration.
3. Locate the logic containing the parity error (i.e. cache, STLB, RCC, etc.) and replace the appropriate CPU board.	
4. Obtain the "last vectored interrupt" address, located in the microcode scratch register by analyzing the tape dump. This register normally isolates the controller that caused the halt.	
5. Try to reproduce the problem. Use AUTOPRIMOS, DTS, and AUTOPAM with voltage and clock margining, to isolate to the hardware logic.	

6.3.5.2 PRIMOS Halts

When PRIMOS halts, a message in the following format is displayed at the system console:

PRIMOS HALTED AT XXX/YYYYYY: ZZZZZZ

DPM400: HALTED AT XXXX/YYYYYYY: ZZZZZZ

In the above message, XXXX corresponds to the segment number where the halt occurred. The word number, or offset, within the segment is indicated by YYYYYY. The contents of the location pointed to by XXXX/YYYYYY is represented by ZZZZZZ.

The slow halt, described in Chapter 3, has been substituted for several of the software halt locations described in Table 6-17.

The final halt address for all slow halts is always at HALT+1. Therefore, although several systems may halting at the same address, the cause of the halts could be different. To determine the cause of the halt, you must take a crash dump of the memory.

To determine the location of the slow halt beginning, record what was printed on the system console at the time of the halt. For further assistance, contact the Software Support Center.

CAUTION

Do not warmstart after a slow halt.

Table 6-17 defines some of the most common PRIMOS halts. Four of these halts (MCHK, MEMPA, PWRFL, and MMOD) are discovered by system hardware. The others are discovered through the system software and firmware.

TABLE 6-17: PRIMOS SYSTEM HALTS

HALT	LOCATION	DEFINITION
AMLCI_	*	Spurious AMLC interrupt.
BOOT0_	*	SHUTDN ALL stops here.**
DKSEM_	*	Disk semaphore not free when it should be.
DSTWO_	*	Illegal recursive call to disk I/O.
DSKNW_	*	No I/O windows for disk I/O.
IFLTB_	*	Bad fault in interrupt process.
INTRT_	*	Too many returns in interrupt process.**
IPAGF_	*	Page fault in interrupt process.**
MCHK_	4/305	Machine check.
MEMH2_	*	Halt after auto mapping out page.
MEMPA_	4/276	Memory parity halt (non-ECCC).
MMOD_	4/315	Missing memory check.

*Those halt locations marked with an asterisk (*) change between revisions of PRIMOS. Halt locations for the revision of PRIMOS being used on your system can be found in the RINGO map (PRIRUN>RINGO.MAP) for that revision. Use ED to examine the map.

**Slow halts as of REV. 20.2

TABLE 6-17: PRIMOS SYSTEM HALTS (CONT.)

HALT	LOCATION	DEFINITION
PAGFB_	*	Illegal block of page faults.**
PAGFI_	*	Illegal inhibit of page faults.**
PAGES_	*	Error handling fault on stack.**
PWRFL_	4/204	Power failure.
REFL0_	*	Flex, UII or PSU when not allowed.
RCMF0_	*	Restrict mode fault when not allowed.
SVCF4_	*	SVC when not allowed.
XRNG0_	*	Illegal ring number in supervisor.

*Those halt locations marked with an asterisk (*) change between revisions of PRIMOS. Halt locations for the revision of PRIMOS being used on your system can be found in the RINGO map (PRIRUN>RINGO.MAP) for that revision. Use ED to examine the map.

**Slow halts as of REV. 20.2

6.3.5.3 Hardware Diagnostic Status Registers

The hardware diagnostic status registers used to troubleshoot the MCHK, MEMPA, PWRFL, and MMOD halts are the following:

- DSWRMA (Register 34) - contains the contents of the CPU Memory Address Register (RMA) at the time of the trap. This is a virtual address and must be converted to a physical address for use.

- DSWSTAT (Register 35) - contains information regarding some of the conditions of the CPU when an error was detected.

- DSWPB (Register 36) - is a copy of the Program Counter at the time that an error was detected.

- DSWPARITY (Register 27) - DSWPARITYH contains system parity information. DSWPARITYL contains operational mode of the MMW3-8MB memory and additional system parity information.

- DSWPARITY2 (Register 24) - DSWPARITY2H contains BD, IS register file, and some cache parity information. DSWPARITY2L contains STLB and cache parity information.

Each register is 32 bits long, and is divided into a high and low side composed of 16 bits each. Tables 6-18 and 6-19 provide the word format for DSWPARITYH and DSWPARITYL. Tables 6-20 and 6-21 provide the word format for DSWPARITY2H and DSWPARITY2L. Tables 6-22 and 6-23 provide the word format for DSWSTATH and DSWSTATL. Refer to these tables when using machine halt error handling routines.

TABLE 6-18: FORMAT OF DSWPARITY REGISTER: HIGH SIDE

BITS	NAME	DESCRIPTION
1	I/O Parity	If 1, the CMI reported an I/O parity error. Sets bits 2 to 5 to represent BPD or BD errors: Bit 2: BDH, left byte Bit 3: BDH, right byte Bit 4: BDL, left byte Bit 5: BDL, right byte Bit 6: Not used Bit 7: Not used
8 to 10	RCC Parity Error Code	If DSWSTAT bit 2 is set to 1, these three bits contain the RCC parity error code: ERROR CODES 000: NO ERROR 001: FRCCPE1 010: FRCCPE2 011: FRCCPE3 100: FRCCPE4 101: FRCCPE5 110: FRCCPE6 111: FRCCPE7
11	Not Used	
12 to 13	RCC/Decode Parity Error	Describes CMI unit parity error status: ERROR CODES 00: no error 01: FRCCPE8 10: DNETPE1 11: DNETPE2
14 to 16	E Unit parity Error Code	Describes the E unit parity error status: ERROR CODES 000: no error 001: BBH left parity error 010: BBH right parity error 011: BBL left parity error 100: BBL right parity error 101: BAH parity error 110: BAL parity error 111: BAE parity error

TABLE 6-19: FORMAT OF DSWPARITY REGISTER: LOW SIDE

BITS	NAME	DESCRIPTION
1	Not Used	
2	Memory Address Shift Control	Specifies the address size of a slot in the memory backplane: 0: 8-megabyte slot decode 1: 16-megabyte slot decode
3	Memory Array	Memory array number 1 reported error
4	Memory Array	Memory array number 2 reported error
5	Memory Array	Memory array number 3 reported error
6	Memory Array	Memory array number 4 reported error
7	Not Used	
8	Not Used	
9	Not Used	
10	Not Used	
11	Not Used	
12	Not Used	
13	Parity Error	CMI reported a write buffer data high left parity error
14	Parity Error	CMI reported a write buffer data high right parity error
15	Parity Error	CMI reported a write buffer data low left parity error
16	Parity Error	CMI reported a write buffer data low right parity error

TABLE 6-20: FORMAT OF DSWPARITY2 REGISTER: HIGH SIDE

BITS	NAME	DESCRIPTION
1 to 4	IS Unit Reports Memory Errors	A 1 in any of these bits specifies the error reported by the IS unit: Bit 1: BDH left parity error Bit 2: BDH right parity error Bit 3: BDL left parity error Bit 4: BDL right parity error
5	IS reported a Base register file parity error, high	
6	IS reported a Base register file parity error, low	
7	IS reported a Index register file parity error	
8 to 9	Not Used	
10	Branch Cache Recoverable Error	If 1, the microcode reported a branch cache recoverable error.

TABLE 6-20: FORMAT OF DSWPARITY2 REGISTER: HIGH SIDE (CONT.)

BITS	NAME	DESCRIPTION
11 to 16	IS Unit Reports Cache parity Errors	A 1 in any of these bits specifies the cache parity error reported by the IS unit: Bit 11: Cache data parity error on Element B even data low byte Bit 12: Cache data parity error on Element B odd data low byte Bit 13: Cache data parity error on Element A even data low byte Bit 14: Cache data parity error on Element A odd data low byte Bit 15: Cache index parity error on Element B low byte Bit 16: Cache index parity error on Element B high byte

TABLE 6-21: FORMAT OF DSWPARITY2 REGISTER: LOW SIDE

BITS	NAME	DESCRIPTION
1 to 16	IS Unit Reports Cache or STLB Errors	A 1 in any of these bits specifies the cache or STLB parity error reported by the IS unit: Bit 1: Cache data parity error on Element A even data high byte Bit 2: Cache data parity error on Element A odd data high byte Bit 3: Cache data parity error on Element B even data high byte Bit 4: Cache data parity error on Element B odd data high byte Bit 5: Cache index parity error on Element A high byte Bit 6: Cache index parity error on Element A low byte Bit 7: STLB parity error on Element B physical address low byte Bit 8: STLB parity error on Element A physical address low byte Bit 9: STLB parity error on Element B access bits Bit 10: STLB parity error on Element B process ID Bit 11: STLB parity error on Element B virtual address tag Bit 12: STLB parity error on Element A physical address high byte

TABLE 6-21: FORMAT OF DSWPARITY2 REGISTER: LOW SIDE (CONT.)

BITS	NAME	FUNCTION
		Bit 13: STLB parity error on Element B physical address high byte Bit 14: STLB parity error on Element A access bits Bit 15: STLB parity error on Element A process ID Bit 16: STLB parity error on Element A virtual address tag

TABLE 6-22: FORMAT OF DSWSTAT REGISTER: HIGH SIDE

BITS	NAME	DESCRIPTION
1	Check Immediate	If 1, the check was taken immediately.
2	Machine Check	If 1, a machine check occurred.
3	Memory Parity	If 1, a memory parity error occurred.
4	Missing Memory Module	If 1, a missing memory module caused the check.
5	E Unit	If 1, the E unit reported a parity error.
6	IS Unit	If 1, the IS unit reported a parity error.
7	CMI Unit	If 1, the control store, memory controller I/O unit reported a parity error.
8	Not Used	
9	ECCU	If bits 3 and 9 are both 1, the memory ECC error was uncorrectable.
10	ECCC	If bits 3 and 10 are both 1, the memory ECC error was correctable.
11	Not Used	
12	RCM Parity	If 1, an RCM parity error was detected by the control store board.
13 to 14	RPBU	Specifies the RP backup count at the time of the error.
15	DMx Operation	If 1, a DMx transfer was in progress when the error occurred.
16	I/O Operation	If 1, an I/O operation was in progress when the error occurred.

TABLE 6-23: FORMAT OF DSWSTAT REGISTER: LOW SIDE

BITS	NAME	DESCRIPTION
1 to 7	ECC Syndrome Bits	If correctable memory parity error ocurred, it is encoded in these bits.
8	Memory Module Number	If a memory error occurred, this bit identifies the interleaved memory module with the error (bit 15 of address).
9	RMA Invalid	If 1, the contents of DSWRMA are invalid.
10	Recoverable Parity Error	If 1, a recoverable parity error occurred in the cache, STLB, or branch cache.
11	Hard Error	If bit 10 is 1 and this bit is also 1, a recoverable hard parity error occurred. There is a permanent error in hardware.
12	Not used	
13	Internal Error	If 1, the microcode detected an internal error. DSWRMA has a code that indicates the failing microcode algorithm.
14	Not Used	
15	Not Used	
16	Not Used	

6.3.5.4 General Machine Check Handling

If a machine check is detected the CPU halts at location 4/306. Machine checks can be caused by the CPU, I/O controllers, memory boards, and the backplane assembly, and occur when the CPU detects bad parity on one of its internal data paths or one of the external buses (BPD, BPA, BMD, or BMA).

The VCP-V Diagnostic Processor in the Model 4050/4150 systems automatically dumps DSWSTAT, DSWRMA, DSWPB, DSWPARITY, and DSWPARITY2 information to the system console before halting.

The first halt after a PRIMOS coldstart saves the entire register file set in memory until the next coldstart. Reference the memory maps for further PRIMOS information including the location of the registers.

After the CPU detects a machine check halt, it reports the status of the check in DSWSTAT. A Warm Start keeps the system operating long enough to record the halt in the event log, but is usually NOT recommended. Use the following guidelines before warmstarting after a system halt:

- Do not warmstart a system using ROAM-based products (DBMS, Primeway, PRISAM) or Midasplus.
- Warmstart can be used to recover from a subsystem hang.
- At Rev. 21, do not warmstart if communications controllers hang.
- Do not warmstart after a hardware failure.

To isolate the component that caused the Machine Check halt, follow this procedure:

CAUTION

Be sure to refer to the warmstart guidelines in this section before warmstarting the system after a machine check. Warmstarting in some instances could cause further loss of data.

1. Record DSWSTAT, DSWPARITY, DSWPARITY2, DSWRMA, and DSWPB values that display on the system console, and dump Registers 0, 1 and 2.

2. Refer to the flowcharts in Figures 6-12 and 6-13 to isolate the fault, and repair the hardware.

3. Coldstart the system and run FIX_DISK.

6.3.6 TROUBLESHOOTING SYSTEM HANGS

This section provides the troubleshooting procedures for handling system hangs on a Model 4050/4150 system. Refer to flowchart F9 (Figures 6-14 and 6-15) to troubleshoot system hangs. Tables 6-24 and 6-25 are a summary of the corrective actions to resolve system hangs.

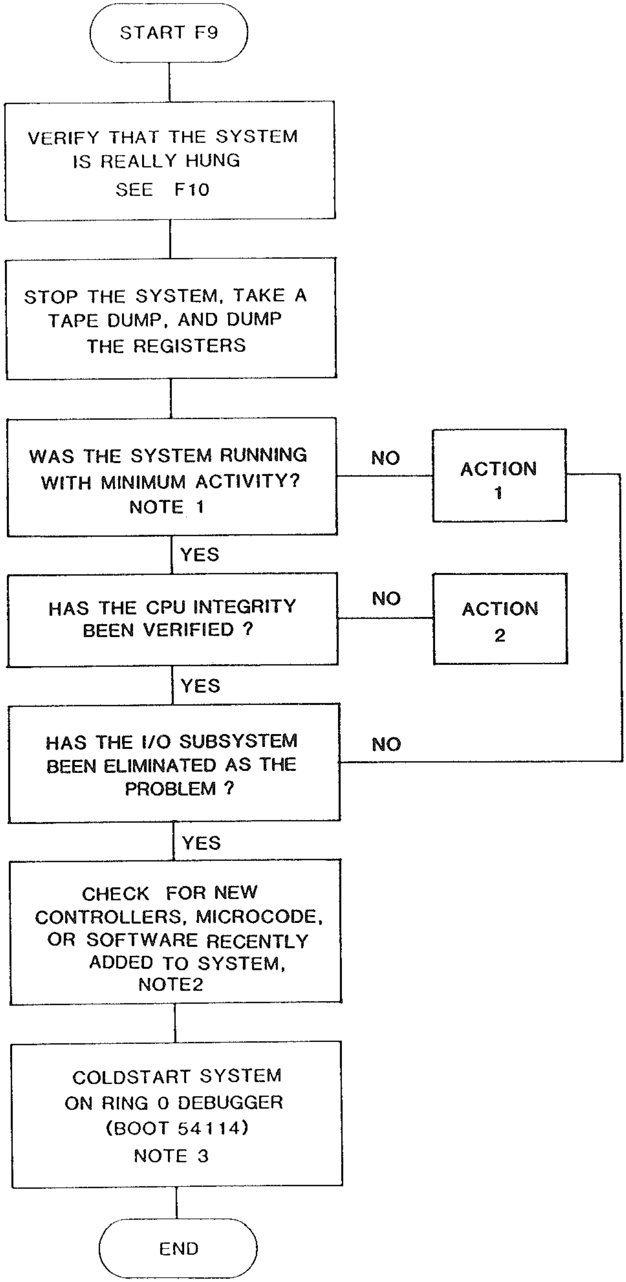


FIGURE 6-14: SYSTEM HANGS FLOWCHART (F9)

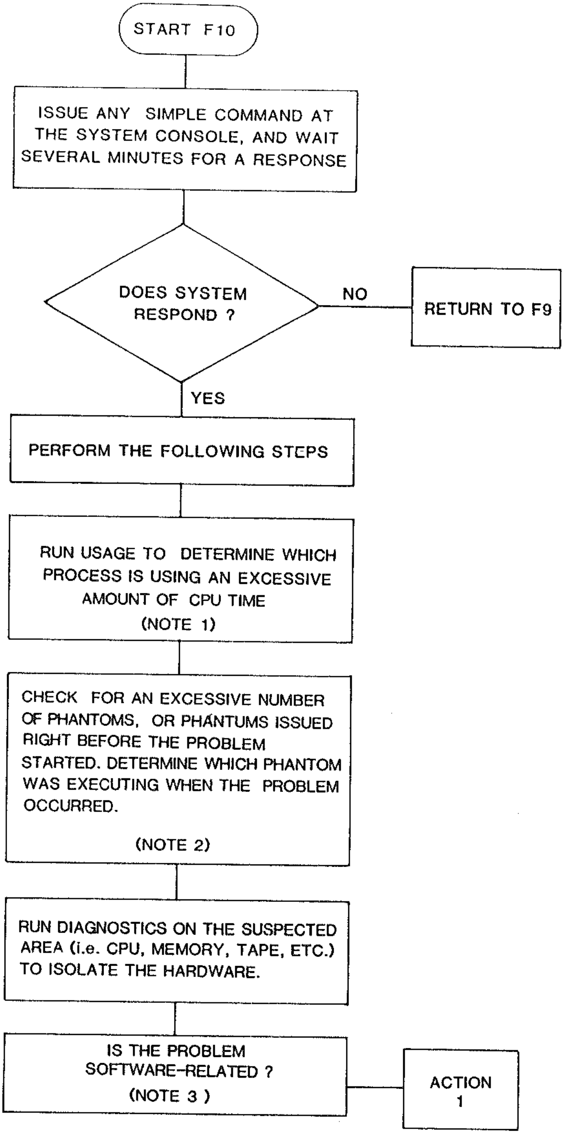


FIGURE 6-15: DETERMINING IF SYSTEM IS REALLY HUNG (F10)

TABLE 6-24: SYSTEM HANGS (F9)

ACTIONS	NOTES
1. If activity has been isolated to a particular process, run diagnostics on the associated controller.	1. Check for any activity started at the system console (i.e. phantom login, tape activity, spool, etc.) Check the associated controller (Action 1).
If the diagnostics do not fail, try to reproduce the problem with PRIMOS operating (i.e., tape backup, disk-to disk copy, etc.) If runnning diagnostics and reproducing the problem are not successful, return to the flowchart (F9).	2. If a new controller has been added, remove it if possible, and coldstart the system. If new microcode has been added, return to the previous rev. microcode, if possible, and coldstart the system.
2. With PRIMOS operating, run AUTOPAM and/or AUTOPRIMOS, to see if the CPU fails (HANG or HALT tests fail). If the tests do not fail, run them again under the following conditions: o voltage margining o frequency margining o heavy user activity If the problem is still not isolated, return to the flowchart (F9).	3. Coldstarting the system with Ring0 Debugger (BOOT 54114) allows you to check the debugger when the system hangs again, to see which process was underway. The debugger may be invoked at any time from the system console with: CTRL C\. Use the HELP option in the debugger routine for a list of commands.

NOTE

Coldstarting the system with the Ring0 debugger takes more memory, although it should not cause a problem.

TABLE 6-25: DETERMINING IF THE SYSTEM IS REALLY HUNG (F10)

ACTIONS	NOTES
1. Boot 54114 to start Ring0 Debugger on coldstart. The next time the problem occurs, use Ring0 debuggger to help isolate the problem.	1. See software service guide SSG080 for information on USAGE. 2. Spooler, network, monitors, etc. Suspect associated controller. 3. If the problem appears to be software related, get software assistance. Go to Action 1.

6.3.7 TROUBLESHOOTING MEMORY PROBLEMS

This section provides corrective maintenance instructions for Model MMW3-8MB memory array boards. Troubleshooting information is organized into the following subsections:

- Troubleshooting Memory Problems Flowchart
- Handling System Memory Boards
- Correctable Memory Parity Errors (ECCC)
- Uncorrectable Memory Parity Errors (ECCU)
- Missing Memory Module Errors
- Troubleshooting With MEM.TEST.8
- Using MEM.TOOLBOX

Refer to Figure 6-16 and Table 6-26 to troubleshoot memory problems.

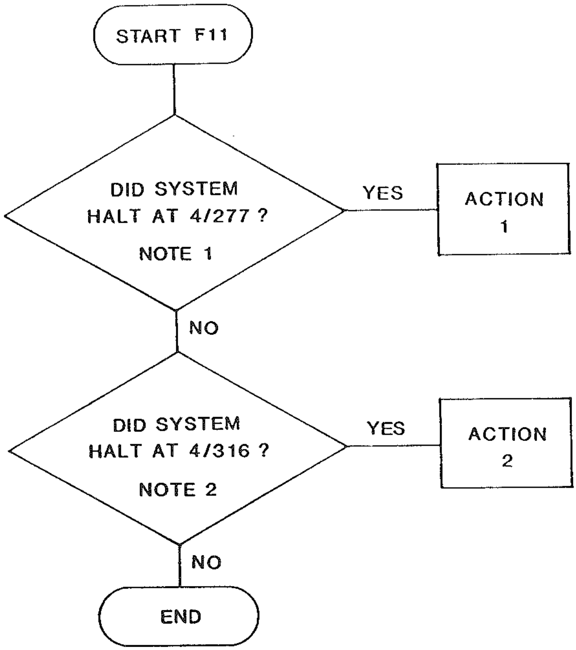


FIGURE 6-16: MEMORY PROBLEMS FLOWCHART (F11)

TABLE 6-26: MEMORY PROBLEMS (F11)

ACTIONS	NOTES
1. This is an Uncorrectable Memory Parity halt (MEMPA_). Refer to Diagnostic Status Registers and ECCU Error Handling Guide in this section.	1. Suspect the memory array boards or CMI board. If boards check out, it could be a faulty Power Supply.
2. This is a Missing Memory Trap (MMOD_). Obtain PPN/WW information from the system console, and follow the procedures in the Missing Memory Module Handling Guide in this section.	2. Suspect the following: a) Memory b) CPU (CMI board) If neither is faulty, it could be a bad address on the AMLC, or ICS products.

6.3.7.1 Handling System Memory Boards

Memory boards contain MOS ICs that can be easily damaged by electro static discharge. When handling memory boards, be sure to use the Field Service Grounding Kit (TEATTFSKIT) and adhere to the following rules:

- Do not handle the board when the board is out of its protective shipping bag unless the grounding kit is worn.
- Do not walk across carpeted floors, especially in low humidity areas, when handling the boards out of their shipping bags.

The Field Service Grounding Kit consists of a 10-foot (3-meter) ground cord, a work surface, and a 12-foot (3.6-meter) wrist strap. Use the following procedure:

1. Attach the work surface to system ground via the 10-foot ground cord.
2. Attach the wrist strap to ground via the 12-foot ground cord.
3. Slip on the wrist strap.
4. When removing a memory board be sure to place it on the grounded work surface. Always place the board in a static shielding bag if further handling or shipping is required. Use the bag in which the board was shipped, or use the pocket of the work surface, which is designed for this purpose.

6.3.7.2 ECCC Error Handling Guide

Memory ECCC errors do not halt the system, but can degrade system performance. Isolate and repair a faulty memory board as soon as system operation makes it convenient.

ECCC error handling information is presented in the following subsections:

- Identifying a Failing RAM
- Sample ECCC Error

6.3.7.2.1 Identifying a Failing RAM

This section provides a general procedure for identifying a failing RAM on a Model MMW3-8MB memory array board. The next section provides an example and detailed instructions for interpreting and troubleshooting a typical ECCC memory error.

To identify a faulty RAM, follow these steps:

1. Locate the ECCC memory error in LOGREC (refer to Checking the Event Loggers in Chapter 5 of this manual for instructions).
2. Form the 25-bit Physical Memory Address as follows:

A) The 10 LSBs of the WN equal the 10 LSBs of the Physical Memory Address.

B) The 15 LSBs of the PPN equal the 15 MSBs of the Physical Memory Address.

3. Note the seven MSBs of DSWSTATL. This identifies the bit in error code.

4. Refer to the MMW3 decode chart (Figure 6-17) to identify the slot, bank, and row of the faulty bit.

5. Refer to the MMW3 bit in error decode table (Table 6-27) to determine the bit-in-error code.

6. Refer to the MMW3 bit map (Figure 6-18), and then use the slot, bank, and row, and the bit-in-error code to identify the faulty RAM.

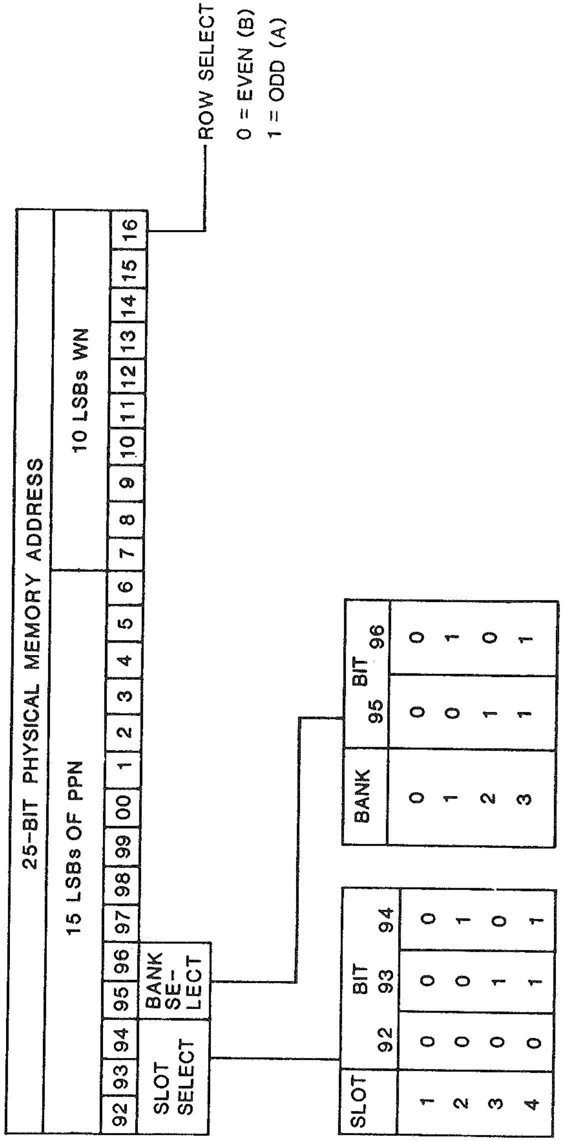


FIGURE 6-17: MMW3-8MB DECODE CHART

HANDLE END OF BOARD

LEFT SIDE OF BOARD

A ODD
B EVEN

	A	B	A	B	A	B	A	B	A	B	A	B
BANK 3	32	32	29	29	26	26	23	23	20	20	17	17
	31	31	28	28	25	25	22	22	19	19	16	16
	30	30	27	27	24	24	21	21	18	18	15	15
BANK 2	30	30	27	27	24	24	21	21	18	18	15	15
	31	31	28	28	25	25	22	22	19	19	16	16
	32	32	29	29	26	26	23	23	20	20	17	17
BANK 1	32	32	29	29	26	26	23	23	20	20	17	17
	31	31	28	28	25	25	22	22	19	19	16	16
	30	30	27	27	24	24	21	21	18	18	15	15
BANK 0	30	30	27	27	24	24	21	21	18	18	15	15
	31	31	28	28	25	25	22	22	19	19	16	16
	32	32	29	29	26	26	23	23	20	20	17	17

DRIVERS

RIGHT SIDE OF BOARD

A	B	A	B	A	B	A	B	A	B	A	B	A	B
14	14	12	12	10	10	8	8	6	6	4	4	2	2
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
14	14	12	12	10	10	8	8	6	6	4	4	2	2
14	14	12	12	10	10	8	8	6	6	4	4	2	2
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
14	14	12	12	10	10	8	8	6	6	4	4	2	2

CONNECTOR END OF BOARD

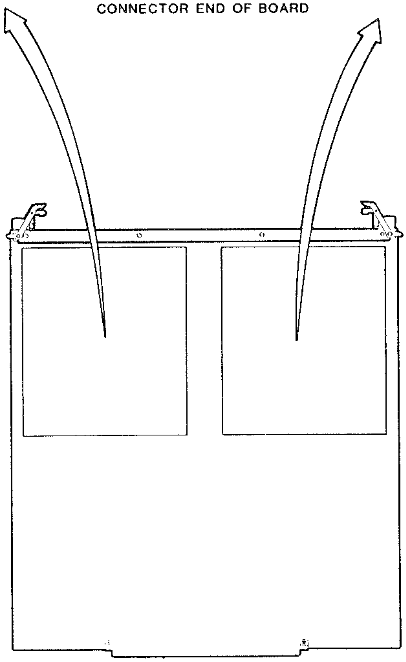


FIGURE 6-18: MMW3-8MB BIT MAP

6.3.7.2.2 Sample ECCC Error

This section provides a sample memory ECCC error and a bit-in-error troubleshooting exercise. A typical ECCC error, as recorded in the event logger, is shown in Figure 6-19.

```
                              20:29:28 MONDAY APRIL 20, 1986
                              ------------------------------
MEMORY PARITY (ECCC)
DSWSTAT = 020110 017400 (OCT)
DSWRMA = 064003 066735 (OCT)
DSWPB = 064000 001030 (OCT)
DSWPARITY = 140000 000000 (OCT)
PHYSICAL PAGE NUMBER = 004043 (OCT) WORD NUMBER = 000737 (OCT)ECCC
SYNDROME = BIT 02
PHYSICAL ADDRESS = 106735 (OCT)
```

Note: PPN, WN, and ADDRESSES are octal numbers.

FIGURE 6-19: MEMORY ECCC ERROR

To interpret a memory ECCC error and obtain the information necessary to identify a failing RAM, refer to Figure 6-19 and the example that follows.

1. Locate the ECCC error recorded in the event log printout (Figure 6-19).

2. Note the value of the PPN, 004043, and the WN, 000735.

3. Form the 25-bit Physical Memory Address as follows:

   A) Note that the 15 MSBs of the Physical Memory Address are the 15 LSBs of the PPN and that the 10 LSBs of the Physical Memory Address are the 10 LSBs of the WN.

   B) Convert the PPN to binary:

      '004043 - 000 000 100 000 100 011

   C) The 15 LSBs of the PPN (000 100 000 100 011) become the 15 MSBs of the Physical Memory Address.

   D) Convert the WN to binary:

      '000737 = 000 000 000 111 011 111

   E) The 10 LSBs of the WN (0 111 011 111) become the 10 LSBs of the Physical Memory Address.

   F) The Physical Memory Address is as follows:

      0 001 000 001 000 110 111 011 111

4. Decode bits 92, 93 and 94 (refer to Figure 6-17) to determine the slot number of the failing memory board.
   000 = Slot A1

5. Decode bits 95 and 96 (refer to Figure 6-17) to determine the bank number of the failing RAM.

   10 = Bank 2

6. Decode bit 16 (refer to Figure 6-17) to determine whether the failing RAM is odd (row A) or even (row B).

   1 = Odd (Row A)

7. Note the value of DSWSTAT low from LOGREC.

   DSWSTATL = 017400

8. Using Table 6-27, decode the seven MSBs of DSWSTATL to determine the bit in error.

   017 = 0001111 = data bit 2

9. Refer to Figure 6-18 and the information gathered in the previous steps to determing the location of the failing bit: slot 1, bank 2, row A, data bit 2.

TABLE 6-27: MMW3 BIT IN ERROR DECODE TABLE

DSWSTATL MSBs	BIT IN ERROR
0001010	1
0001111	2
0010010	3
0010100	4
0010111	5
0011000	6
0011011	7
0011101	8
0100010	25
0100100	26
0100111	27
0101000	28
0101011	29
0101101	30
0110000	32
0110101	31
0111111	CB0
1001011	17
1001110	18
1010011	19
1010101	20
1010110	21
1011001	22
1011010	23
1011100	24

TABLE 6-27: MMW3 BIT IN ERROR DECODE TABLE (CONT.)

DSWSTATL MSBs	BIT IN ERROR
1011111	CB1
1100011	9
1100101	10
1100110	11
1101001	12
1101010	13
1101100	14
1101111	CB2
1110001	16
1110100	15
1110111	CB3
1111011	CB4
1111101	CB5
1111110	CB6
1111111	No Error

6.3.7.3 ECCU Error Handling Guide

Uncorrectable errors often halt the system, requiring immediate intervention by the operator or CSR if on-site. Use the following procedure to recover from ECCU errors:

NOTE

> Never use the MASTER CLEAR button or the SYSCLR and VIRY commands before recording the halt location in the system logbook and determining all of the recovery actions to be performed. Some recovery actions are ineffective unless they are taken before using MASTER CLEAR, SYSCLR, or VIRY.

1. When the system halts, do not Master Clear or SYSCLR. Fetch and record registers 0, 1, and 2 in mapped memory mode. These registers contain the following information:

    Register 0 = Current User Number
    Register 1 = PPN (Physical Page Number)
    Register 2 = WN (Word Number)

2. Note the Diagnostic Status Word (DSWSTAT) that appears on the system console.

3. When the user number (Register 0) recorded in Step 1 is a 0 or 1, the system must be cold started because the error is in the operating system. Failure to cold start the system could lock out the operating system. If the system is to be cold started, this may be a good time to repair or replace the failing memory board (refer to Identifying a Failing RAM in this chapter).

4. If the user number (Register 0) is greater than one, lock the page out in memory by entering RUN (do not MASTER CLEAR). This locks out the page (1024K words) to system use in memory only. The page

is unlocked at coldstart. Now Master Clear and Warm Start the system.

NOTE

Inform the system operator of the user number indicated in Register 0. This user is affected by the lock out. The user should restart any jobs in progress.

5. If the system (PRIMOS) stays up for one minute after Warm Start, the memory parity error is automatically recorded in the event log. Otherwise, perform a SHUTDN ALL to record the error in the event log.

6. Use the information from the event log or from DSWSTAT, PPN, and WN recorded in step 2 to isolate the failing memory board as described in Identifying a Failing RAM in this chapter.

6.3.7.4 Missing Memory Error Handling Guide

When a missing memory module check occurs (halt at 4/315) and the operating system records the error after a warm start, the following information is displayed on the system console:

MISSING MEMORY, DSWSTAT = xx DSWRMA = xx DSWPB = xx DSWPARITY =xx

Use the following procedure to locate the slot number of the possibly failing memory board using DSWRMA:

1. Convert the value of DSWRMA to binary.

2. Bits 8-16 of DSWRMAH are the nine most significant bits of the Physical Address.

3. Use bits 92, 93, and 94 of the Physical Address (refer to Figure 6-17) to determine the slot location of the memory board that contains the missing address.

4. If the procedure provides a memory address that should exist, replace the failing memory board. Otherwise, a failing CPU board (CMI) or a software error could be indicated.

6.3.7.5 Troubleshooting With MEM.TEST8

MEM.TEST8 is a Diagnostic Testing System utility to test 8 Mb memory boards in Model 4050/4150 systems. Since it uses restricted instructions and writes all memory, it can only run under the Stand Alone Monitor (SAM). This diagnostic resides in the first 32Kw of main memory with the Monitor residing in the second 32Kw of main memory.

MEM.TEST8 operating instructions and troubleshooting procedures are described in Diagnostic Testing System Software Service Guide (SSG400).

6.3.7.6 Using MEM.TOOLBOX

MEM.TOOLBOX is a collection of programs to assist the user when configuring and/or debugging memory subsystems. Most of the MEM.TOOLBOX tests run under SAM or PAM.

MEM.TOOLBOX operating instructions are described in Diagnostic Testing System Software Service Guide (SSG400).

6.3.8 TROUBLESHOOTING DISK/TAPE SUBSYSTEM FAILURES

This section provides troubleshooting procedures and reference information to diagnose and correct failures to the following Model 4050/4150 disk or tape subsystems:

- Model 4587 Tape Subsystem (GCR Quad-Density Drive and MSTC)
- Model 4735 Disk Subsystem (496Mb Drive and IDC1 Controller)
- Model 4835 Disk Subsystem (770Mb Drive and IDC1 Controller)

For additional troubleshooting information, refer to the following publications:

- Model 4587 Tape Subsystem Service Procedures Manual (SPM920).
- 496 Megabyte Fixed Module Disk Subsystem Service Procedures Manual (SPM470).
- 770 Megabyte Fixed Storage Disk Subsystem Service Procedures Manual (SPM390).

6.3.8.1 Troubleshooting Model 4587 Tape Subsystem Failures

The following subsections contain information to identify Model 4587 Tape Subsystem failures:

- Troubleshooting MSTC Self-Verification Failures
- Using MSTC Status Indicators
- Decoding MSTC Tape Status Words

If the information provided in this subsection indicates the MSTC controller is operating correctly, refer to Model 4587 Tape Subsystem Service Procedures Manual (SPM920) for tape drive troubleshooting and corrective action procedures.

6.3.8.1.1 Troubleshooting MSTC Self-Verification Failures

A set of self-verification diagnostics is executed whenever power is applied to the MSTC, when a SYSCLR is received, or an OCP '17 is received. The diagnostics test the tape logic of the MSTC, and are designed to isolate over 80% of the possible failures. Self-verification status is reported by two sets of six LEDs mounted at the front of the board. One set of LEDs corresponds to the QIC-02 portion of the MSTC and is not used. The other set corresponds to the SCSI interface used by the Model 4587 Tape Subsystem, as shown in Figure 6-20.

Each set of LEDs contains one single red LED, one single green LED, and an array of four red LEDs. The single LEDs are used to indicate the operational status of the MSTC. The group of four LEDs can indicate the number of the diagnostic test being executed during self-verification, or the status of the respective device while the system is operating. Table 6-28 indicates the various states of the diagnostic LEDs.

TABLE 6-28: MSTC DIAGNOSTIC LED TRUTH TABLE

----LED ARRAY---- 1	2	3	4	GRN LED	RED LED	DESCRIPTION
OFF	OFF	OFF	OFF	OFF	OFF	Power OFF, or other abnormal condition.
x	x	x	ON	ON	OFF	DRAM Memory Warning. The value xxx represents the status of the SCSI Interface. Refer to Table 6-30.
x	x	x	OFF	ON	OFF	DRAM Memory is OK. The value xxx represents the status of the SCSI Interface. Refer to Table 6-30.
y	y	y	y	OFF	ON	Self-Verification has failed. The value yyyy is the test number that failed. Refer to Table 6-29.
y	y	y	y	ON	ON	Self-Verification in progress. The value yyyy is the test being executed. Refer to Table 6-29.

There are two modes of execution for the MSTC self-verification tests: Destructive Mode and Non-Destructive Mode.

Destructive Mode testing invokes memory tests that destroy the contents of the controller's DRAM and SRAM. For this reason Destructive Mode testing is allowed only if one or more of the following conditions are true.

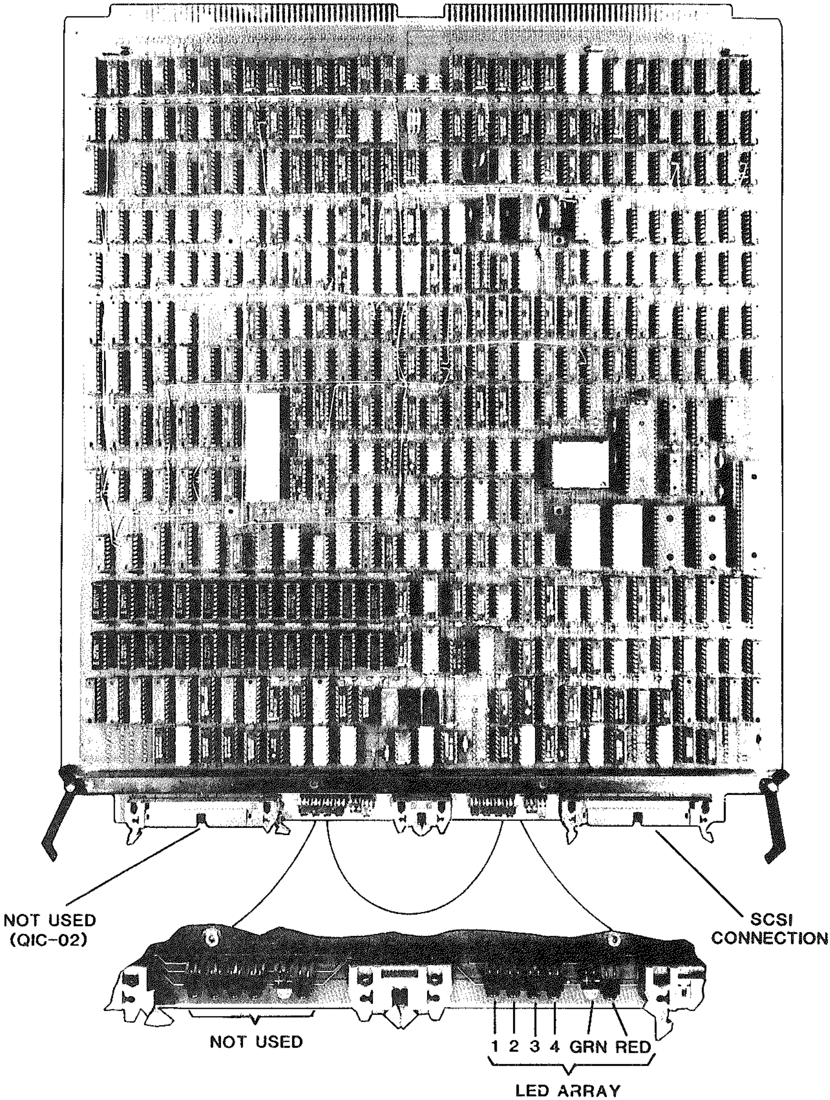


FIGURE 6-20: MSTC CONTROLLER LEDS

- Power-up reset has occurred.

- Double-Bit memory errors have been detected during normal system operation, or as a result of self-verification tests initiated by a SYSCLR, or OCP '17.

- More than 16 single-bit memory errors have been detected during one minute of normal system operation, and a subsequent double-bit error has been detected.

With none of the above conditions true, tests are executed in Non-Destructive Mode if self-verification is initiated by a SYSCLR or an OCP '17.

Table 6-29 lists MSTC self-verification tests. Those tests executed in Destructive Mode only are marked with an asterisk. The first series of tests executed, called General Tests, test both the disk and tape portions of the board. Therefore, if a failure is detected the same error code is displayed in both the disk and tape LEDs. Following the General Tests are a series of SCSI-only tests. A failure of the SCSI-only tests would be indicated in the SCSI LEDs, but not the unused LEDs.

If any of the MSTC self-verification tests fail, replace the controller. Indicate the failing self-verification test on the Failure Report Tag.

TABLE 6-29: MSTC SELF-VERIFICATION TEST LED DESCRIPTIONS

TEST SERIES	CODE HEX	CODE BINARY	DESCRIPTION
General Tests: (Both Sets of LEDs)	F	1111	Init_Prior
	7	0111	PROM Checksum Test
	B	1011	Init_Middle
	3	0011	Refresh Timer 0 Test
	D	1101	Init_Final
	5	0101	*SRAM Test
	9	1001	*DRAM Error Correction Logic Test
	1	0001	*DRAM Test
	E	1110	ECC_NMI
	6	0110	OTA Interrupt Handling Test
	A	1010	Non-Maskable Interrupt Test
	2	0010	Timer 1 and 2 Test
	C	1100	Input FIFO Test (Host to MSTC)
	4	0100	Output FIFO Test (MSTC to Host)
	8	1000	SCC Test
SCSI Only Tests: (SCSI LEDs)	A	1010	Tape Flop Check
	2	0010	*Tape Register File Test
	C	1100	Tape Interrupt (INT 0) Test
	4	0100	Tape DMA (Channel 0) Test
	8	1000	SCSI Interface Chip Test

6.3.8.1.2 Using MSTC Status Indicators

During normal system operation, data representing the status of the disk and tape drives is displayed in the 4-LED array corresponding to each device.

The MSTC monitors the number of single-bit memory errors occuring for both the disk and tape portions of the controller. If more than 16 single-bit errors are detected during one minute of system operation the MSTC sets an internal latch and turns on the DRAM Warning LED (LED 3) for the device on which the errors were detected.

Once the DRAM Warning LED has been turned on the system continues to operate, but in a degraded mode due to the large number of correction cycles required. System operation continues in degraded mode until the fault is removed, or a double-bit error is detected.

The MSTC also monitors the status of the SCSI Select, Attention, and Busy lines, displaying the data in LEDs 0, 1, and 2 of the disk LEDs, respectively. ON indicates that the state being monitored is false. Table 6-30 provides a description of MSTC SCSI Interface LEDs.

TABLE 6-30: MSTC SCSI INTERFACE LED DESCRIPTIONS

LED				MEANING
1	2	3	4	
x	x	x	ON	Board Running in Degraded Mode (DRAM Warning LED)
ON	x	x	x	Device Not Selected
x	ON	x	x	Interface Not At Attention
x	x	ON	x	Device Not Busy

6.3.8.1.3 Decoding Tape Drive Status Words

The MSTC maintains status words, STATUS WORD I and STATUS WORD II, that are accessible by issuing an OTA '02 with the appropriate bit set, followed by an INA '00 to copy the contents to the CPU A register.

These status words are defined in the following paragraphs:

TAPE STATUS WORD I

Status Word I, defined in Table 6-31 describes the operation that has just completed. To access the status word, use an OTA '02 with bit 1 set.

TABLE 6-31: TAPE STATUS WORD I BREAKDOWN

BIT	VALUE	MEANING	DESCRIPTION
1	1	Read Error	The drive failed to recover data from tape during a read operation.
	0	Write Error	
2	1	Runaway Tape/End of Recorded Media	No data was seen on tape after read operation started. The tape drive has sensed the end of recorded data (25 ft. of tape have passed with no data present). If this condition is detected from BOT (bottom of tape) a blank tape is indicated.
3	Always 0		
4	Always 0		
5	1	Record Length Mismatch	DMX end-of-range and end-of-chain occurred while reading a record and end of data was not detected.
6	1	Error or Fault	Bit set if selected drive is not connected.
7	1	Uncorrectable Write Error	Read after write error detected during 7 retries.
8	1	File Mark Detected	File mark is detected during a Read Record or Read File Mark operation.
9	1	Drive Ready	Tape drive is powered up, online, and is not busy.
10	Always 1 when BIT 9 is 1		
11	1	Logical EOT	Tape has passed logical EOT (end of tape).
12	1	Rewinding	
13	1	Load Point	
14	1	File Protected	Media is write protected.
15	1	Error	Drive detected DMX overrun or MSTC FIFO parity error.
16	1	Erasing to EOT	

TAPE STATUS WORD II

Tape Status II, defined in Table 6-32, is an extension of Status Word I. It provides additional operating information as well as further definition of errors reported in Status Word I.

To access this status word, use an OTA '02 with bit 5 set.

TABLE 6-32: TAPE STATUS WORD II BREAKDOWN

BIT	VALUE	MEANING	DESCRIPTION
1-3		GCR Density	1 0 0 = PE 1 0 1 = GCR 1 1 0 = NRZI 1 1 1 = DPE 0 1 1 = Default to Drive Control Panel
4	1	Speed	Indicates 100 ips selected.
5	1	Illegal Command	Tape operation illegal for MSTC controller is requested. Examples are a Write to a file-protected drive, or an operation directed to a non-existent drive.
6	0	Mode	Indicates non-buffered mode (default).
7	1	Correctable Error	Tape drive has performed a successful error correction on a block of data. Used by diagnostic only.
8-11	Always 0	Unused	
12	1	Error	Fatal MSTC memory error or SCSI hung. Requires OCP '17 to restart.
13	1	Invalid OTA	An invalid OTA was received and rejected.
14	1	Tape Drive Fault/ Tape Drive Reset	
15	1	Self-verification Failure in MSTC	Indicates a self-verification failure in the tape portion of the MSTC after an initialization or power up.
16	1	Tape Operation Aborted	A tape operation was aborted. (Used by diagnostics only.)

6.3.8.2 Troubleshooting Disk Subsystem Failures

The following subsections contain information to identify disk subsystem failures:

- IDC1 LED Display
- Disk Drive Status Words

If the information in this section indicates the disk controller is operating correctly, refer to 496 Megabyte Fixed Module Disk Subsystem Service Procedures Manual (SPM470) or to 770 Megabyte Fixed Storage Disk Subsystem Service Procedures Manual (SPM390) for additional disk drive troubleshooting information and corrective action procedures.

6.3.8.2.1 IDC1 Controller LEDs

Six LEDs on the controller board report faults and status (see Figure 6-21). The LEDs can be lighted in four general patterns to indicate the status of the board. Refer to Table 6-33 for the general conditions and their meanings.

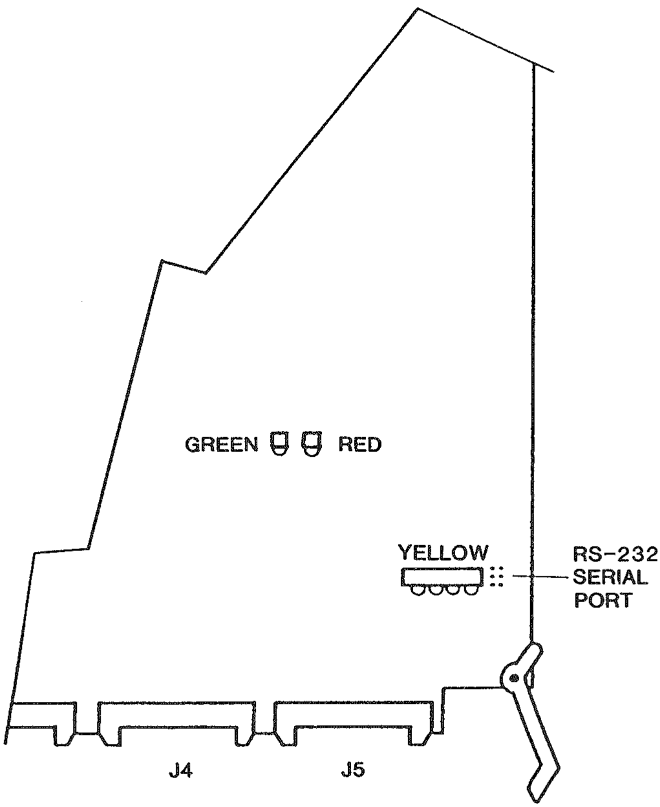


FIGURE 6-21: IDC1 CONTROLLER LEDS

TABLE 6-33: CONTROLLER BOARD STATUS INDICATORS

CONDITION	MEANING
Green and Red Lights Blinking	Board is executing self-verify tests
Green only on	Board is operational
Red only on	Board rev is not correct
Red and Yellow on	Board failed self-verify test

At system power-up, the controller runs a series of self-verify tests. After successful completion of these tests, the controller is ready to run in channel command mode.

The Yellow and Red LEDs enable you to interpret the cause of a power up or operation fault. Use Table 6-34 to interpret power-up problems. If you suspect a controller error during operation, refer to Table 6-35 to interpret the cause.

NOTE

With the LEDs toward you, the Most Significant Bit (MSB) is LED 4 and the Least Significant Bit (LSB) is LED 1, as shown in Figure 6-21. Refer to Tables 6-34 and 6-35 for specific patterns.

TABLE 6-34: POWER-UP SELF-VERIFY FAILURE REPORTS

TEST NUMBER	LEFT LED BANK					RIGHT LED BANK		
	Y	Y	Y	Y	Y	G	Y	R
TEST 01	OFF	OFF	OFF	OFF	ON	ON	OFF	ON
TEST 02	OFF	OFF	OFF	ON	OFF	ON	OFF	ON
TEST 03	OFF	OFF	OFF	ON	ON	ON	OFF	ON
TEST 04	OFF	OFF	ON	OFF	OFF	ON	OFF	ON
TEST 05	OFF	OFF	ON	OFF	ON	ON	OFF	ON
TEST 06	OFF	OFF	ON	ON	OFF	ON	OFF	ON
TEST 07	OFF	OFF	ON	ON	ON	ON	OFF/ON	ON
TEST 08	OFF	ON	OFF	OFF	OFF	ON	SAME	ON
TEST 09	OFF	ON	OFF	OFF	ON	ON	OFF/ON	ON
TEST 0A	OFF	ON	OFF	ON	OFF	ON	SAME	ON
TEST 0B	OFF	ON	OFF	ON	ON	ON	SAME	ON
TEST 0C	OFF	ON	ON	OFF	OFF	ON	SAME	ON
TEST 0D	OFF	ON	ON	OFF	ON	ON	SAME	ON
TEST 0E	OFF	ON	ON	ON	OFF	ON	OFF/ON	ON
TEST 0F	OFF	ON	ON	ON	ON	ON	OFF/ON	ON
TEST 10	ON	OFF	OFF	OFF	OFF	ON	SAME	ON
TEST 11	ON	OFF	OFF	OFF	ON	ON	SAME	ON
TEST 12	ON	OFF	OFF	ON	OFF	ON	SAME	ON
TEST 13	ON	OFF	OFF	ON	ON	ON	SAME	ON
TEST 14	ON	OFF	ON	OFF	OFF	ON	SAME	ON
TEST 15	ON	OFF	ON	OFF	ON	ON	SAME	ON

TABLE 6-35: OPERATIONAL ERROR CONDITIONS

ERROR CONDITION	LEFT LED BANK Y	Y	Y	Y	Y	RIGHT LED BANK G	Y	R
Microprocessor Divide Error	OFF	OFF	OFF	OFF	ON	OFF	SAME	ON
Microprocessor Single Step Int	OFF	OFF	OFF	ON	OFF	OFF	SAME	ON
NMI - power fail	OFF	OFF	OFF	ON	ON	OFF	SAME	ON
Microprocessor Brk. Point Int	OFF	OFF	ON	OFF	OFF	OFF	SAME	ON
Microprocessor Into Overflow	OFF	OFF	ON	OFF	ON	OFF	SAME	ON
Microprocessor Bound Exceeded	OFF	OFF	ON	ON	OFF	OFF	SAME	ON
Microprocessor Invalid Opcode	OFF	OFF	ON	ON	ON	OFF	SAME	ON
Microprocessor Proc. Extension	OFF	ON	OFF	OFF	OFF	OFF	SAME	ON
Microprocessor Proc. Extension Error	OFF	ON	OFF	OFF	ON	OFF	SAME	ON
Microprocessor Null ISR	OFF	ON	OFF	ON	OFF	OFF	SAME	ON
ECC Error Overflow	OFF	ON	OFF	ON	ON	OFF	SAME	ON
NMI - Parity	OFF	ON	ON	OFF	OFF	OFF	SAME	ON
NMI - dram multibit	OFF	ON	ON	OFF	ON	OFF	SAME	ON

6.3.8.2.2 Disk Status Words

Table 6-36 defines disk status words reported by the IDC1 controller, the Model 4735 disk drive and the Model 4835 disk drive.

TABLE 6-36: DISK STATUS WORDS

BIT	DESCRIPTION
Bit 1 -	This status bit is tied high in the controller and is always set to a 1 to indicate that the disk status word is valid. If this status bit is not set, replace the disk controller.
Bit 2 -	The disk controller detected a loss of data between the disk drive and the controller's internal memory. One possible cause of this error is single-bit correctable memory errors within the controller. If this status bit is set, replace the disk controller.
Bit 3 -	This status bit is generated in the disk drive as Bus In Bit 4 (BIB4) and is set whenever the disk drive is write protected via either the operator panel Write Protect button or the Control PCB jumper plug or when a fault condition exists on the disk drive (remember that attempting to write on a write protected disk generates a fault). If this status bit is set along with status bit 16 (Disk Not Ready), troubleshoot the failure as a disk drive fault. If only status bit 3 is set and the drive is not write protected via the operator panel button or the Control PCB jumper plug, troubleshoot this failure as an interface problem.
Bit 4 -	During a read operation the controller determined that the 32-bit CRC field of the record being read did not compare with the CRC computed by the controller. The software retries the operation. If after 10 attempts the error has not been corrected the software reads the record into the system memory and attempts to perform an error correction. If the attempt is successful an error message is displayed along with the message 'WORDNO ERROR ERROR' to indicate that the error was corrected. If the correction attempt was not successful an error message is displayed with the message 'UNCORRECTABLE'. If the checks point to the same track, head, and record a badspot is indicated. Run FIX_DISK using the -ADD_BADSPOT option to add the record to the BADSPOT file. If the checks point to random record locations a R/W failure is indicated. Suspect the I/O PCB, R/W PCB, Control PCB, and the HDA. Check the power supply for ripple.
Bit 5 -	During a DMA operation the disk controller generates and checks parity on the data path between the system backplane I/O drivers and receivers and the controller's internal memory. If this status bit is set, a parity error was detected. Replace the disk controller.

TABLE 6-36: DISK STATUS WORDS (CONT.)

BIT	DESCRIPTION
Bit 6 -	If this status bit is set, a record header check is indicated. A header check can be generated for one of two possible reasons: 1. During a read, write, or format operation the 16-bit CRC field within the record header did not match the CRC computed by the disk controller. 2. The disk controller did not find a match for the requested record address within 16 revolutions of the disk platters. If the checks point to the same track, head, and record a badspot may be indicated. Run FIX_DISK using the -ADD_BADSPOT option to add the record to the BADSPOT file. If the checks point to random record locations first verify the disk servo circuits, since a header check results if the disk heads are located on the incorrect track. Status bits 13 and/or 14 may be set along with status bit 6 if a servo problem exists. If the servo circuits are operating correctly suspect a disk drive read failure or the disk controller and cables.
Bit 7 -	If a disk controller is operating in ICOP mode when a bad record is found the controller marks the record bad and relocates the data to an alternate record. On the next attempt to access the original record the controller is directed to the alternate record to obtain the data. The operation is transparent to Primos. If a record is relocated by a controller running in ICOP mode, but is later accessed by a disk controller running in 4005 mode, status bit 7 is set and the controller is not able to locate the alternate record. (If a problem is detected with ICOP operation the controller automatically reverts to 4005 mode.) This function is not supported at this time and therefore status bit 7 is always set to a 0. (****THIS MAY CHANGE****)
Bit 8 -	This status bit indicates that an error occurred when the system CPU attempted to down-line load the ICOP protocol into the disk controller. This function is not supported at this time and status bit 8 is always be set to 0.
Bit 9 -	The disk controller is capable of detecting and correcting single-bit errors within the controllers internal memory. If more than 16 single-bit errors are detected per minute the controller sets this status bit to indicate that it is operating in the degraded mode. The controller also indicates a degraded mode of operation in its status LEDs. Status bit 10 may be set along with status bit 9. If status bit 9 is set, replace the disk controller.

TABLE 6-36: DISK STATUS WORDS (CONT.)

BIT	DESCRIPTION
Bit 10 -	This status bit is set to indicate that the disk controller has detected, and corrected, a single-bit error within its internal memory. If more than 16 single-bit errors are detected per minute status bit 9 is set along with this status bit. If errors are very intermittent no action need be taken at this time. If the errors become frequent replace the disk controller.
Bit 11 -	This status bit is used with dualported disk drives only and is generated by the disk drive, as BUSY. If this status bit is set the disk drive was busy servicing another disk controller when this controller requested service. Otherwise this status bit is set to 0.
Bit 12 -	This status bit is not used and is always set to 0.
Bit 13 -	This status bit is generated within the disk drive as BIB1. If set, the disk drive has not yet completed a seek channel order or has drifted off cylinder. This bit may be set along with bit 14 (SEEK ERROR). An attempt to read or write while bit 13 is set causes the disk drive to generate a Read or Write and Off Cylinder fault, setting disk status word bits 3 and 16.
Bit 14 -	This status bit is generated by the disk drive as BIB2 and indicates that a SEEK ERROR occurred during a normal seek or a RTZ seek operation. A seek error can be the result of several conditions: 1. The controller specified a cylinder address greater than 710. 2. The disk drive head positioner could not complete a normal seek operation within the allowed 60 millisecond time period. 3. The disk drive head positioner could not maintain the heads directly over the requested cylinder. 4. A fault occurred during the seek operation. If the disk drive SEEK ERROR LED is ON, refer to the appropriate service rocedures manual to troubleshoot the disk drive, otherwise suspect the disk controller. If a read or write operation is attempted when a seek error exists a Read or Write and Off Cylinder fault is generated causing disk status word bit 3 and 16 to be set.

TABLE 6-36: DISK STATUS WORDS (CONT.)

BIT	DESCRIPTION
Bit 15 -	This status bit is generated by the disk controller and indicates that the controller has detected that two or more disk drives have responded to the same Select channel order. Verify that each disk drive contains a unique unit address plug. If all drives are uniquely addressed suspect the disk drive's I/O Control board, the disk controller, and the interconnecting cables. If a Select channel order, fails the controller's status line receivers are not enabled. This sets all disk drive generated status bits to one (e.g., disk status word = 120047).
Bit 16 -	This status bit is generated in the disk drive as BIB0 (UNIT READY) and indicates the disk drives availability to accept commands. If this bit is set along with bit 3 check the disk drive for faults. A fault can be generated by the following conditions: 1. Read and write operations were attempted simultaneously. 2. A read or write operation was attempted and the drive was off cylinder. 3. The first seek failed. 4. Write fault (No write clock present, disk write protected, no write data transitions, or no arm enable signal active when the write gate was active, or an open head). 5. An attempt was made to write and the disk drive was write protected. 6. More than one head was selected during a write operation, 7. An operating voltage is below satisfactory limits or the actuator current exceeds an allowable limit. In addition to the above fault conditions, bits 3 and 16 is set if a loss of motor speed is detected by the disk drive. If the disk drive is faulted or a motor speed error exists refer to the appropriate disk drive service procedures manual for troubleshooting procedures. If the drive is not faulted suspect the disk drive I/O Control board, disk controller, and the interconnecting cables.

6.3.8.2.3 Disk Errors Reported by the Disk Driver Software

Table 6-37 defines common disk errors reported by the driver software:

TABLE 6-37: COMMON DISK ERRORS

ERROR	DESCRIPTION
177777 -	CRA Read does not match the CRA requested. During a read, write, or format operation it was determined by the disk driver software that the Current Record Address (CRA) just read did not match the address of the requested record. The physical disk record was read successfully if no header or read checks were reported, but the logical disk record within the data portion of the physical record was read incorrectly. Suspect a corrupted disk media, R/W failure, or disk controller problem.
177776 -	Controller not ready.
177775 -	Parity Error During DMX.
177774 -	No controller is available for this process. An attempt by the disk driver software to execute an INA '11xx to the disk controller requested by a process did not succeed. Verify that the proper disk controller was selected by the operator. In no operator errors have been made replace the disk controller.
177773 -	Disk Controller Hung, Disk Drive Hung, or the system has been Warmstarted. This error message is the result of a best guess by the disk driver software to determine the cause of a failure and can be generated under three conditions: 1. After the completion of each normal seek operation the disk driver software checks each disk drive connected to the controller, beginning with unit 0, to verify that it is not hung. This is accomplished by first checking the drives work list for any pending requests. If no requests are pending, the drive is skipped and the software moves on to the next unit. If a request is pending, the software checks whether the drive is marked as busy. If no request is pending, the drive is skipped and the software moves to the next unit. If the drive is marked busy, the software checks the amount of time elapsed since the request was initiated (the start time for a request is stored on the Queue Request Block for that request). If the time elapsed is greater than 2 seconds the system flags the error and clears any disk drive faults by issuing a RTZ seek to the hung drive. After all disk drives are checked, the software driver attempt to initiate I/O. This error can result from a disk servo problem, from a failing disk controller, or a bad cable.

TABLE 6-37: COMMON DISK ERRORS (CONT.)

	2. During a read or write request the software checks the amount of time elapsed since the beginning of the request. This is done by sending an INA '17xx (Input the Order Address Register) to the controller. If controller does not respond indicating a successful completion of the INA within 2 seconds the controller is considered hung. It is initialized (OCP '17xx), the error is flagged, and the software returns to the calling routine to retry the operation. Replace the controller if the error persists. 3. If the system is warmstarted, the disk controller is initialized and, as a result, loses track of important information (for instance the content of the OAR). If this error occurs during a R/W operation the error is flagged and the software returns to the calling routine to retry the operation. If the error occurs during a seek operation it is treated as a Failing Seek (see 177772 below).
177772 -	A Seek is Failing. While waiting for a seek to complete the disk driver software determined that the disk controller has been busy for more than 2 seconds. The software checks to see if the disk drive has a request pending in its work list. If a request is pending, it determines if the disk drive is marked busy. If both of these conditions are true, the software flags an error indicating that the seek is failing, issues a RTZ seek to attempt to clear any disk faults that may exist, and attempts to restart the seek operation. If the seek has not completed successfully after 10 attempst, the software gives up. Suspect the disk controller first, and then the disk drive.
177771 -	An error occurred when the disk controller attempted to enter ICOP mode. When the Enter ICOP channel order was sent to the disk controller no response was made within 10 seconds, or the controller ID word returned indicating a failure to enter ICOP mode. This message is only supported at Rev 20.2 of Primos and above. Replace the disk controller if this error occurs.
177770 -	The operation code contained in the Queue Request Block for this request is illegal for 4005 mode of operation. The only legal disk operations for a 4005 mode controller are Seek, Read, Write, and Format. This is a software problem.

6.3.9 TROUBLESHOOTING SYSTEM PERFORMANCE DEGRADATION

Refer to Figures 6-22, 6-23, and 6-24, and Tables 6-38, 6-39, and 6-40 for standard procedures to troubleshoot Model 4050/4150 performance problems.

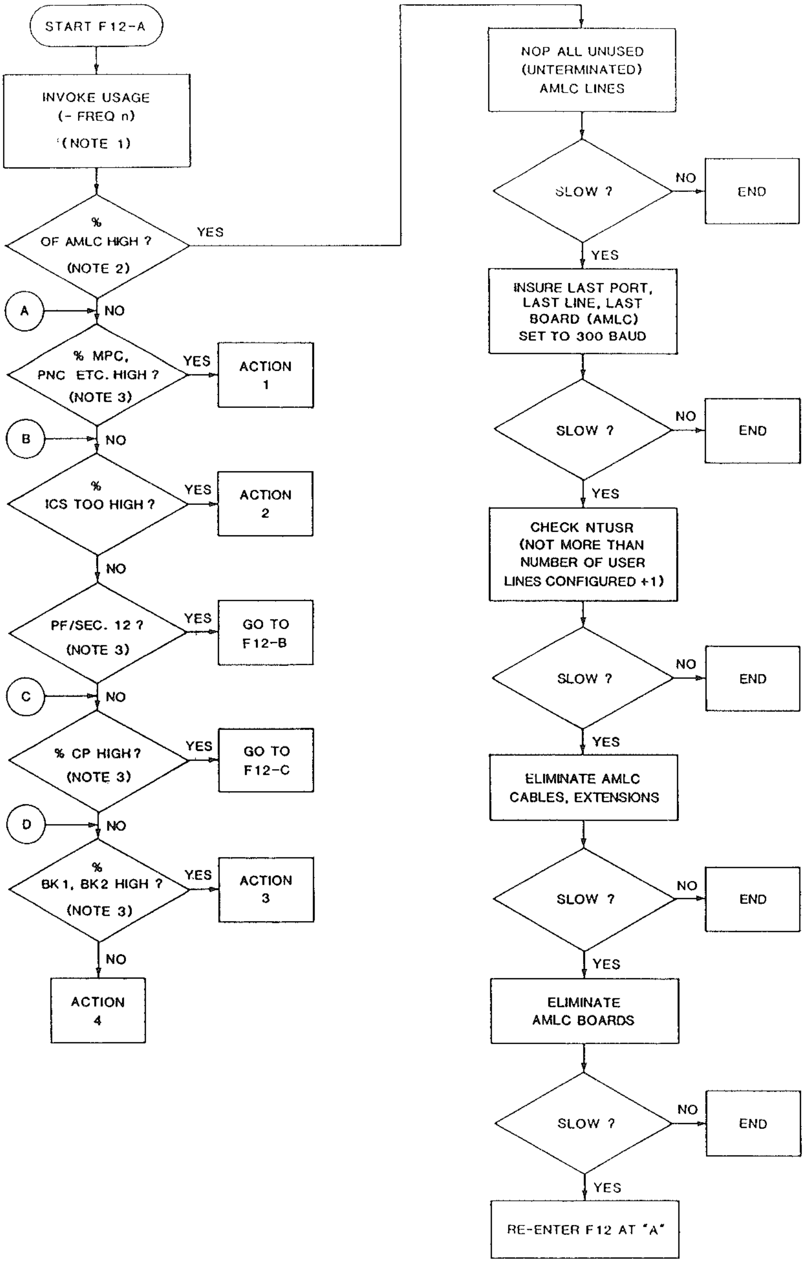


FIGURE 6-22: SLOW SYSTEM FLOWCHART A (F12-A)

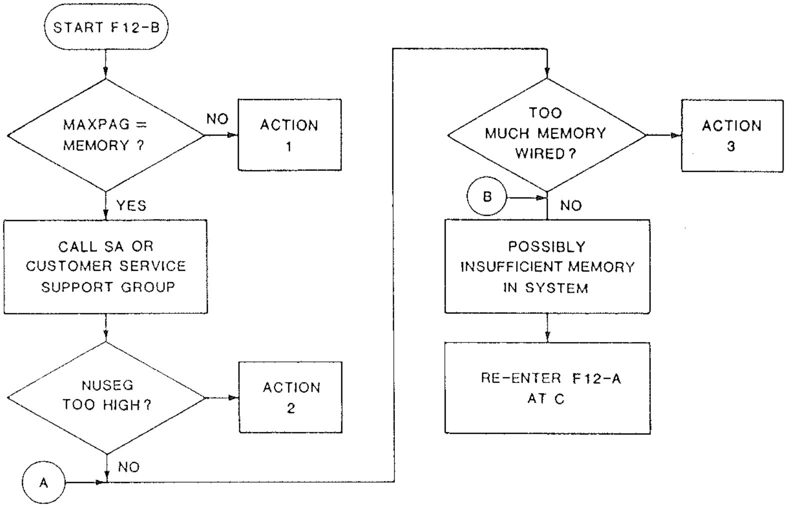


FIGURE 6-23: SLOW SYSTEM FLOWCHART B (F12-B)

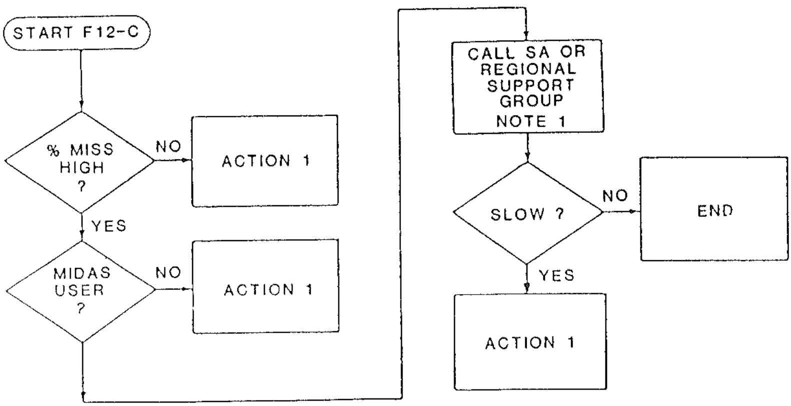


FIGURE 6-24: SLOW SYSTEM FLOWCHART C (F12-C)

TABLE 6-38: SLOW SYSTEM - STEP A (F12-A)

CONDITIONS	
1. System appears to have slowed down drastically. 2. System running PRIMOS. 3. No known hardware problems.	
ACTIONS	**NOTES**
1. Replace the appropriate controller (if no change, go to B in flowchart F12-A).	1. Refer to Service Manual SSG080 for USAGE.
2. Replace the ICS controller.	2. Snapshot of USAGE should be done while the system is <u>not</u> running slow. Refer to SSG080 for more information.
3. Increase MAXSCH to a value between 4 and 7. (If no change, perform step 4).	
4. Rule out CPU (clean edge connectors, reseat ICs, replace boards). If no change, perform Tape Dump and contact Regional Support.	3. AMLC should run approximately 1 to 1.2% per AMLC board.

TABLE 6-39: SLOW SYSTEM - STEP B (F12-B)

CONDITIONS	
1. Directed to this procedure from troubleshooting flowchart F12-A. 2. System appears to have slowed down drastically. 3. System running PRIMOS. 4. No known hardware problems.	
ACTIONS	**NOTES**
1. Set MAXPAG (in CONFIG) to equal physical memory in the system. (Octal 200 per quarter Megabyte.)	None.
2. With the aid of Regional Support or a Systems Analyst, determine if NUSEG <u>can</u> be lowered. If so, lower NUSEG. If a lower NUSEG has no effect, have the Analyst or Regional Support group discuss Alternate Paging. If alternate paging is impossible, or makes no difference, reenter F12-A at A.	
3. Check for AMLBUF statements entered properly. If correct, or makes no difference, re-enter F12-A at B.	

TABLE 6-40: SLOW SYSTEM - STEP C (F12-C)

CONDITIONS	
1. Directed to this procedure from troubleshooting flowchart F12-B. 2. System appears to have slowed down drastically. 3. System running PRIMOS. 4. No known hardware problems.	
ACTIONS	**NOTES**
1. Reenter flowchart F12-A at location D. Snapshot of USAGE should be done while the system is not running slow for comparison. (Refer to SSG080 for details.)	1. After Systems Analyst or Regional Support Group determines MIDAS is or is not at fault, continue with this flowchart.

6.4 TROUBLESHOOTING WITH DIAGNOSTIC MESSAGES AND LEDS

Check system messages and LEDs for information. This section provides message descriptions and possible corrective actions. System messages and LEDs include:

- VCP-V LEDs, and Error and Warning Messages
- Diagnostic LEDs on System Power Supplies
- Diagnostic LEDs on the Intelligent Disk Controller (IDC1)
- Diagnostic LEDs on the Minnow SCSI Tape Controller (MSTC)
- Diagnostic LEDs on the Intelligent Communications Controller (ICS3)
- Diagnostic LEDs on the PNC-II

6.4.1 VCP-V ERROR AND WARNING MESSAGES

The VCP-V provides the following messages:

- VCP-V self-verify messages
- System Error and Warning Messages

6.4.1.1 VCP-V Self-Verify Messages

When the VCP-V fails a self-verification test, the VCP LEDs display the binary test number that failed, and the VCP prints an error message on the system console. Table 6-41 is a summary of each test and related error messages.

TABLE 6-41: VCP-V LED MESSAGES

TEST	LED DISPLAY: 4 3 2 1	FAILURE/ERROR MESSAGE NUMBER*
	1 1 1 1	Z80 CPU not functioning, unable to initiate self-test
	0 0 0 1	Green LED on, Red LEDs off: All tests passed.
VCP-V Memory	0 0 1 0	Failed EPROM checksum test.
	0 0 1 1	Failed RAM data test/
	0 1 0 0	Failed RAM address test/ ERR001 through ERR007
Environmental Test (Initial)	0 1 0 1	Failed Environmental Test (initial test) ERR070 - ERR076
System Power Test	0 1 1 0	Failed PDU and Power Supply Test (Initial Test) WRN504, ERR08n
Environmental Test	0 1 1 1	Failed Environmental Sensor Test (Second Test) ERR070 - ERR075
Floppy Disk Check Sector Test	1 0 0 0	Failed Floppy Drive Test, ERR030, WRN000
System Validation and Application Software Test	1 0 0 1	Failed System Check
	1 0 1 0	Failed to Load Application Software ERR03X, ERR040 - ERR042
Time-of-Day Clock	1 0 1 1	Failed Real Time Test, ERR800

In addition, the Diagnostic Processor performs the following tests only at power up. The group of four LEDs does not indicate a failure in these tests, but Error Messages are sent to the console*:

1. Loading the System Configuration

2. System Power Supplies (Second Test)

3. Time-of-Day Clock (Second Test)

4. CPU(s) Control Store Verification

* Refer to Table 6-42 and 6-43 for error and warning messages and corrective actions.

6.4.1.2 System Error and Warning Messages

During autoboot and during normal system operation, the VCP-V displays two types of mesages:

- System Error Messages
- System Warning Messages

These messages display on the system console in full or brief mode.

If a system error message displays, refer to Table 6-42 for a description of the error code and possible corrective measures. Refer to Table 6-43 for a description of warning messages and corrective actions.

NOTE

System warning messages can signal an intermittent problem. If a warning message appears more than once, be sure to take the corrective action indicated in Table 6-42.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS

NOTE

Messages with an asterisk are written to the history disk.

DEFINITION	ACTION
ERR000: Diagnostic Processor memory error An error is detected during a checksum verification of the VCP-V's bootstrap PROM memory at board location 25E.	1. Replace the VCP-V.
ERR001: Diagnostic Processor memory error An error is detected during a verification of the SRAM at board location 28E.	1. Replace the VCP-V RAM at location 28E. Refer to RAM Removal/Replacement procedures in Chapter 7. 2. If the error still occurs, replace the VCP-V PCB.
ERR002: Diagnostic Processor memory error An error is detected during a verification of the SRAM at board location 31E.	1. Replace the VCP-V RAM at location 31E. Refer to RAM Removal/Replacement procedures in Chapter 7. 2. If error still occurs, replace VCP-V PCB.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DEFINITION	ACTION
ERR003: Diagnostic Processor memory error An error is detected when performing a verification of the SRAM at board location 34E.	1. Replace the VCP-V RAM at location 34E. Refer to RAM Removal/Replacement procedure in Chapter 7. 2. If error still occurs, replace the VCP-V PCB.
ERR004: Diagnostic Processor memory error An error is detected during a verification of the SRAM at board location 37E. This component is a FRU and is the most likely cause of the failure.	1. Replace the VCP-V RAM at location 37E. The RAM replacement procedure is located in Chapter 7. 2. If error still occurs, replace the VCP-V PCB.
ERR005: Diagnostic Processor memory error An error is detected during a verification of the SRAM at board location 40E.	1. Replace the VCP-V RAM at location 40E. Refer to RAM Removal/Replacement procedures in Chapter 7. 2. If error still occurs, replace the VCP-V PCB.
ERR006: Diagnostic Processor memory error An error is detected during a verification of the SRAM at board location 43E.	1. Replace the VCP-V RAM at location 43E. Refer to RAM Removal/Replacement procedures in Chapter 7. 2. If error still occurs, replace the VCP-V PCB.
ERR007: Diagnostic Processor memory error An error is detected during a verification of the SRAM at board location 46E.	1. Replace the VCP-V RAM at location 46E. Refer to RAM Removal/Replacement procedures in Chapter 7. 2. If error still occurs, replace VCP-V PCB.
ERR030: Diagnostic Processor Floppy Disk read error An error is detected while trying to read and verify the disk check from track 34, sector 31 of the floppy disk.	1. Replace the floppy disk with a known good disk. 2. Verify correct operation of the drive. 3. If the error persists replace the VCP-V.
ERR031: Diagnostic Processor Floppy Drive read error An error occurred while trying to validate the floppy disk for application software load. The floppy disk is defective and should be replaced.	1. Refer to ERR030.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DEFINITION	ACTION
ERR032: Diagnostic Processor PROM Card read error Floppy disk format identifier error. The floppy disk does not contain a valid format identifier field. The floppy disk should be replaced.	1. Refer to ERR030.
ERR033: Diagnostic Processor Floppy Drive read error Floppy disk contains wrong software revision. Revision level of VCP-V code contained on floppy disk does not match the current VCP-V hardware revision level.	1. Verify the revision levels between the VCP-V hardware and the floppy disk. If revisions do not match, update as appropriate.
ERR040: Diagnostic Processor Floppy Drive read error A read error occurred while trying to read the VCP-V application software.	1. Refer to ERR030.
ERR041: Diagnostic Processor Floppy Drive read error The floppy disk does not contain VCP-V application software.	1. Replace the Floppy disk. Could be bad floppy, or wrong floppy.
ERR070: Diagnostic Processor detects overtemperature on its own board VCP-V detects overtemperature condition on the VCP-V PCB during self-verification.	1. Verify that cabinet blower assembly is functioning. 2. Verify that room temperature is within acceptable limits. 3. Verify that air filter, is not clogged. 4. If problem persists, replace the VCP-V.
ERR073:Diagnostic Processor detects CPU board 1 over-temperature VCP-V detects an overtemperature condition on the CPU CMI-Board during self-verification.	1. Verify that CPU cabinet blower is functioning. 2. Verify that room temperature is within acceptable limits. 3. Replace the CPU CMI-Board. 4. If the problem persists, replace the CPU E-Board. 5. If problem persists, replace the VCP-V PCB.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DEFINITION	ACTION
ERR077 Diagnostic Processor detects improper Air Flow 2 VCP-V detects insufficient air flow in the CPU cabinet during self-verification.	1. Verify that CPU cabinet blower is functioning. 2. Verify that the air flow sensor is functioning. 3. If the problem persists, replace the VCP-V PCB.
ERR08n: Diagnostic Processor detects a power supply failure VCP-V detects a system power supply failure during PDU sequencing. The failing supply is indicated by "n".	1. Refer to Troubleshooting Power-Up Problems in this chapter. 2. If the problem persists, replace the VCP-V.
*ERR100: Failure detected in Microdiagnostic "<file>", Test <nnnn> A microdiagnostic test has failed. The most likely failing FRUs are indicated in the error printout. The error printout displays only when the system is in MO FULL mode.	1. Suspect the FRUs listed in the error message, in the order displayed.
ERR111: Microdiagnostic "<filename>" not found A copy of the microdiagnostic microcode is not found during load control store sequence.	1. Use the CP mode DIR command to verify that the file <filename> (file type M) exists on the floppy disk. 2. If the file does not exist, replace the floppy disk. 3. If the file exists, replace the VCP-V.
ERR112: File <filename> not found The given PMA file is missing from the floppy disk directory during LOAD PMA command.	1. Use the CP mode DIR command to verify that the file <filename> (file type P) exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.
*ERR114: Instruction Set Microcode not found Copy of the instruction set microcode verification was not found during the Auto-boot to PRIMOS sequence.	1. Use the CP mode DIR command to verify that the file CPU_UCODE (file type B) exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
*ERR115: Decode Net File not found Copy of the decode net is not found during Autoboot or during execution of LDNET or VFNET commands.	1. Use the CP mode DIR command to verify that the file DECODE_NET (file type D) exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.
*ERR116: PRIMOS Boot routine file not found Copy of the PMA BOOT file is not found during the AutoBoot to PRIMOS sequence.	1. Use the CP mode DIR command to verify that the file BOOT_CODE (type P) exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.
ERR117: CPU Decode Net Verification Error Discrepancy between CPU's loaded Decode Net and the image in the floppy disk.	1. Use CP mode DIR command to verify that a file of type D exists on the floppy diskette. 2. Follow steps 2 and 3 as outlines for ERR111.
*ERR118: Decode Net file <filename> not found> Copy of the indicated decode net file was not found during the AutoBoot to PRIMOS sequence.	1. Use the CP mode DIR command to verify that the file <filename> (type D) exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.
ERR119: File <filename> is not a Valid Decode Net file The filename given in the command LDNET or VFNET exists on the floppy disk, but is not a valid (type D) decode net file.	1. Enter a LDNET or VFNET command with a valid decode net filename. 2. Follow the same procedure as described in ERR111.
ERR120: File "<filename>" not a valid microcode file The filename given in the command LOADM, VERIFYM, RUND, RUNDC is not valid (file type M, B, or S.)	1. Enter a LOADM, RUND RUNDC or VERIFYM command with a valid microcode filename. 2. Follow the same procedure as described in ERR111.
ERR121: File "<filename>" not a valid PMA file The filename given in the command RUNTM or LOADTM is not valid (type P).	1. Enter a RUNTM or LOADTM command with a valid PMA filename. 2. Follow the same procedure as described in ERR111.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
ERR122: No Filename given A CP command that requires a filename was entered without a filename.	1. Re-enter the command with a filename.
*ERR130: CPU Recoverable Verification error on file "<filename>" An error occurred and was successfully corrected when the VCP-V retried the operation. Indicates a "soft" floppy disk error and possible transient hardware failure.	1. Replace floppy disk with a known good floppy disk. 2. Replace the VCP-V or the CPU.
*ERR131: CPU Verification error on file "<filename>" VCP-V detects control store microcode discrepancies when verifying microcode. System halts.	1. Refer to ERR130.
*ERR140: Configuration file not found Copy of the indicated configuration file was not found during the AutoBoot to PRIMOS sequence.	1. Use the CP mode DIR command to verify that the configuration file (type C) exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.
*ERR141: Invalid Configuration Table Entry During configuration table load, the VCP-V found a configuration number in non-volitile memory not in the required 0-15 range. Base config table is loaded automatically.	1. Refer to CP mode CONFIG command and load the correct configuration table for the system.
*ERR142: Invalid Configuration Table Loaded During configuration table load, the VCP-V loaded an invalid one. The VCP-V monitors only its own environmental sensor and the ON/INITIATE SHUTDOWN switch.	1. Refer to CP mode CONFIG command and load a valid configuration table for the system.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
*ERR143: Configuration Table not loaded During configuration table load, the VCP-V detected a floppy disk/ ID PROM mismatch. The VCP-V monitors only its own environmental sensor and the ON/INI-TIATE SHUTDOWN switch.	1. Determine if the disk or ID PROM is incorrect. 2. Replace the diskette with a proper revision level diskette. 3. Replace the ID PROM with proper revision level for the diskette.
ERR200: Fileread error on <filename> Copy of the indicated filename was not found during the AutoBoot to PRIMOS sequence.	1. Use the CP mode DIR command to verify that the indicated filename exists on the floppy disk. 2. Follow steps 2 and 3 as outlined for ERR111.
ERR201: Diagnostic Processor Floppy read error on directory sector The VCP-V is unable to read the directory information from the floppy disk.	1. Replace the floppy diskette with a known good floppy disk. 2. Replace the VCP-V PCB.
*ERR202: Unknown Central Processor System type VCP-V is unable to determine the processor type.	1. Replace the Floppy Disk with a known good floppy diskette. 2. Replace the system ID board. 3. Replace VCP-V.
ERR203: Floppy Drive has unknown format2. Replace floppy.	1. Reformat floppy diskette.
ERR205: Incorrect password entered The password entered isn't correct. This message appears any time a port is enabled. The password can be entered from the port in question only. The password is requested a maximum of three times after which the VCP-V disconnects the port.	1. Contact the local System Administrator for the correct password.
ERR208: Local 1 Terminal not enabled. The operator tried to use LOCAL1 when it was not enabled.	1. Use the CP mode ENABLE command to enable LOCAL1.
ERR209: Local 2 Terminal not enabled. The operator tried to use LOCAL2 when it was not enabled.	1. Use the CP mode ENABLE command to enable LOCAL2.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
*ERR300: CPU not responding Forcing Processor Check The VCP-V and the CPU are not communicating during the microcode load sequence.	1. Suspect the CPU CMI-Board. 2. Suspect the backplane.
*ERR301: CPU not responding Forcing Halt The CPU is not responding to VCP-V commands.	1. Refer to ERR300.
*ERR302: CPU not responding. Sysclring System	1. Refer to ERR300.
*ERR303: CPU not responding	1. Refer to ERR300.
*ERR304: CPU not responding during DMD transfer	1. Refer to ERR300.
*ERR308: CPU Verification error on Decode Net file <filename>	1. Replace the floppy diskette with a known good one. 2. If error persists, suspect the CPU CMI-Board, and VCP-V.
*ERR375: Verification error on file "<filename>", Word <nnnn> VCP-V detects control store microcode discrepancies when verifying microcode.	1. Replace the floppy disk with a known good floppy disk. 2. If error persists suspect the CPU and the VCP-V PCB.
*ERR401: Diagnostic Processor detects improper air flow. There is inadequate air flow to cool the CPU. PRIMOS attempts to perform an orderly shutdown.	1. Verify that the blower assembly is functioning. 2. Verify that the air flow sensor is functioning. 3. Check the sensor harness (CBL10616-001 or CBL10481-001) for poor connection or broken wires. 4. If the problem persists, replace the VCP-V PCB.
*ERR404: Diagnostic Processor detects overtemperature on its own board.	1. See ERR070.
*ERR405: Diagnostic Processor detects CPU board 1 overtemperature.	1. See ERR073.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
*<u>ERR411: Diagnostic Processor detects UPS/BBU A Batteries Low.</u> The VCP-V has detected a low battery on the BBU/UPS while the unit was active.	1. Check UPS/BBU system. 2. If no UPD/BBU exists, replace VCP-V.
*<u>ERR412: Diagnostic Processor detects BBU B Batteries Low.</u>	1. See ERR411.
*<u>ERR413: Diagnostic Processor detects MBBU Batteries Low.</u>	1. See ERR411.
*<u>ERR417: BBU/UPS Fault.</u>	1. See ERR411.
<u>ERR424: Diagnostic Processor detects a fault in power supply <n>.</u> The VCP-V has detected a system power supply which has stopped providing dc voltage due to an internal fault condition (loss of dc output, over-temperature, or overcurrent). The VCP-V turns the supply off immediately to prevent damage to it or any other component in the system.	1. Refer to Troubleshooting System Power Problems.
*<u>ERR430: Voltage critical for supply <n>.</u>	1. Faulty power supply. Replace supply indicated by <n>.
*<u>ERR431: High voltage critical for supply <n>.</u>	1. See ERR430.
*<u>ERR432: Low voltage critical for supply <n>.</u>	1. See ERR430.
*<u>ERR433: Error detected during power down sequence of supply <n>.</u>	1. See ERR430.
*<u>ERR434: Error detected during power up sequence of supply <n></u>.	1. See ERR430.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
*<u>ERR500: Diagnostic Processor Load device identification error</u> The wrong Floppy Drive is installed in the system.	1. Verify that correct Floppy Drive is installed. 2. Replace the Floppy Drive with a known good Floppy Drive. 3. Replace the VCP-V PCB.
<u>ERR501: Attempted to access History Disk as Load Device.</u> You tried to access the history disk without using the HISTORY command (you used DIR :2).	1. Reset default device to :0.
<u>ERR502: Invalid History Disk detected.</u> Valid diskette not detected at Logical Device 1.	1. Verify that formatted diskette is in Device 1. 2. Check disk drive.
<u>ERR503: History Disk not responding.</u> VCP-V tried to log error and failed.	1. Verify that formatted diskette is in Device 1. 2. Check that diskette is not write protected. 3. Replace diskette.
<u>ERR504: History Disk write error.</u> VCP-V tried to write to history disk and. failed.	1. Verify that formatted diskette is in Device 1. 2. Check that diskette is not write protected. 3. Replace diskette.
<u>ERR600: Bad Syntax [<last token>]</u> The last line typed contained bad syntax or incorrect arguments. The input that caused the error is displayed as the "<last token>". If an argument is missing, the <last token> is "null" and is displayed as "[]".	1. Change the command's Syntax and reenter.
<u>ERR601: Unsupported Command.</u> The command entered is correct in syntax, but the argument supplied is not supported by the particular VCP-V software.	1. Issue the command with an argument that is supported.
*<u>ERR701: Can't determine the Control Store size.</u>	1. Replace CMI board. 2. Replace VCP-V.
<u>ERR704: Control Store verification error at location.</u>	1. Replace CMI Board.

TABLE 6-42: VCP-V ERROR CODES AND CORRECTIVE ACTIONS (CONT.)

DESCRIPTION	ACTION
*ERR800: Diagnostic Processor time of day clock not valid VCP-V time-of-day clock is not working correctly. This can occur if it has not been initialized properly or the VCP-V is defective. (If the batteries are dead replace the VCP-V.)	1. Set the time-of-day clock by entering CP mode and using the "SE" command. 2. Replace the VCP-V PCB.
*ERR900: CPU Command not acknowledged. The CPU does not acknowledge a VCP command. This might happen during a parity or framing error and should always recover when the VCP attempts resynchronization.	1. After VCP-V resynchronizes, reenter the command. 2. Replace the VCP-V PCB.
*ERR901: Unexpected character received from CPU <n> The CPU is sending data that the VCP-V is not expecting. This occurs when both the VCP-V and the PDA have control of CPU.	1. Enter CP mode and type "MO PDA". Enter "<OFF LINE>". 2. Remove the PDA. 3. Replace the CPU CMI-Board. 4. Run Microdiagnostics 1.
*ERR902: DMD transfer not acknowledged.	
ERR903: Invalid input (token too big) The command entered has more characters than the VCP-V can handle.	1. Check the command's syntax and reenter.
*ERR904: CPU did not acknowledge DMD NAK.	
*ERR905: CPU not responding during DMD NAK.	
*ERR906: CPU did not acknowledge DMD ACK.	
*ERR907: CPU not responding during DMD ACK.	
*ERR910: Parity Error detected during communication with CPU.	

TABLE 6-43: VCP-V WARNING CODES AND CORRECTIVE ACTIONS

MESSAGE/DEFINITION	ACTION
WRN000: Verification	1. Replace floppy disk continue trying next (microcode) consecutive device. 2. Replace floppy drive. 3. Replace VCP-V.
*WRN001: <nn> Recoverable disk read error(s) occurred.	1. Replace floppy disk. 2. Replace floppy drive. 3. Replace VCP-V.
*WRN002: <nn> Recoverable verification error(s) occurred. Printed when a recoverable error is detected while loading the CPU microcode. If this error persists, the system integrity still remains, but the problem should be corrected.	1. Replace the Floppy Diskette. 2. Replace floppy drive. 3. Replace VCP-V.
*WRN003: UPS system active. Main Power interrupted. Printed whenever the main ac power goes down on a system connected to a UPS. The system operates on UPS until batteries fail or power returns.	1. Check UPS system. 2. If no UPS exists, replace VCP-V.
WRN004: Mode specifier is not set to Octal. Indicates that the current sense switch setting is in decimal, binary or hexadecimal. The operation specified continues using the current setting.	1. If mode octal is desired, enter CONTROL-P or ESC twice to exit the current command. Use the ':O' command to specify mode.
*WRN005: Sysverify file not found. AUTOBOOT sequence terminated, entering Control Panel mode. Indicates a copy of the SYSVERIFY microcode is not found during the microcode load sequence.	1. Check that a valid Floppy diskette is installed. 2. Enter the "DIR" command at the Control Panel level and verify that a file of Type S exists on the card. 3. If S file does not exist, get a correct microcode floppy. 4. If the file does exist, replace the floppy and enter the BOOTP command.

TABLE 6-43: VCP-V WARNING CODES AND CORRECTIVE ACTIONS (CONT.)

MESSAGE/DEFINITION	ACTION
WRN008: BBU/UPS no longer has a fault. The Uninterruptible Power Supply (UPS) or the Battery Back Up (BBU) unit has experienced a fault condition that has been resolved.	Not supported at this time.
WRN042: Checksum error while reading code.	1. Retry the operation that caused the warning to ensure that the data loaded is correct.
*WRN043: Checksum error on file "<filename>" The diagnostic processor detects a checksum error while reading the named file from the Floppy Drive. This warning can occur any time the VCP-V accesses the Floppy drive, and usually indicates some form of read error undetected by any other check mechanism.	1. Retry the operation that caused the warning and ensure that the loaded data is correct. If the problem occurs again, replace the Floppy diskette.
*WRN100: Autoboot Sequence terminated, entering Control Panel Mode. The DP detected a control store verification error during autoboot.	1. Replace floppy diskette. 2. Replace CMI-Board. 3. Replace VCP-V.
*WRN200: A run command was issued with frequency set high. The user has issued a run command with the CPU crystal set high.	1. Use the FREQNORM command to return to normal frequency. This is a Prime proprietary command.
WRN400: Diagnostic Processor shutting down system power. Prints just before the VCP-V shuts down system power in response to one of the environmental sensors.	1. Check cabinet and room temperatures. 2. Check environmental sensors.

TABLE 6-43: VCP-V WARNING CODES AND CORRECTIVE ACTIONS (CONT.)

MESSAGE/DEFINITION	ACTION
WRN401: Diagnostic Processor detects soft shutdown request. The diagnostic processor has detected a request for a soft shutdown of the system, such as that caused by the operator pressing the ON/ INITIATE SHUTDOWN button. The diagnostic processor shuts the entire system down, including PRIMOS, in an orderly fashion and turns off system power.	This message is normal.
*WRN500: Voltage out of range for supply <n>. The normal operating voltage is out of range for indicated supply.	1. Adjust the +5V. 2. Replace the power supply.
*WRN501: High voltage out of range for Supply <n>. Margin HI is out of range for the indicated supply.	1. Adjust the +5V. 2. Replace the power supply.
*WRN502: Low voltage out of range for Supply <n>. Margin LO is out of range for the indicated supply.	1. Adjust the +5V. 2. Replace the power supply.
WRN503: External PDU not responding. If no external PDUs are daisy-chained to the mainbay, this message appears at each power up. Otherwise, one of the external PDUs is not sequencing correctly.	1. If external PDUs are not daisy-chained, ignore the message. 2. See System Power Failures flowchart.
WRN504: Retry occurred during the sequencing of the PDU.	1. If condition persists, replace the PDU.
*WRN600: CPU detects wired memory page failure. The CPUs SYSCLR microcode has detected a wired memory page failure. The DP enters CP mode after logging.	

TABLE 6-43: VCP-V WARNING CODES AND CORRECTIVE ACTIONS (CONT.)

MESSAGE/DEFINITION	ACTION
WRN401: Diagnostic Processor detects soft shutdown request. The diagnostic processor has detected a request for a soft shutdown of the system, such as that caused by the operator pressing the ON/ INITIATE SHUTDOWN button. The diagnostic processor shuts the entire system down, including PRIMOS, in an orderly fashion and turns off system power.	This message is normal.
*WRN500: Voltage out of range for supply <n>. The normal operating voltage is out of range for indicated supply.	1. Adjust the +5V. 2. Replace the power supply.
*WRN501: High voltage out of range for Supply <n>. Margin HI is out of range for the indicated supply.	1. Adjust the +5V. 2. Replace the power supply.
*WRN502: Low voltage out of range for Supply <n>. Margin LO is out of range for the indicated supply.	1. Adjust the +5V. 2. Replace the power supply.
WRN503: External PDU not responding. If no external PDUs are daisy-chained to the mainbay, this message appears at each power up. Otherwise, one of the external PDUs is not sequencing correctly.	1. If external PDUs are not daisy-chained, ignore the message. 2. See System Power Failures flowchart.
WRN504: Retry occurred during the sequencing of the PDU.	1. If condition persists, replace the PDU.
*WRN600: CPU detects wired memory page failure. The CPUs SYSCLR microcode has detected a wired memory page failure. The DP enters CP mode after logging.	

6.4.2 DIAGNOSTIC LEDS ON TLA10113 POWER SUPPLIES

There are three LEDs on the front panel of each TLA10113 power supply (see Figure 6-25).

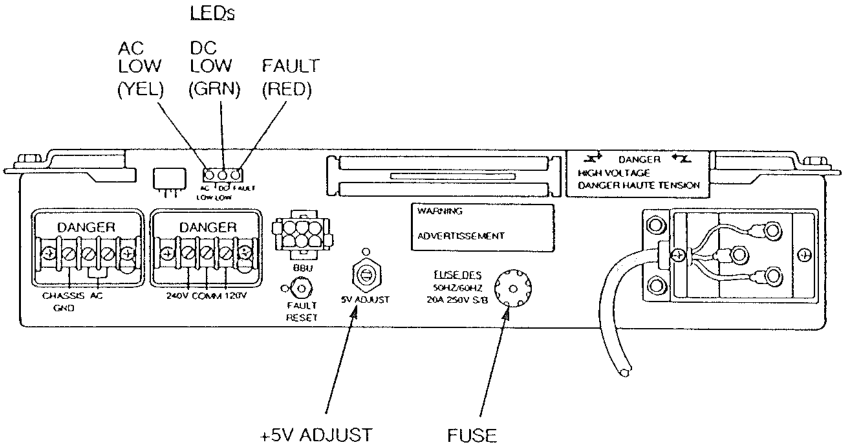


FIGURE 6-25: TLA10113 POWER SUPPLY LEDS

The LEDs are used to diagnose power supply voltage failures. The LEDs and their respective failure signals and meanings are shown in Table 6-44.

- Solidly lighted LEDs indicate nominal power supplies (refer to Table 6-44).
- Blinking LEDs indicate an overcurrent condition.
- If a LED is OFF, it indicates that the voltage it is monitoring has dropped below a nominally good limit.

TABLE 6-44: SYSTEM POWER SUPPLY LEDs

LED	VOLTAGE/SIGNAL MONITORED	VOLTAGE LIMIT
1	+5 Vdc	+4.70 Vdc
2	+12 Vdc	+11.4 Vdc
3	-12 Vdc	-11.4 Vdc

Follow the corrective steps below if any of the LEDs report on abnormal voltage conditions:

1. If any of the LEDs are OFF, refer to Measuring Backplane Voltages in this chapter and follow the corrective procedure.

2. If any overcurrent conditions are indicated, press the ON/INITIATE SHUTDOWN button immediately and determine the cause of the condition.

Refer to Tables 6-45 and 6-46 for LED pattern definitions.

TABLE 6-45: ICS3 COLDSTART LED ERRORS

LED4 RED	LED3 RED	LED2 RED	LED1 RED	DESCRIPTION	ACTION
OFF	OFF	OFF	OFF	All memory test pass	None
BLINK	OFF	OFF	OFF	Normal operation	None
OFF	OFF	OFF	ON	Data checkerboard memory test fails	Replace controller
OFF	OFF	ON	OFF	Refresh memory test fails	Replace controller
OFF	OFF	ON	ON	Checkbit checker-board memory test fails	Replace controller
OFF	ON	OFF	OFF	Byte write memory test fails	Replace controller
OFF	ON	OFF	ON	Address line memory test fails	Replace controller
OFF	ON	ON	OFF	Bit shift memory test fails	Replace controller
OFF	ON	ON	ON	Address offset memory test fails	Replace controller
ON	OFF	OFF	OFF	EDAC detect/correct memory test fails	Replace controller
ON	OFF	OFF	ON	EDAC interrupt logic test fails	Replace controller
ON	OFF	ON	OFF	EDAC multiple bit error test fails	Replace controller

TABLE 6-46: ICS3 STATUS LED ERRORS

LED	CONDITION		DESCRIPTION	ACTION
1	BLINK	Warning	LAC card cage power failure	Replace LAC card power supply
2	BLINK	Warning	Single-bit memory parity error detected	Replace controller
3	ON	Fatal	WCS parity error detected	Replace controller
4	BLINK	Normal	ICS3 controller self-verification completed	None

6.4.6 DIAGNOSTIC LEDS ON THE PNC-II

The PNC-II controller has six LEDs: two to indicate overall controller status; four to report on network status (see Figure 6-27). When there is a network failure, the four network status indicators on the right become error code indicators.

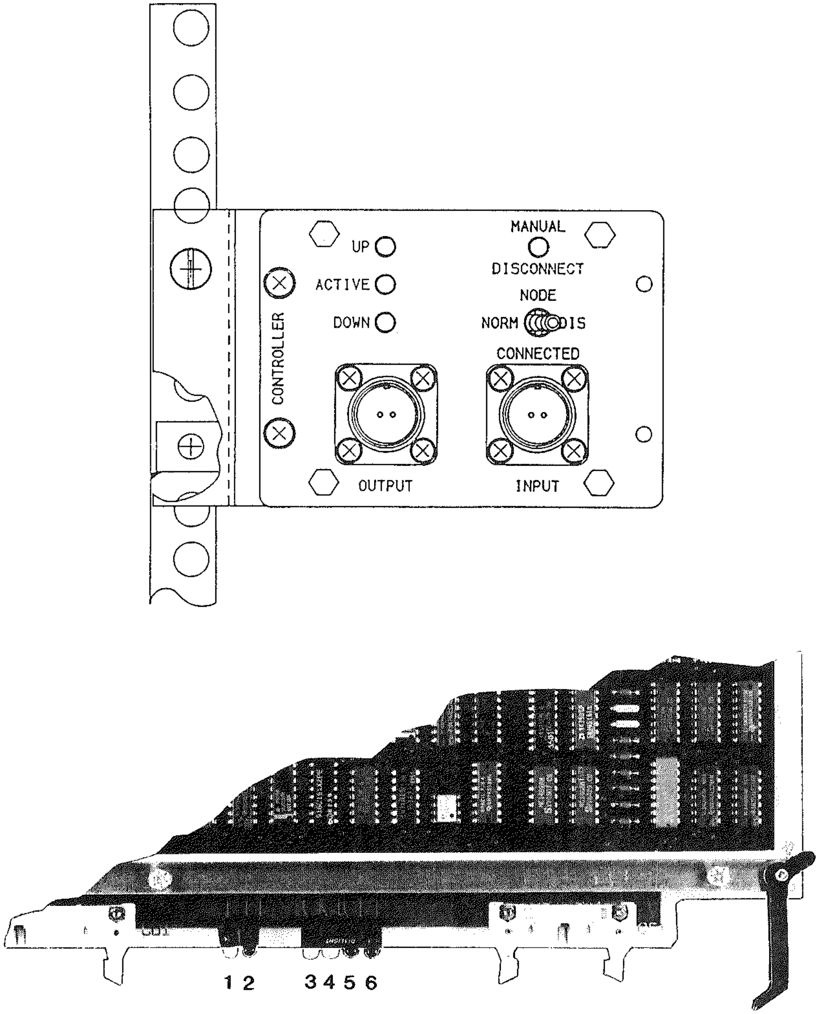
The four LEDs serve a double purpose:

- TABLE 6-47 summarizes the significance of these four LEDs when the Board Active LED (green) is ON.
- TABLE 6-48 summarizes the interpretation of these four LEDs when the Board Fail LED (red) is ON.

TABLE 6-47: PNC-II PCB NETWORK STATUS LEDS

LED				MEANING
Ring Up	Node Active	Ring Down	J-Box Fault	
ON OFF				Network up with Token circulating Network Down
	BLINK			Activity displayed as packets are transmitted and received
		ON BLINK OFF		No Tokens or data being received Receiving intermittent errors Ring running with no errors
			ON	MJ-Box not plugged in, or MJ-Box cable plugged in backwards, or MJ-Box switch disconnected

If an error is detected during self-verification or run-time the four rightmost LEDs cease to be used for network status and instead display an error code by light pattern. Refer to Table 6-48.



CONTROLLER STATUS		NETWORK STATUS			
1	2	3	4	5	6
GREEN	RED	YELLOW	YELLOW	RED	RED
GOOD	ERROR	RING UP	NODE ACTIVE	RING DOWN	J-BOX FAULT

FIGURE 6-27: PNC-II CONTROLLER AND MJ-BOX LEDS

TABLE 6-48: PNC-II LED ERROR CODES

D4	D3	D2	D1	MEANING	DURING
0	0	0	1	ROM Verify Failed	Self-verify
0	0	1	0	RAM Verify Failed	Self-verify
0	0	1	1	EDAC Verify Failed	Self-verify
0	1	0	0	CTC Verify Failed	Self-verify
0	1	0	1	DMA Verify Failed	Self-verify
0	1	1	0	FIFO Verify Failed	Self-verify
0	1	1	1	Loopback Verify Failed	Self-verify
1	0	0	0	Network RAM Error	Self-verify
1	0	0	1	SCC Verify Error	Self-verify
1	0	1	0	Multiple Bit EDAC Error	Run-time
1	0	1	1	NMI (Backplane Parity) Error	Run-time
1	1	0	0	Bad 186 Interrupt Taken	Run-time
1	1	0	1	PNC-II DMA Error	Run-time
1	1	1	0	Fatal Error	Run-time
1	1	1	1	NMI (Watch Dog Timer) Failure	Run-time

NOTE: LED on = 1   LED off = 0

The PNC-II Junction Box (MJ-Box) has four LEDs. The three LEDs to the left display the network status. The fourth LED, when lit, indicates that the junction box is connected (see Figure 6-27). Refer to Table 6-49 to interpret the MJ-Box LED messages.

TABLE 6-49: MJ-BOX LED STATES

LED DISPLAY			MEANING OF COMBINATION
GRN Ring Up	GRN Ring Act	RED Ring Down	
OFF	OFF	OFF	System not powered up, or MJ-Box not connected, or MJ-Box plugged in backwards, or MJ-Box switched OFF
OFF	OFF	ON	Twinax cables inverted
OFF	OFF	ON	Ring Net "Broken" above this node
OFF	BLK	ON	Ring Net "Broken", receiving tokens from other nodes, break not directly above this node

BLK = blinking

* LEDs on the controller DO NOT match those on the MJ-Box when there is a failure condition (PCB Board Fault LED is ON).

TABLE 6-49: MJ-BOX LED STATES (CONT.)

LED DISPLAY			MEANING OF COMBINATION
BLK	OFF	BLK	Ring Net intermittent (uneven opposing blink)
ON	BLK	OFF	Normal, Ring functioning properly
ON	BLK	BLK	Ring functioning properly but intermittent cable detected

BLK = blinking

* LEDs on the controller DO NOT match those on the MJ-Box when there is a failure condition (PCB Board Fault LED is ON).

NOTE

If the MJ-Box is disconnected, the three network status LEDs have NO meaning.

6.5 TROUBLESHOOTING WITH DIAGNOSTICS

This section includes the following procedures:

- Running Microdiagnostics
- Running the Diagnostic Testing System (DTS)
- Using Remote Diagnostics

6.5.1 TROUBLESHOOTING WITH MICRODIAGNOSTICS

The CPU microdiagnostics allow the CSR to diagnose a CPU problem to the optimal Field Replaceable Unit (FRU) at a customer site. The microdiagnostics are controlled by the VCP-V Diagnostic Processor. They are stored on floppy disks. Part numbers are listed in Chapter 7 of this manual.

When a failure occurs, the VCP-V reports up to four FRUs as being the most likely failing FRUs. The failing FRUs and the failing test numbers are displayed on the terminal.

The extent of messages displayed during execution of the microdiagnostics varies depending on the VCP-V message mode status (FULL or BRIEF) and the situation the diagnostics are being executed under (AUTOBOOT or via commands).

To run the system microdiagnostics:

1. Place the VCP-V in CP mode. Enter the following command to place the VCP-V in BRIEF message mode:

   CP1>MO BRIEF

2. Remove the functional microcode diskette from Logical Device 0, then insert the microdiagnostics diskette into the drive.

3. Enter the following command to display the contents of the microdiagnostic diskette on the system terminal:

   CP1>DIR :0

4. To load and execute a microdiagnostic overlay, enter the following command, where <filename> can be any of the UDIAG tests:

   CP1>RUND <filename>

5. After each microdiagnostic overlay has completed execution and the VCP-V has returned to CP mode, place the VCP-V into FULL message mode. This is done by entering the following command:

   CP1> MO FULL

6. Load and execute each microdiagnostic overlay using the RUND.

7. If any failures are detected, the VCP-V displays the following message on the system terminal and enters CP mode:

```
ERR100: Failure detected in microdiagnsotic "<filename>",
        test <nnnn>
[       Most probable replaceable unit is <ORU1>        ]
[       Most probable replaceable unit is <ORU2>        ]
[       Most probable replaceable unit is <ORU3>        ]
[       Most probable replaceable unit is <ORU4>        ]
```

   Suspect the Optimal Replaceable Units (ORUs) in order displayed in the error message.

8. If no errors are detected, the VCP-V displays the following message on the system terminal after each test:

```
DPM003: Diagnostic "Filename" successfully completed
```

If the VCP-V is configured in full message mode, the following message is displayed after the completion of each test:

```
DPM010: Test # <nnnn> successfully completed.
```

6.5.2 RUNNING THE DIAGNOSTIC TESTING SYSTEM

The following sections provide a brief guide to using the Diagnostic Testing System to troubleshoot Model 4050/4150 system failures. For operating procedures, refer to Applicable Diagnostics in the troubleshooting guide for each subsystem. For a more detailed description of each test, refer to the Diagnostic Testing System Software Service Guide (SSG400).

6.5.2.1 Applicable DTS Diagnostics

Table 6-50 lists DTS diagnostics which support the Model 4050/4150 system. They can be used to test the portions of the system shown.

TABLE 6-50: SYSTEM DIAGNOSTICS

DEVICE	DIAGNOSTIC	UNITS TESTED
CPU	All DTS CPU	Functional blocks of the CPU and the ability of the CPU to execute instructions. Unsupported tests abort.
DISK	IO.DISK	Disk and common logic of disk drives.
TAPE	IO.TAPE.MSTC	MSTC tape controller and quad-density tape drive
	IO.TAPE	Streaming tape subsystem.
QAMLC	IO.AMLC IO.ASYNC	Asynchronous controller capability of system.
ICS1	IO.ASYNC	Async capability of the ICS1.
ICS3	IO.ICS3	All components of ICS3 subsystem.
PNC	IO.PNC	PNC and PNC-II controllers either alone or in a network configuration.

6.5.2.2 DTS Diagnostic Monitors

DTS supports two diagnostic monitors that serve as single-user operating systems to control the execution of the various DTS diagnostics. Table 6-51 describes the DTS monitors.

TABLE 6-51: DTS MONITORS

MONITOR	DESCRIPTION
Standalone Architectural Monitor (SAM)	Cannot be run under Multi-user PRIMOS
PRIMOS Architectural Monitor (PAM)	Runs under PRIMOS. Cannot be run standalone. Includes AUTOPAM, which executes copies of PAM as phantoms.

Commands are provided to load and execute individual diagnostics and groups of diagnostics. Commands provide diagnostic status and system configuration data. More information on SAM, PAM, and their commands can be found in the Diagnostic Testing System Software Service Guide (SSG400).

6.5.2.3 Loading and Running DTS From Disk

PRIMOS Rev. 20 and greater has introduced some changes into the method of starting DTS in standalone mode. The HBOOT routine is no longer needed, since CPBOOT accomplishes the same testing when the boot is initiated. SAM is now a standalone program and can be booted directly from either disk or tape.

To boot a DTS from disk in standalone mode, refer to the example below (operator input is underlined):

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        11 Jan 88 09:30:00 Monday
```

2. Boot (see note below):

```
CP1> BOOT 11114
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]
```

3. Enter the run file treename and physical device:

```
RUN FILE TREENAME=DIAG>SAM.SAVE

BOOTING FROM 001060    DIAG>SAM.SAVE

SAM Rev 13.1 Copyright (c) Prime Computer, Inc. 1985
Enter physical device = 1060
ENTER 'LOAD;RUN' FOR DEFAULT EXECUTION
SAM>
```

NOTE

Sense switch 4 has been set to inhibit machine check mode during the initial boot and diagnostic testing that is performed by CPBOOT.

6.5.2.4 Loading and Running DTS From Tape

Since SAM.SAVE is now a standalone program it can also be booted directly from tape. To load a DTS from tape, refer to the example below:

1. Clear the system:

```
CP1> SYSCLR
REALLY? YES
DPM006: Central Processor system initialization completed.
        11 Jan 88 09:30:00 Monday
```

2. Boot:

```
CP1> BOOT 11005
DPM007: System booting, please wait.
[CPBOOT Rev. 10.0 Copyright (c) Prime Computer, Inc. 1987]
```

3. Enter run file treename and physical device:

```
RUN FILE TREENAME= DIAG>SAM.SAVE

BOOTING FROM MT0      DIAG>SAM.SAVE

SAM Rev 9.1 Copyright (c) Prime Computer, Inc. 1985
Enter physical device = 1060
ENTER 'LOAD;RUN' FOR DEFAULT EXECUTION

SAM>
```

6.5.3 USING REMOTE DIAGNOSTICS

The Model 4050/4150 system can be remotely accessed from any field office that has a terminal and a 1200 baud originate mode modem. All domestic (U.S.) systems ship with an internal 1200 baud answer mode modem. Systems sold outside the U.S. do not contain the internal modem but do have provisions to connect an external 300 or 1200 baud modem via the system bulkhead.

To gain access to the customer system from the remote terminal follow this procedure:

NOTE

For clarity the customer's system and modem is referred to as the remote system and the remote modem and the field office's terminal is referred to as the calling terminal.

1. Inform the customer that you intend to run diagnostics on the remote system via its internal (or external) modem.

2. Obtain the telephone number of the remote modem. Instruct the customer to press the REMOTE ENABLE button on the status panel to allow access by the calling terminal.

3. After connection has been made with the remote system, the customer must press the REMOTE PRIVILEGE button to allow the calling terminal to become the master system console.

After connection is made to the remote system and the calling terminal has system console privileges, take the following actions to gain failure information about the remote system:

- Examine the event log file
- Examine the VCP-V status display using the CP mode STATus command
- Examine software configuration files (i.e., CONFIG and PRIMOS.COMI)
- Initiate and monitor a boot sequence
- Monitor CPBOOT execution with informative message mode enabled
- Load and run DTS diagnostics
- Load and run T&Ms d run T&Ms

CHAPTER 7
REMOVAL & REPLACEMENT PROCEDURES

This chapter provides removal and replacement procedures for the following Model 4050/4150 Field Replaceable Units:

- Cabinet Doors and Covers
- System Control Panel
- Board Interface Cables
- System Boards
- Board PROMS and RAMS
- Power Supply Fuse
- Power Supplies
- Battery Backup Unit
- Power Shunt Board
- Blower Assembly
- Air Filter
- Backplane
- AC Power Cable
- Mainbay Power Distribution Unit (PDU)
- Peripheral Cabinet Power Distribution Unit (PDU)
- Floppy Disk Drives
- PRIMENET Node Controller and Modular Junction Box
- Intelligent Communications Subsystem 3 (ICS3)
- Model 4587 Tape Drive (Quad-Density)
- Model 4735 Disk Drive (496 MB)
- Model 4835 Disk Drive (770 MB)

Major system components and assemblies are shown in Figure 7-1.

Part numbers for system components, cables, and fuses are listed under System Part Numbers at the end of this chapter.

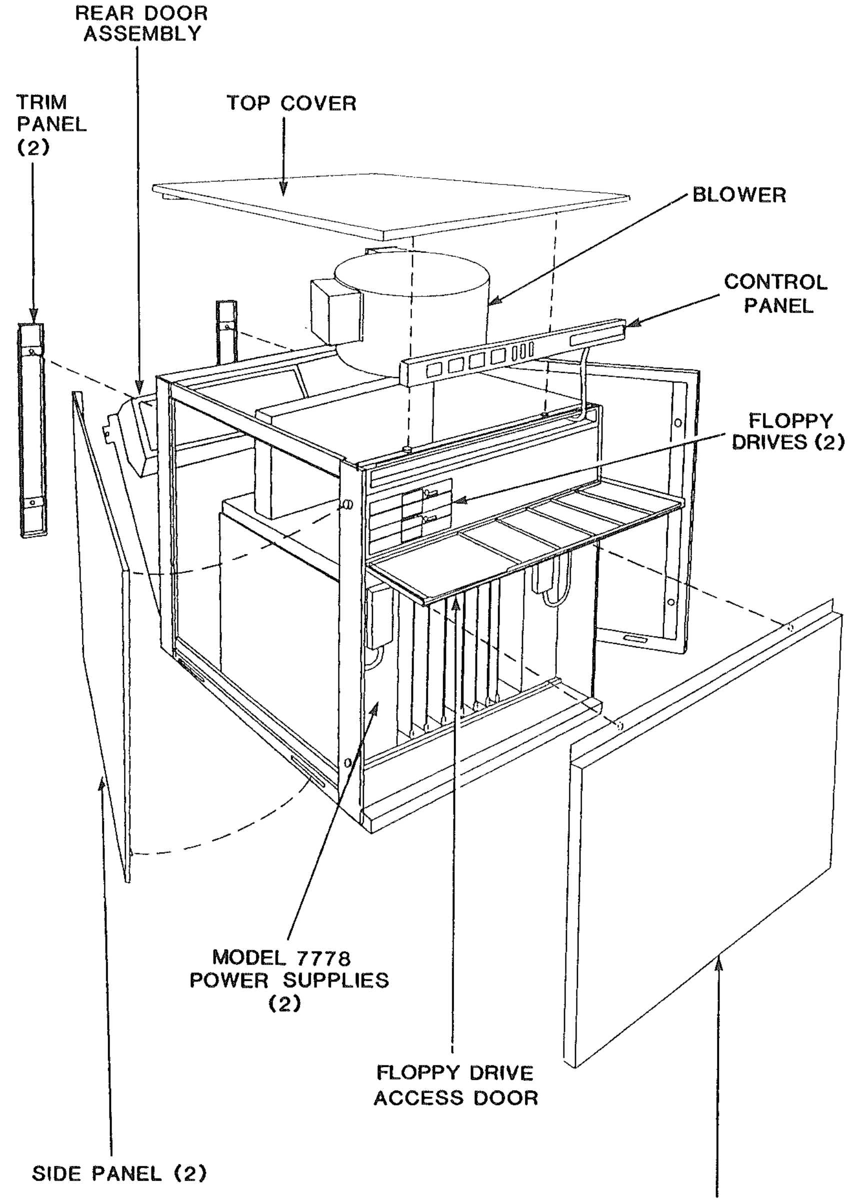


FIGURE 7-1: MODEL 4050/4150 EXPLODED VIEW

7.1 SYSTEM POWER-DOWN

WARNING

Power down the mainbay and peripheral cabinets before removing any Field Replaceable Units (FRUs).

To power down the system, follow these steps:

1. Notify all users that the system is being shut down. Set MAXUSR to 0 to prevent additional users from logging in.

2. Press the write protect button on all disk drives and power down all peripheral devices.

3. Use the STATUS USERS command to verify that all terminal users are logged out and all subsystems are shut down.

4. Shut down PRIMOS with the SHUTDN ALL command.

5. Press the ON/INITIATE SHUTDOWN switch on the control panel to begin the soft shut-down sequence.

6. From the rear of the peripheral cabinet, turn the PDU circuit breaker to the OFF (down) position.

7. From the rear of the mainbay, turn the PDU circuit breaker to the OFF (left) position.

8. Remove the mainbay and peripheral cabinet ac power cables from their external power sources.

WARNING

Pressing the ON/INITIATE SHUTDOWN button does not remove power to the system or Battery Backup Unit. To remove power completely, turn the mainbay and peripheral cabinet PDU circuit breakers to the OFF position and remove the mainbay and peripheral cabinet ac power cables from their wall outlets.

7.2 REMOVING AND REPLACING SYSTEM CABINET COVERS

To access system FRUs, open or remove the following Model 4050/4150 cabinet covers:

- Front Panel
- Floppy Disk Drive Access Door Assembly
- Top Cover
- Side Covers
- Rear Door Assembly

NOTE

Most system covers are secured to the cabinet chassis by a series of quarter-turn Phillips head captive fasteners. To unlock a fastener, push and turn it counterclockwise. To lock a fastener, push and turn it clockwise.

The subsections that follow provide removal and replacement procedures for these covers.

7.2.1 REMOVING AND REPLACING THE FRONT PANEL

The following subsections provide procedures for removing and replacing the front panel (see Figure 7-1). Remove the front panel to access the boards and power supplies in the system card cage.

CAUTION

Operating the system with the front panel removed impairs the cooling capability of the variable-speed blower. To avoid overheating boards and power supplies in the card cage, do not run the system for more than three minutes with the front panel removed.

7.2.1.1 Removing the Front Panel

To remove the front panel, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).
2. Open the floppy disk drive access door assembly.
3. Supporting the front panel with one hand, unlock the two captive fasteners that secure the top of the panel to the system chassis (see Figure 7-2).
4. Tilt the top of the panel toward you and lift it away from the chassis to expose the card cage.

7.2.1.2 Replacing the Front Panel

To replace the front panel, follow these steps:

1. Open the floppy disk drive access door assembly.

NOTE

Be sure to open the floppy disk drive access door assembly before continuing with this procedure to avoid damage to the door.

2. Insert the two pins on the bottom edge of the front panel into the corresponding holes in the system chassis (see Figure 7-2).
3. Push the top of the panel toward the system cabinet until the panel rests against the chassis.

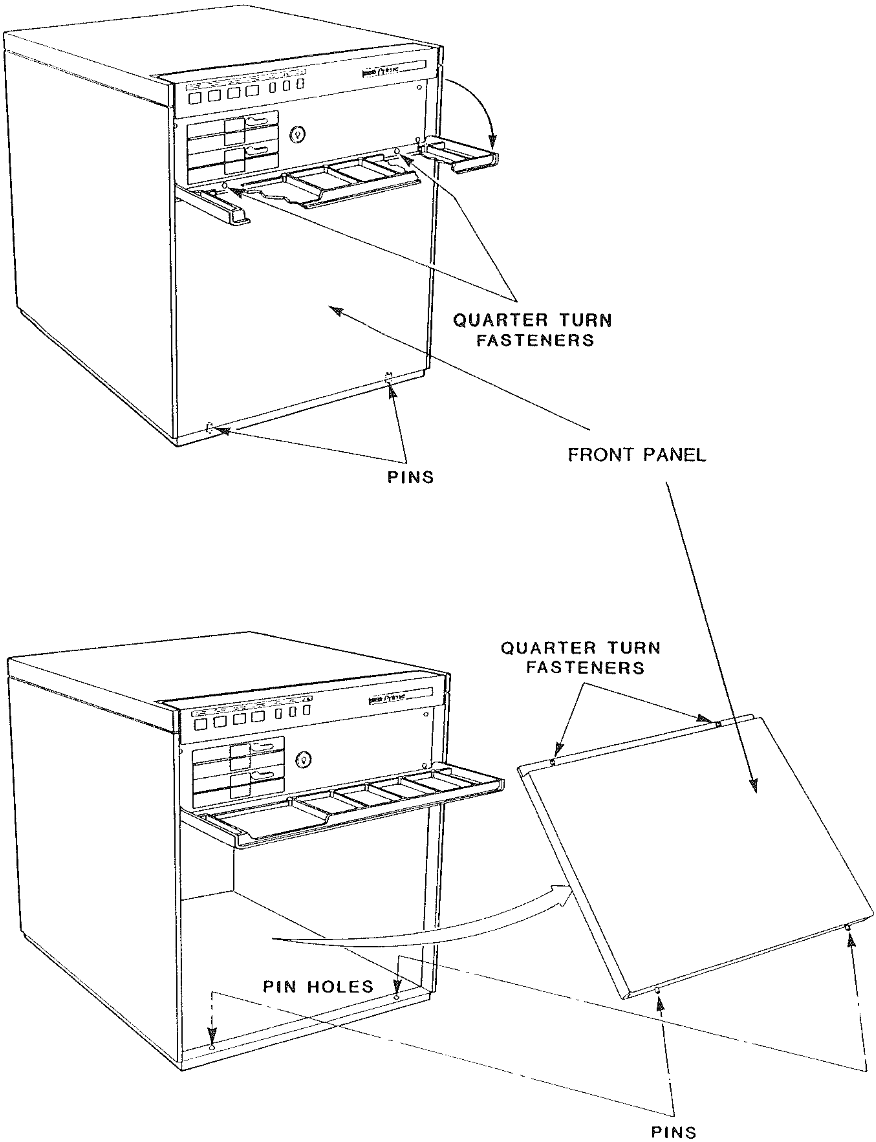


FIGURE 7-2: FRONT PANEL REMOVAL

4. Align the two captive fasteners on the panel with their corresponding captive hardware on the cabinet directly below the floppy drive access door.

5. Lock the fasteners to secure the front panel to the chassis.

7.2.2 REMOVING AND REPLACING THE FLOPPY DISK DRIVE ACCESS DOOR ASSEMBLY

The floppy disk drive access door assembly, located below the system control panel (see Figure 7-1), conceals twin floppy drives and the enable/disable key lock. Remove the access door assembly to install board interface cables into the cable dress plate.

NOTE

> Remove the front panel before removing the floppy disk drive access door assembly.

7.2.2.1 Removing the Floppy Disk Drive Access Door Assembly

To remove the floppy disk drive access door, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Open the access door by pushing and releasing the top center of the door to disengage a spring-loaded push latch (see Figure 7-3).

3. Remove the front panel.

4. Unlock the four quarter-turn captive fasteners that secure the access door assembly to the chassis (see Figure 7-2) and remove the door.

7.2.2.2 Replacing the Floppy Disk Drive Access Door Assembly

To replace the floppy disk drive access door assembly, follow these steps:

1. With the door in the open position, align the four fasteners with the captive hardware on the system chassis.

2. Lock the fasteners to secure the door to the chassis.

7.2.3 REMOVING AND REPLACING THE TOP COVER

The following subsections provide procedures for removing and replacing the top cover (see Figure 7-1).

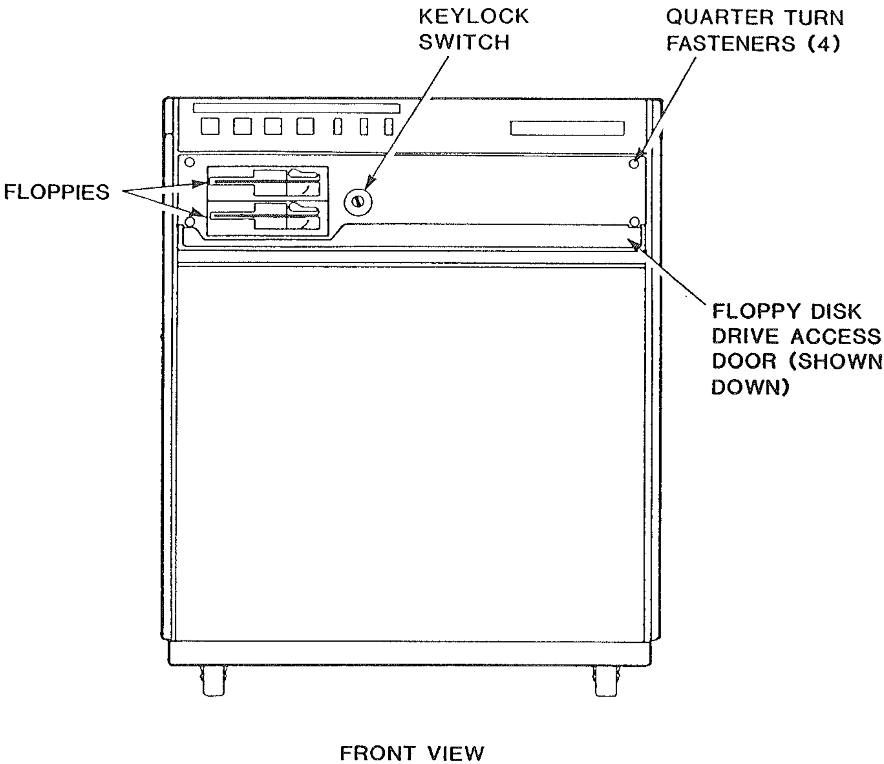


FIGURE 7-3: FLOPPY DRIVE ACCESS DOOR REMOVAL

7.2.3.1 Top Cover Removal

To remove the top cover, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).
2. Remove the two trim panels from the rear of the cabinet by carefully pulling them away from their ball stud fasteners (see Figure 7-4).
3. From the rear of the system, unscrew the two captive Phillips screws that secure the top cover to the chassis (see Figure 7-4).
4. Slide the top cover toward the rear of the system until it clears the two cover retaining screws mounted on the top front cross brace of the chassis (see Figure 7-4).
5. Lift the top cover off of the cabinet.

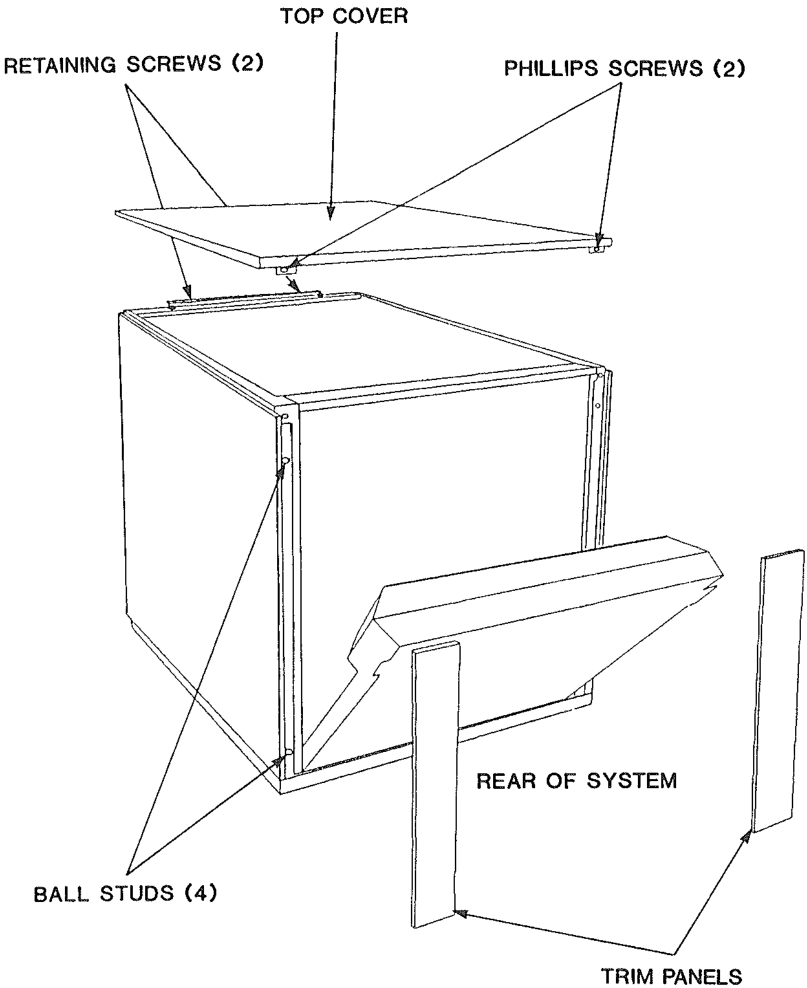


FIGURE 7-4: TOP COVER REMOVAL

7.2.3.2 Replacing the Top Cover

To replace the top cover, follow these steps.

1. Place the top cover on the cabinet with the cutout section facing the control panel.

2. Slide the top cover toward the front of the system until the cover engages the two retaining screws (see Figure 7-4).

3. Fasten the two captive Phillips screws to secure the top cover to the chassis.

7.2.4 REMOVING AND REPLACING THE SIDE COVER

The subsections that follow provide procedures for removing and replacing the side covers (see Figure 7-1). Procedures for the left and right side panels are identical.

7.2.4.1 Removing the Side Cover

To remove a side cover, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the two trim panels from the rear of the cabinet by pulling them away from their ball stud fasteners (see Figure 7-5).

3. From the rear of the system, unlock the two captive fasteners that secure the side cover to the chassis (See Figure 7-5).

4. Slide the side cover toward the rear of the system until it clears the two cover retaining screws mounted on the front side support brace of the chassis (see Figure 7-5).

5. Tilt the top of the side cover toward you, then lift the cover away from the cabinet until the two tabs at the bottom of the cover clear the tab retainers on the lower side support brace of the system cabinet (see Figure 7-5).

7.2.4.2 Replacing the Side Cover

To replace a side cover, refer to Figure 7-5 and follow these steps.

1. Insert the two tabs at the bottom of the cover into the tab retainers on the lower side support brace of the system cabinet.

2. Push the top of the cover toward the system cabinet until the cover rests against the chassis.

3. Slide the side cover toward the front of the system until the cover engages the two retaining screws, and the two captive fasteners align with the captive hardware at the rear of the chassis (see Figure 7-5).

4. Lock the two fasteners to secure the side cover to the chassis.

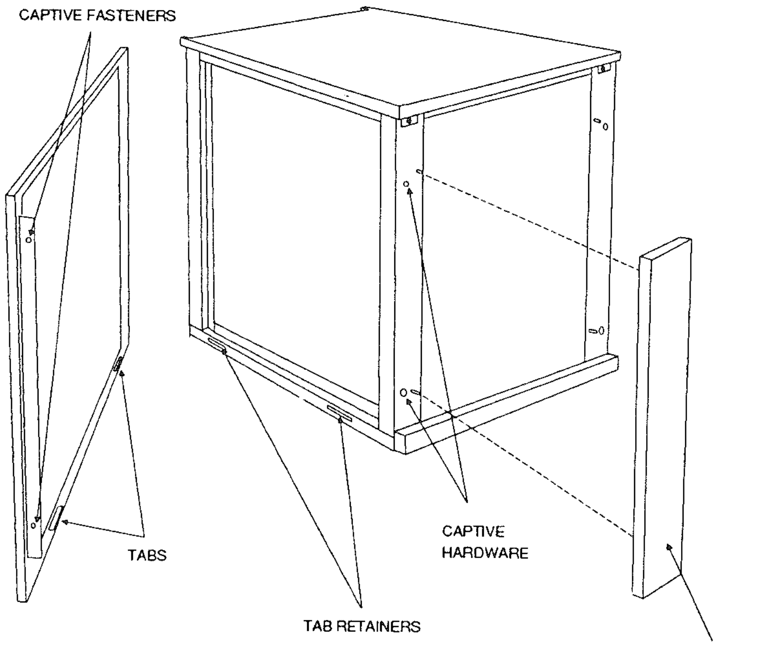


FIGURE 7-5: SIDE COVER REMOVAL

7.2.5 OPENING THE REAR DOOR ASSEMBLY

The hinge-mounted rear door assembly houses the system bulkhead, power distribution unit (PDU), and blower exhaust duct (see Figure 7-1). Tilt open the rear door to access internal PDU connectors, internal bulkhead connectors, the air temperature sensor, and the system backplane.

To open the rear door assembly, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the two trim panels from the rear of the cabinet by pulling them away from their ball stud fasteners.

3. Unlock the two captive fasteners that secure the door to the top of the chassis (see Figure 7-6).

4. Grasp the top edge of the door and tilt the door toward you. Two guide cables support the door at a 45-degree angle (see Figure 7-6).

5. To tilt the door open 90 degrees, disconnect the two guide cables by following these steps:

   A) Label and remove all external bulkhead cables, PDU cables, and the ac power cable.

   B) Supporting the rear door with one hand, slide the door end of one guide cable to the round opening in its track (see Figure 7-6).

   C) Push the cable in slightly until the cable retaining ball clears the track, then remove the cable end from the door.

   D) Repeat steps B and C to disconnect the other guide cable.

7.3 REMOVING AND REPLACING THE CONTROL PANEL

The following subsections provide procedures for removing and replacing the system control panel (see Figure 7-1).

NOTE

> The control panel, the control switches, and the indicator LEDs are one Field Replaceable Unit.

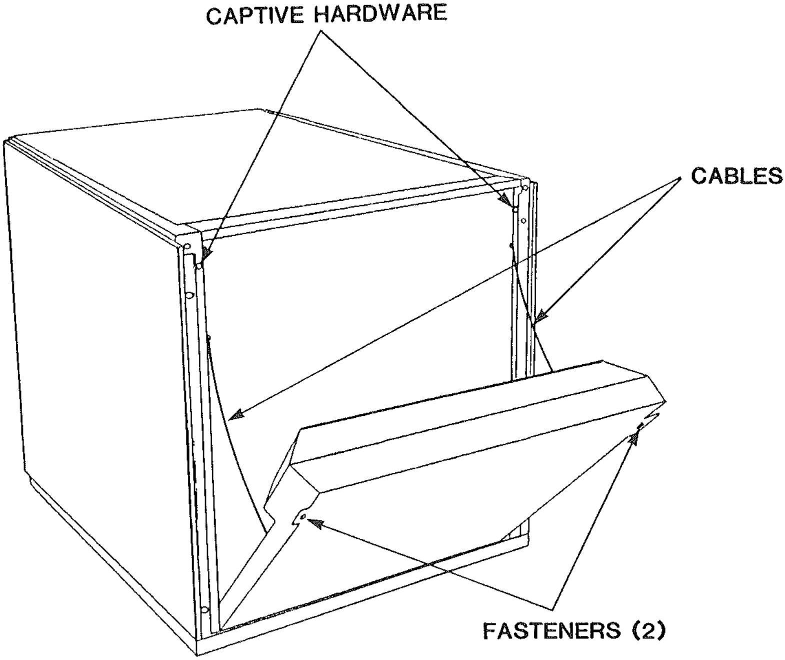


FIGURE 7-6: REAR DOOR ASSEMBLY

7.3.1 REMOVING THE CONTROL PANEL

To remove the control panel, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the top cover and floppy disk drive access door (refer to Removing and Replacing System Cabinet Covers in this chapter).

3. Remove connector P3 of CBL10486-001 from J1 of CBL10490-001 (see Figure 7-7).

4. Remove the seven screws (four on the top and three on the bottom) that secure the control panel to the chassis (see Figure 7-7).

NOTE

> Be sure to place your hand under the three bottom screws when you are removing them. They could fall into the system card cage.

5. Lift the control panel away from the chassis, then disconnect J1 of CBL10490-001 from the system chassis (see Figure 7-7).

NOTE

> In some early models, the CBL10490-001 connector is secured to the chassis by two riveted standoffs (see Figure 7-7). To disconnect J1, use a pair of pliers to snap the rivets off.

7.3.2 REPLACING THE CONTROL PANEL

To replace the control panel, follow these steps.

1. Holding the control panel in one hand, secure cable CBL10490-001 to the chassis using the standoffs, nuts, and washers supplied with the replacement control panel (see Figure 7-7).

2. Align the seven holes in the system chassis with the mounting hardware on the control panel.

NOTE

> For the next step, a magnetic screwdriver is helpful when replacing the bottom three screws. Be careful to avoid dropping the screws into the card cage.

3. Replace the seven screws that secure the control panel to the chassis.

4. Secure connector P3 of CBL10486-001 to J1 of CBL10490-001 (see Figure 7-7).

5. Replace the floppy disk drive access door and top cover (see Removing and Replacing Covers, this chapter).

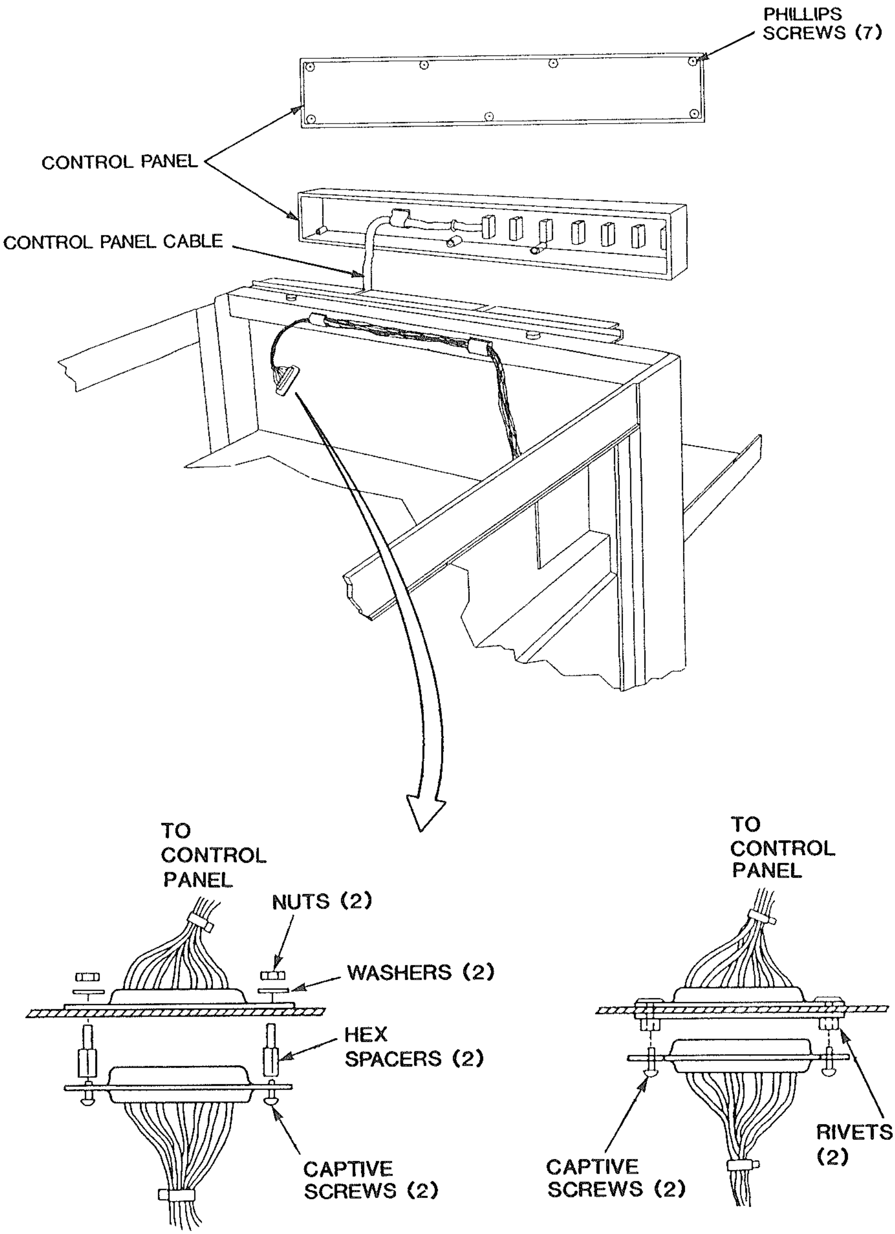


FIGURE 7-7: CONTROL PANEL REMOVAL

7.4 REMOVING AND REPLACING BOARD INTERFACE CABLES

This section provides removal and replacement procedures for standard and optional system board interface cables running from the system card cage to the inside of the rear bulkhead panel.

7.4.1 REMOVING A CABLE

To remove a board interface cable, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the front panel, the floppy disk drive access door, and the top cover, then tilt open the rear door assembly (refer to Removing and Replacing System Cabinet Covers in this chapter).

3. Locate and disconnect the cable from its board in the card cage.

4. Remove the cable from its slot in the cable dress comb and from the wireform cable trough along the top right side of the cabinet (see Figure 7-8).

5. Locate and disconnect the cable from the inside of the bulkhead panel and remove the cable from the cabinet.

7.4.2 REPLACING A CABLE

To replace an interface cable, follow these steps:

1. Lay the cable in the wireform cable trough on the top right side of the system cabinet (see Figure 7-8).

2. Connect the cable to the inside of the bulkhead panel.

3. Feed the free end of the cable through the slot in the cable dress comb closest to its corresponding board in the card cage.

4. Connect and secure the cable to its board.

5. At the rear of the system, fold any excess cable and secure it with a tie wrap (see Figure 7-8).

NOTE

> Make sure the cable is of sufficient length to tilt open the rear door assembly 90 degrees.

6. Close the rear door assembly. Replace the front panel, the floppy disk drive access door, and the top cover (refer to Removing and Replacing System Cabinet Covers in this chapter).

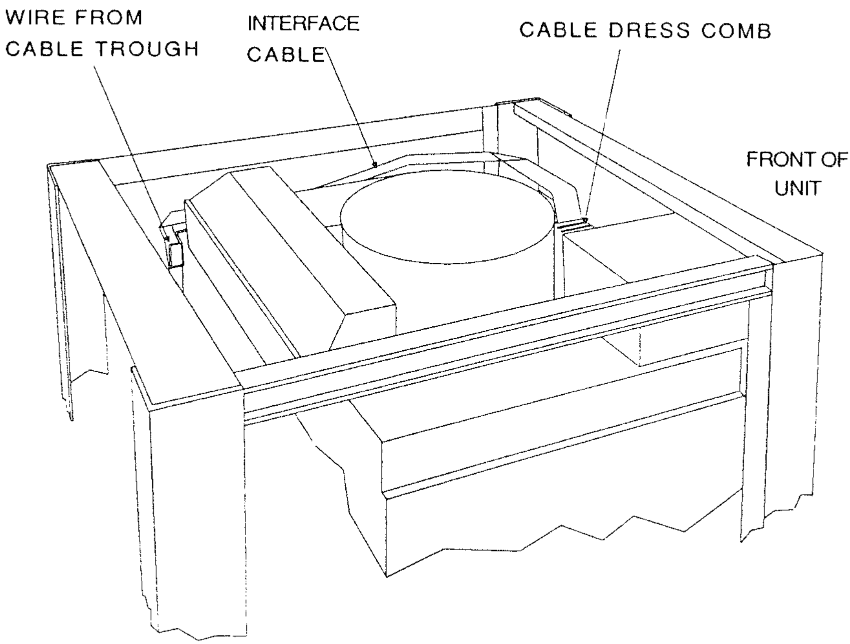


FIGURE 7-8: BOARD INTERFACE CABLE REMOVAL

7.5 REMOVING AND REPLACING SYSTEM BOARDS

This section provides removal and replacement procedures for the standard and optional system boards located in the system card cage (CPU, memory, disk and tape controllers, I/O boards).

To access the boards, remove the front panel as described in Removing the Front Panel in this chapter.

7.5.1 HANDLING SYSTEM BOARDS

The following information is provided to prevent damage to static-sensitive system boards.

Metal Oxide Semiconductor (MOS) circuits and chips are static sensitive. Be sure to use the Field Service Grounding kit (TEATIFSKIT) before handling any static sensitive components.

The kit consists of a 10-foot ground cord, a work surface, and a 12-foot wrist strap. Complete the steps that follow before handling any of the sensitive items.

1. Attach the work surface (10-foot) ground cord to a ground such as an equipment frame, electrical conduit, building frame or water pipe to ground the work surface.

2. Attach the wrist strap to a ground via the 12-foot ground cord.

3. Slip on the wrist strap.

4. After removing the board from the card cage, place it on the grounded work surface.

5. If moving the component further, place it in the static shielded pocket of the work surface. If shipping the board, place it in a static shielding bag.

Use these general guidelines when handling static sensitive components:

- Eliminate any static charge from your body before handling boards by momentarily touching a solid ground.

- Do not handle boards unless they are protected by shielded covering.

7.5.2 REMOVING A BOARD

To remove the boards, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the front panel.

3. Locate the board to be removed.

4. Label and disconnect the system board interface cables.

5. CPU, memory, and power shunt boards are equipped with locking board extractor keys (see Figure 7-9). To unlock and eject these boards, use the following procedure:

   A) Grasp the top and bottom keys (see Figure 7-9).

   B) Squeeze the locking trigger between your thumb and forefinger to unlock the key.

   C) Push the top key up, and the bottom key down. Once the keys are fully extended, slide the board out of the backplane connector toward you until it clears the card cage.

7.5.3 REPLACING A BOARD

To replace the boards, follow these steps:

CAUTION

> The three CPU boards contain unusually tall VLSI components. To avoid collisions between VLSI cooling towers and other board components, be certain to mount the CPU E-board and the VCP-V with the component side facing left. Mount all other boards with the components facing right. Boards must be mounted in dedicated slots. Silkscreens on the top and bottom of the card cage clearly indicate the slot and correct mounting direction of each board.

1. Holding the board vertically, align the board with the guide rails on the top and bottom of the card cage. Push the board straight back into the backplane connector.

2. Push the extractor keys toward the board until the board is firmly seated in the backplane.

   CAUTION

   > To avoid damaging the backplane connectors, be careful not to exert undue pressure. If the board does not insert easily, realign the board and try installing it again.

3. Connect the interface cables labelled and removed in step 4 of Removing a Board.

4. Replace the front panel (refer to Replacing the Front Panel in this chapter).

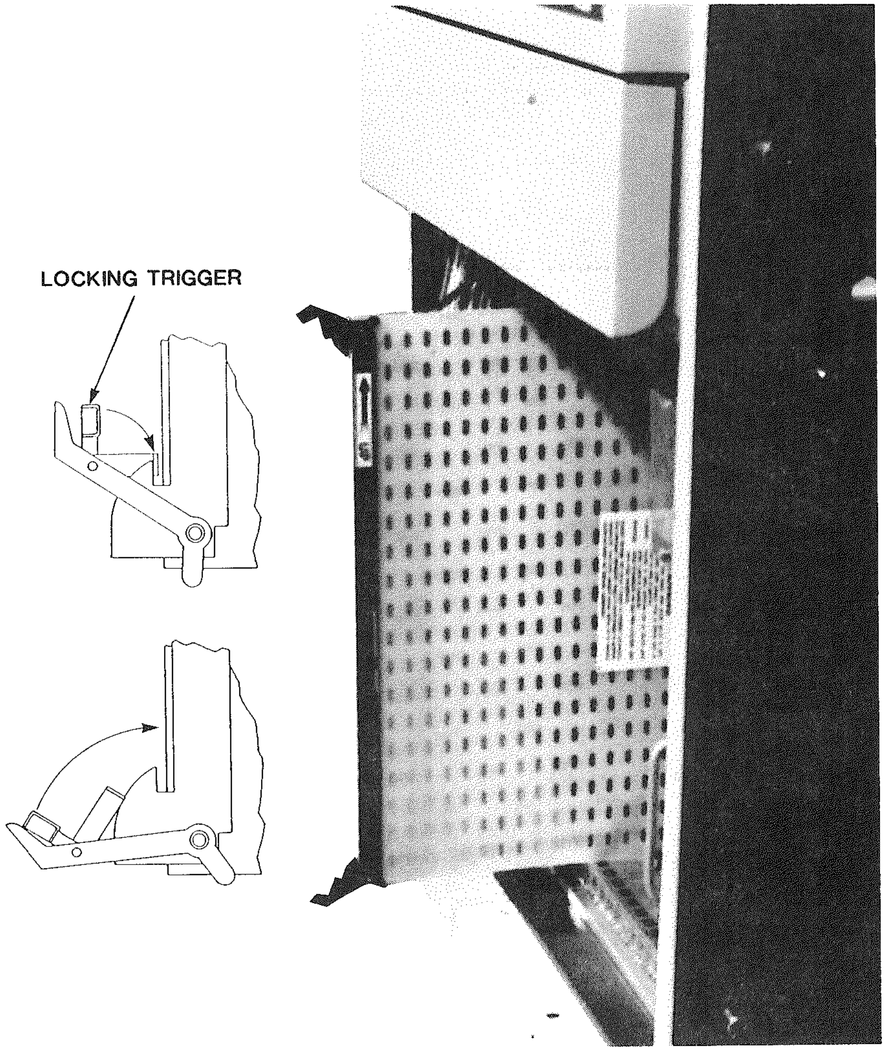


FIGURE 7-9: BOARD REMOVAL

7.6 REMOVING AND REPLACING BOARD RAMS AND PROMS

System boards contain metal oxide semiconductor RAMs and PROMs. These components are FRUs and may have to be replaced if found defective.

CAUTION

> To prevent damage to static-sensitive components, be sure to use the field service grounding kit previously described when completing board RAM and PROM removal/replacement procedures.

7.6.1 REMOVING RAMS AND PROMS

To remove a RAM or PROM, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Slip on the grounded wrist strap and remove the board (refer to Removing System Boards in this chapter).

3. Using a small standard screwdriver, gently ease the RAM or PROM from its socket.

7.6.2 REPLACING RAM AND PROM

To replace a RAM or PROM, follow these steps:

1. Firmly press the new component into its socket.

CAUTION

> Make sure the pins do not bend when reseating the component.

2. Replace the board (refer to Removing and Replacing System Boards in this chapter).

7.7 REMOVING AND REPLACING SYSTEM POWER SUPPLY FUSES

The system power supply fuse is located on the system power supply front panel (see Figure 7-10).

7.7.1 REMOVING THE POWER SUPPLY FUSE

To remove the power supply fuse, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the front panel (refer to Removing the Front Panel in this chapter).

3. Locate the power supply front panel and fuse holder (see Figure 7-10).

4. Push the fuse holder in and twist it counterclockwise a half turn to remove the fuse and holder from the power supply panel.

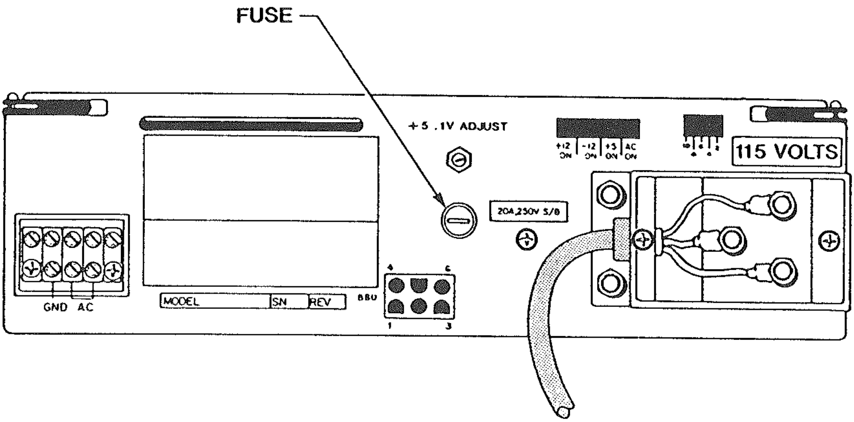


FIGURE 7-10: TLA10113 POWER SUPPLY FUSE REMOVAL

7.7.2 REPLACING THE POWER SUPPLY FUSE

To replace the power supply fuse, follow these steps:

1. Install either FUS0224-036 (domestic 60Hz 20 amp slow blow) or FUS6215-007 (international 50Hz 10 amp slow blow) into the fuse holder.

2. Insert the fuse holder into the power supply front panel (see Figure 7-10). Secure the fuse holder with a half turn clockwise.

7.8 REMOVING AND REPLACING MODEL TLA10113 POWER SUPPLIES

The two Model TLA10113 power supplies are installed in slots PS2 and PS3 of the system card cage.

NOTE

PS2 faces left in the card cage and PS3 faces right (see Figure 7-11).

7.8.1 REMOVING A POWER SUPPLY

To remove the system power supply, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the ac line cord from the external power source.

3. Remove the front panel (refer to Removing the Front Panel in this chapter).

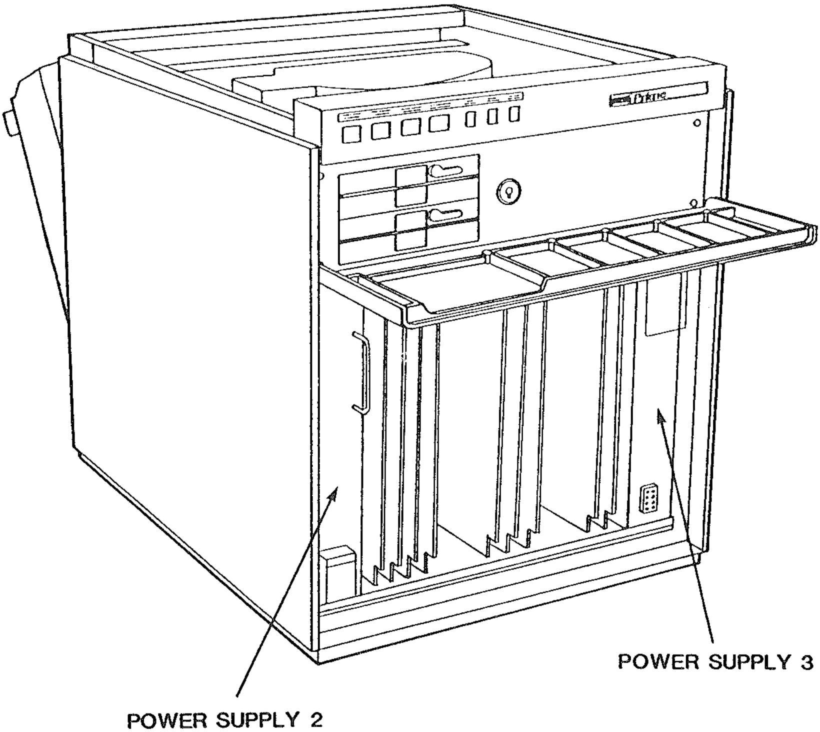


FIGURE 7-11: POWER SUPPLY LOCATIONS

4. Locate the system power supply front panel (see Figure 7-11). Label and remove all cables attached to the power supply front panel, except the ac power connection cable.

5. Remove the two screws securing the protective cover shielding the ac power connector lugs (see Figure 7-12).

6. Label and remove the three power cables from the lugs. Hexagonal nuts secure the cables to the lugs (See Figure 7-12).

7. Locate and remove the two hex nuts securing the power cable bracket to the system cabinet (see Figure 7-12).

8. Remove the power cable securing bracket and ac power cord.

9. To eject the power supply from the chassis, push the top power supply ejector key to the left (to unlock it) and up (refer to Figure 7-11). Push the lower key left (to unlock it) and down.

10. Once the keys are fully extended, back the power supply out of the backplane connector toward you until it clears the card cage.

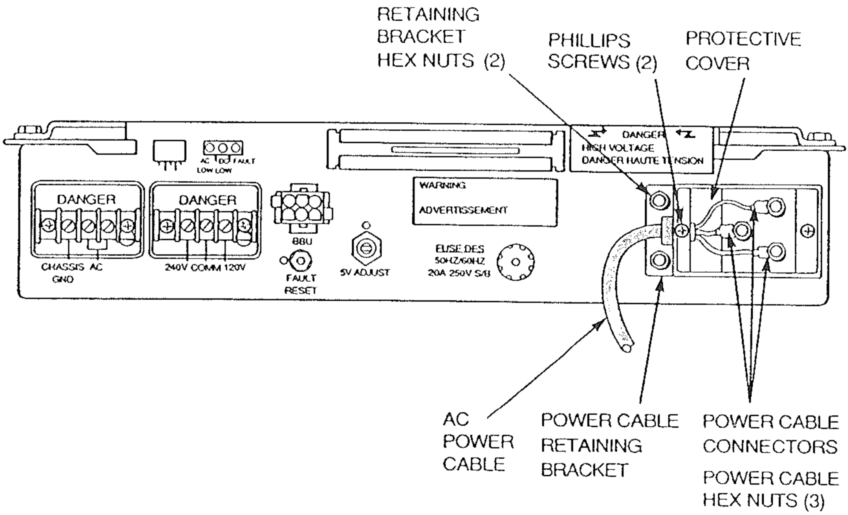


FIGURE 7-12: TLA10113 POWER SUPPLY REMOVAL

7.8.2 REPLACING A POWER SUPPLY

To replace the system power supply, follow these steps:

1. Align the new power supply in slots PS2 or PS3 of the card cage.

2. Push the power supply into the slot until it rests against the backplane connectors.

3. Push the top ejector key down and lift the bottom ejector key up until the power supply is firmly seated in the backplane.

4. Align the power cord securing bracket with the ac power cables over the ac power lugs on the front panel (see Figure 7-12). Replace and secure the ac cables to the lugs with the three hex nuts.

5. Replace and tighten the securing nuts for the bracket and plate. Place the protective cover over the lugs and install and tighten the cover securing screws.

6. Replace all cables connected to the power supply front panel.

7. Replace the front panel (refer to Replacing the Front Panel in this chapter).

7.9 REMOVING AND REPLACING THE MEMORY BATTERY BACKUP UNIT (MBBU)

The following subsections provide removal and replacement procedures for the memory battery backup unit.

CAUTION

You must install a power shunt board (ESA10252-001) in the card cage before powering up the system with the memory battery backup unit removed. Failure to do so could severely damage the system. Refer to Verifying Power Shunt Board Installation in Chapter 2 of this manual for installation verification procedures before applying power to the system.

All Model 4050/4150 systems require an MBBU Safety Shield (MEC10495-001) in slot I/O 4. Do not operate the system with an MBBU unless this shield is in place. The shield is secured to the card cage by two flat-head captive screws.

7.9.1 REMOVING THE MEMORY BATTERY BACKUP UNIT (MBBU)

To remove the MBBU, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the ac line cord from the external power source.

3. Remove the front panel (refer to Removing and Replacing the Front Panel in this chapter).

4. Locate the MBBU. Label and remove the POWER-IN and POWER ENABLE cables from the unit (see Figure 7-13).

5. To eject the MBBU from the chassis, push the top power supply ejector key up and the bottom key down.

6. Once the keys are fully extended, back the MBBU out of the backplane connector toward you until it clears the card cage.

7.9.2 REPLACING THE MEMORY BATTERY BACKUP UNIT (MBBU)

To replace the MBBU, follow these steps:

1. Align the MBBU in slot PS1 of the card cage.

2. Push the unit into the slot until it rests against the backplane connectors.

3. Push the top ejector key down and lift the bottom ejector key up until the MBBU is firmly seated in the backplane.

4. Replace all cables connected to the MBBU front panel.

5. Replace the front panel (refer to Removing and Replacing the Front Panel in this chapter).

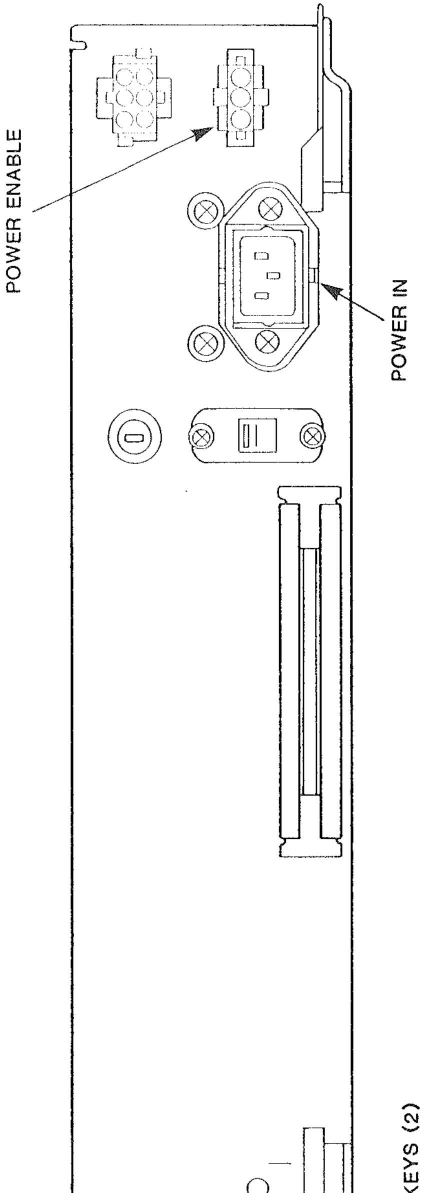


FIGURE 7-13: MBBU REMOVAL

7.10 REMOVING AND REPLACING THE BLOWER ASSEMBLY

The following subsections provide removal and replacement procedures for the blower assembly (see Figure 7-1).

NOTE

> The blower unit and the air temperature sensor are one Field Replaceable Unit.

7.10.1 REMOVING THE BLOWER ASSEMBLY

To remove the blower, follow these steps.

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the top cover and tilt open the rear door assembly 45 degrees (refer to Removing and Replacing System Cabinet Covers in this chapter).

3. Disconnect the air flow sensor at its mate 'n lock connector (see Figure 7-14).

4. Disconnect the blower bypass switch at J1 on the blower (see Figure 7-14).

5. At the rear of the system, remove the blower temperature sensor by removing the two screws that secure the sensor mounting plate to the plenum (see Figure 7-14).

6. Disconnect the blower power cable from the system backplane (see Figure 7-14).

7. Remove the two screws that secure the blower retaining bracket to the exhaust duct (see Figure 7-14).

8. Remove the three screws that secure the three blower housing mounting brackets to the top of the card cage (see Figure 7-14).

9. Carefully lift the blower assembly from the cabinet.

7.10.2 REPLACING THE BLOWER ASSEMBLY

To replace the blower assembly, follow these steps:

1. Position the blower over the opening on top of the card cage. Make sure the blower exhaust port is flush against the cabinet exhaust duct and the three blower mounting brackets are positioned over the threaded screw holes on top of the card cage (see Figure 7-14).

2. Secure the blower to the card cage with three screws.

3. Replace the blower retaining bracket. Secure it in place with two screws.

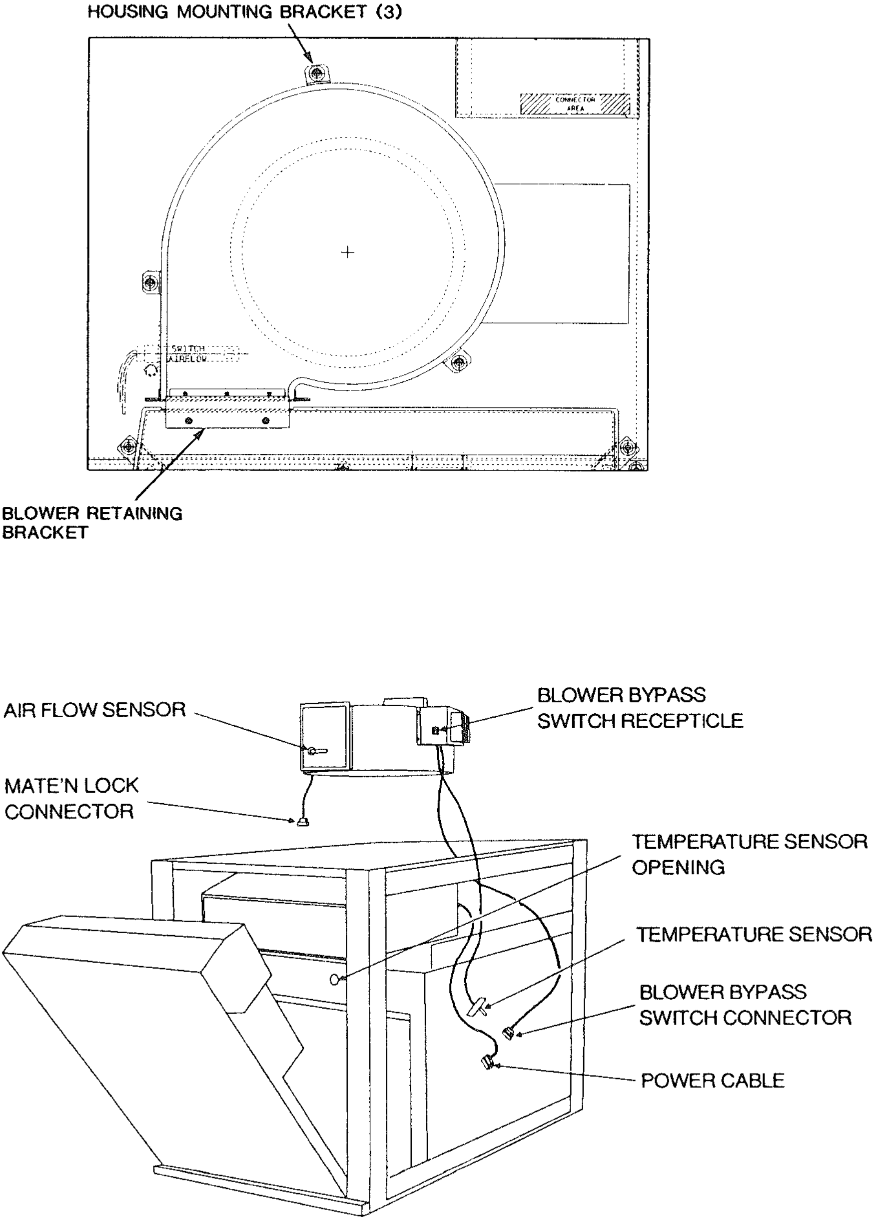


FIGURE 7-14: BLOWER ASSEMBLY REMOVAL

4. Connect the front panel bypass switch cable at J1 on the blower.

5. Connect the air flow sensor at its mate 'n lock connector.

6. Connect the blower power cable to the system backplane.

7. Install the blower temperature sensor in the plenum and secure it in place with two screws.

7.11 REMOVING AND REPLACING THE AIR FLOW SENSOR

The following subsections provide removal and replacement instructions for the air flow sensor (see Figure 7-15).

7.11.1 REMOVING THE AIR FLOW SENSOR

To remove the air flow sensor, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the top cover (refer to Removing and Replacing System Cabinet Covers in this chapter).

3. Remove the Phillips head screw that secures the air flow sensor and mounting plate to the blower unit housing (see Figure 7-15)

4. Remove the air flow sensor and plate from the opening in the blower and disconnect the mate 'n lock connector (see Figure 7-15).

7.11.2 REPLACING THE AIR FLOW SENSOR

To replace the air flow sensor, follow these steps:

NOTE

When installing the sensor, be sure the air flow opening faces the front of the system (see Figure 7-15).

1. Holding the air flow sensor and mounting plate with the air flow opening facing the front of the system, insert the assembly into its opening in the blower housing (see Figure 7-15).

2. Replace the Phillips screw that secures the sensor mounting plate to the blower housing (see Figure 7-15).

3. Reconnect the mate 'n lock connector (see Figure 7-15).

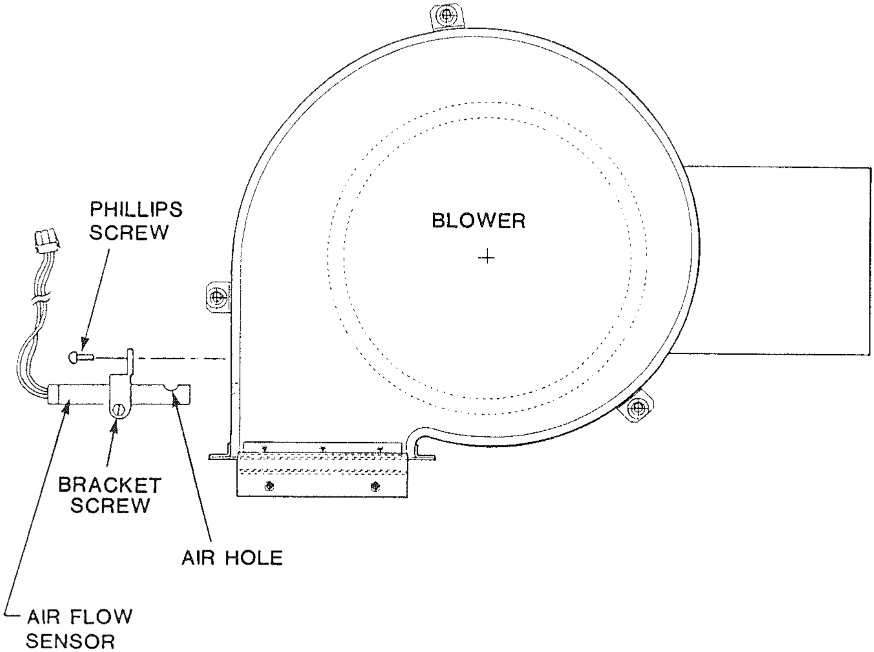


FIGURE 7-15: AIR FLOW SENSOR REMOVAL

7.12 REMOVING AND REPLACING THE SYSTEM AIR FILTER

The subsections that follow provide removal and replacement instructions for the system air filter (see Figure 7-16).

7.12.1 REMOVING THE AIR FILTER

To remove the air filter follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the front panel (refer to Removing and Replacing System Cabinet Covers Rin this chapter).

3. Remove the air filter stop bracket (MEC11036-001) by lifting the snap fastener that secures the bracket to the lower rail of the card cage (see Figure 7-16).

4. Grasp the air filter by its plastic tab and slide the filter from the system card cage (see Figure 7-16).

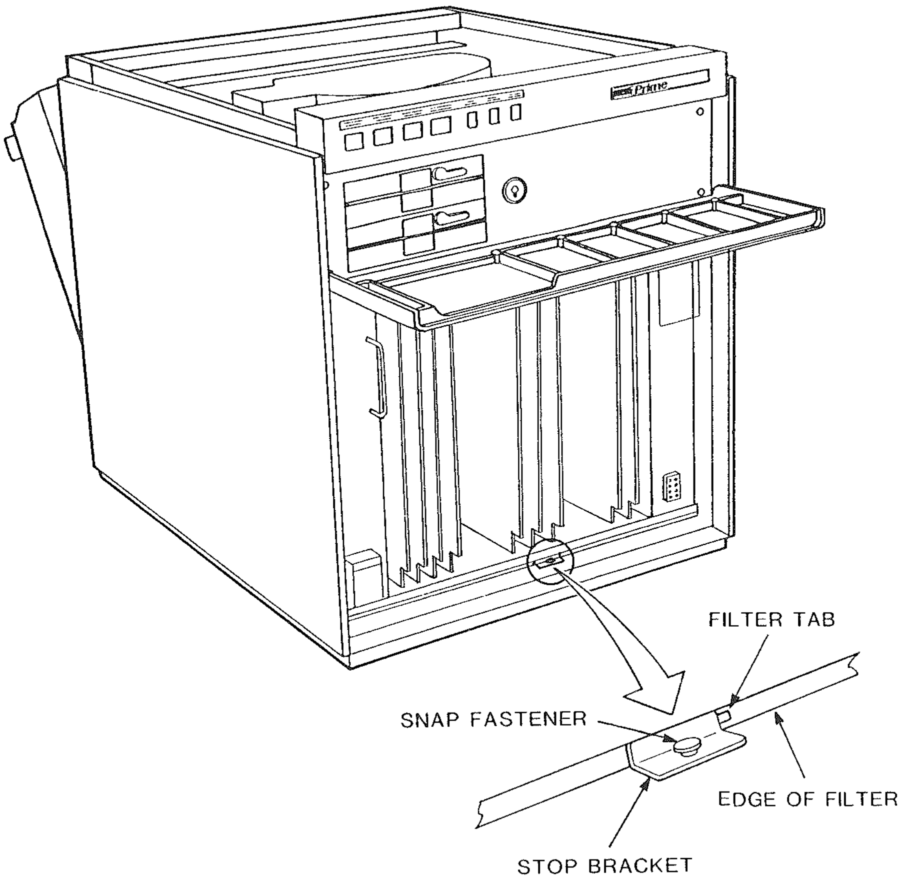


FIGURE 7-16: AIR FILTER REMOVAL

7.12.2 REPLACING THE AIR FILTER

To replace the air filter, follow these steps:

1. Holding the air filter so that the plastic tab is toward you, align the filter with its guide rails below the system card cage.

2. Slide the air filter into the cabinet until its leading edge is flush with the card cage.

3. Replace the air filter stop bracket.

CAUTION

> The air filter and stop bracket are UL-required. Do not power up the system unless both are in place.

4. Replace the front panel.

7.13 REMOVING AND REPLACING THE SYSTEM BACKPLANE

The following subsections provide removal and replacement procedures for the system backplane (see Figure 7-17).

7.13.1 REMOVING THE SYSTEM BACKPLANE

To remove the system backplane, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the front panel and tilt open the rear door 90 degrees (refer to Removing and Replacing System Cabinet Covers in this chapter).

3. Remove all system boards from the card cage (refer to Removing and Replacing System Boards in this chapter).

4. Remove the system power supplies and the battery backup unit, if one is present, from the card cage (refer to Removing and Replacing Power Supplies and Removing and Replacing the Battery Backup Unit in this chapter).

5. Label and remove all cable connectors from the backplane.

6. Remove the plastic protective backplane cover by lifting the snap fasteners that secure the cover to the backplane.

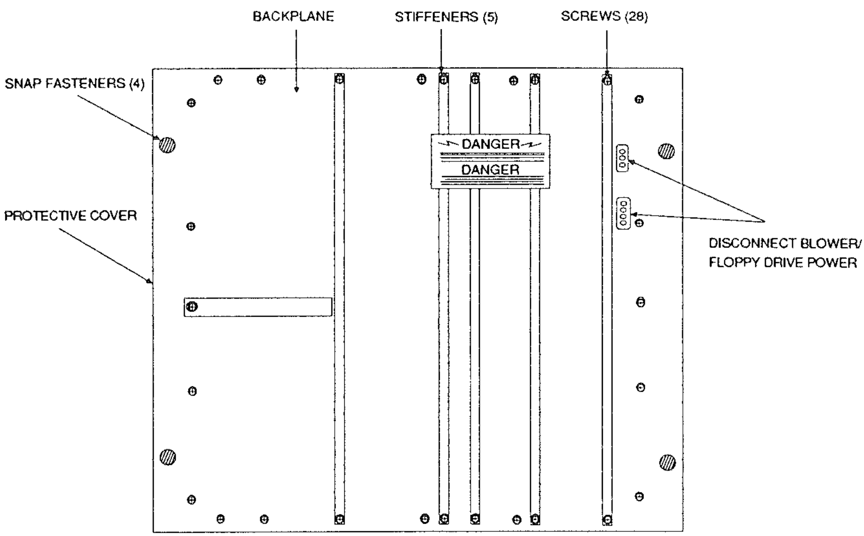


FIGURE 7-17: BACKPLANE REMOVAL

7. Remove the 28 Phillips screws securing the backplane to the system cabinet. There are nine on top, nine on the bottom and five on each side of the backplane (see Figure 7-17).

NOTE

The nine screws on the top and bottom also secure five backplane stiffeners to the cabinet (see Figure 7-17).

8. The backplane will tip toward you when the screws are removed. Lift the backplane from the rear of the system cabinet.

7.13.2 REPLACING THE SYSTEM BACKPLANE

To replace the system backplane and all backplane-related components, follow these steps:

1. Align the backplane with the system cabinet and install the 28 Phillips and regular screws securing the backplane and stiffeners to the cabinet.

2. Replace the protective plastic cover on the backplane.

3. Install all cable connectors to their correct positions on the backplane.

4. Install the system power supply.

5. Install the battery backup unit, if one is present.

6. Install all system boards into the card cage.

7. Replace the front panel and close the rear door assembly.

7.14 REMOVING AND REPLACING THE SYSTEM AC POWER CABLE

The ac power cable is connected to the mainbay and peripheral cabinet PDU ac connectors (see Figure 7-18).

7.14.1 REMOVING THE SYSTEM AC POWER CABLE

To remove the ac power cable, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Locate and disconnect ac power cable from the external ac source.

3. Unlock the ac power cable connector from the PDU by pushing the connector in firmly and twisting it counterclockwise (see Figure 7-18).

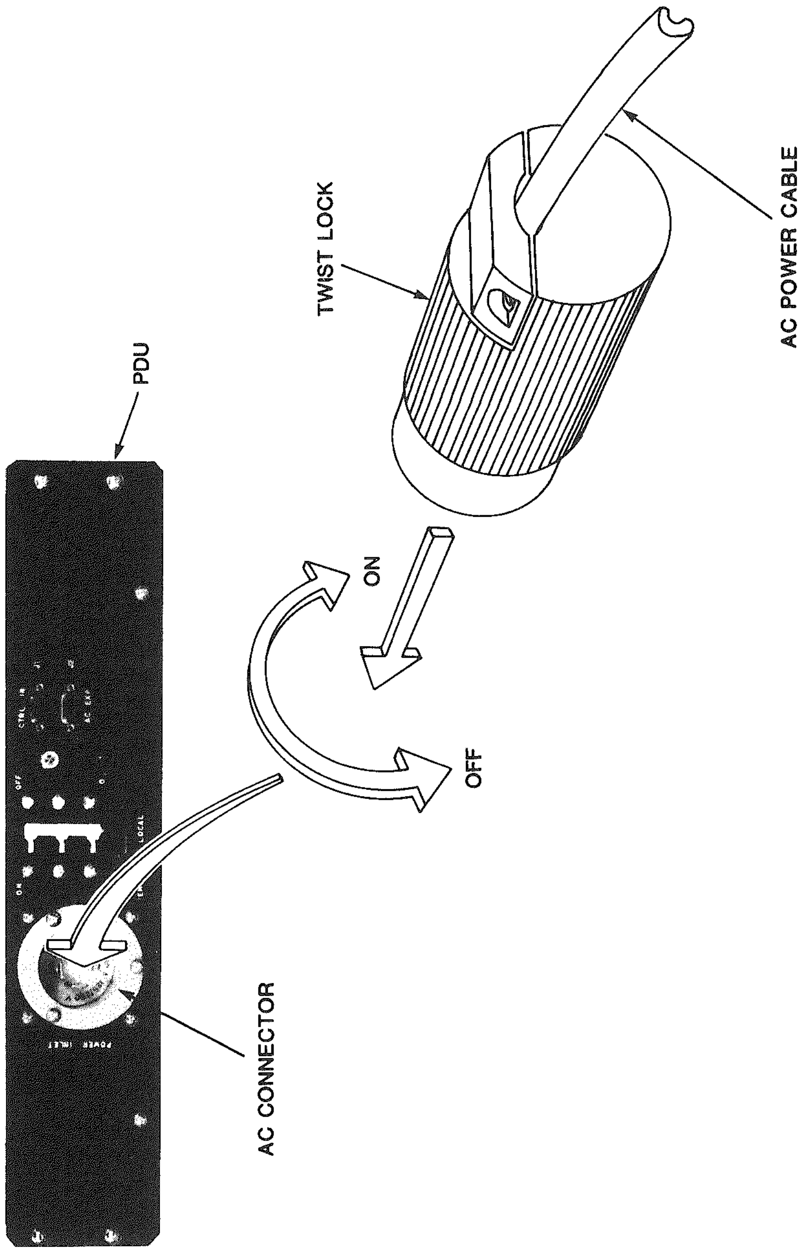


FIGURE 7-18: AC POWER CABLE REMOVAL

7.14.2 REPLACING THE SYSTEM AC POWER CABLE

To replace the ac power cable, follow these steps:

1. Mate the ac power cable connector to the PDU at the bottom rear of the system cabinet.

2. Lock the connector in place by pushing it in firmly and twisting it clockwise.

3. Connect the ac power cable to the external power source.

7.15 REMOVING AND REPLACING THE POWER DISTRIBUTION UNIT (PDU)

PDUs are mounted in the mainbay and peripheral cabinets. The following subsections provide PDU removal and replacement procedures:

- Removing and Replacing the Mainbay PDU

- Removing and Replacing the Peripheral Cabinet PDU

7.15.1 REMOVING THE MAINBAY PDU

To remove the mainbay PDU, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the system ac power cable (refer to Removing and Replacing the System AC Power Cable in this chapter).

3. Label and disconnect the CONTROL IN and AC EXP cables from the PDU front panel (see Figure 7-19).

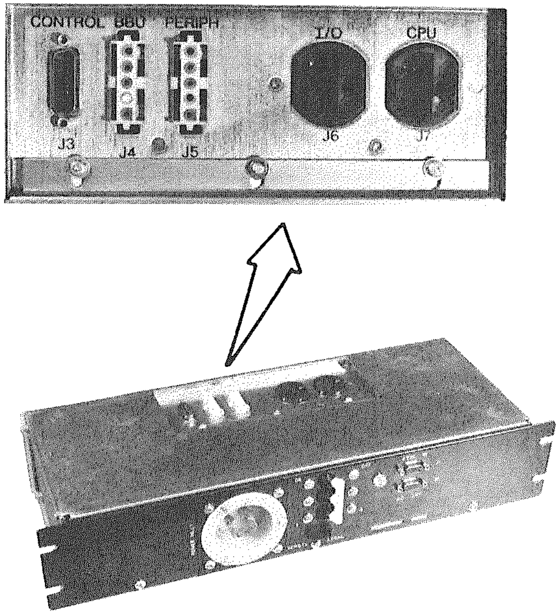
4. Tilt open the rear door 45 degrees.

5. Label and disconnect the two Model 7778 power supply cables (J6 and J7), the MBBU cable if present (J4), the ICS3 power cable if present (J5), and the control cable (J3) (see Figure 7-19).

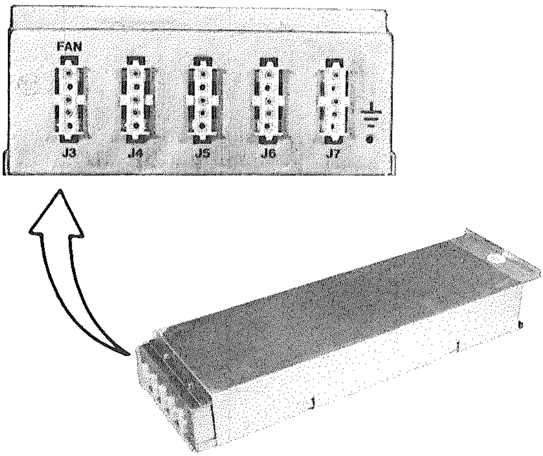
6. Close and lock the rear door.

7. Remove the four screws that secure the PDU to the rear door and set them aside (see Figure 7-19).

8. Slide the PDU from the cabinet.



MAINBAY PDU



PERIPHERAL BAY PDU

FIGURE 7-19: MAINBAY PDU REMOVAL

7.15.2 MAINBAY PDU REPLACEMENT

To replace the mainbay PDU, follow these steps.

1. With the rear door in the upright position, slide the PDU into its opening at the bottom of the rear door (see Figure 7-19).

2. Replace and tighten the four screws that secure the PDU to the rear door (see Figure 7-19).

3. Tilt open the rear door assembly 45 degrees.

4. Connect the two Model 7778 power supply cables (PS3 to J6 and PS2 to J7), the MBBU cable if present (J4), the ICS3 power cable if present (J5), and the control cable (J3).

5. Close and lock the rear door.

6. Connect the ac power cable (refer to Removing and Replacing the AC Power Cable in this chapter) and the CONTROL IN and AC EXP cables to the PDU front panel.

7.15.3 REMOVING THE PERIPHERAL CABINET PDU

To remove the peripheral cabinet PDU, follow these steps:

1. Power down the peripheral bay (refer to System Power-Down in this chapter).

2. Remove the ac power cable (refer to Removing and Replacing the System AC Power Cable in this chapter).

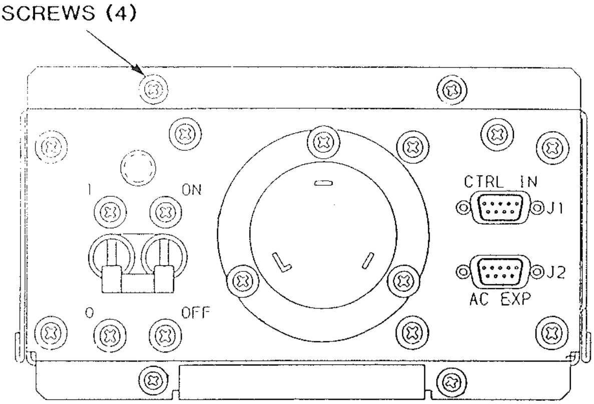
3. From the front of the cabinet, remove the lower cover panel from its ball stud fasteners, then remove the two screws that secure the cover plate to the cabinet chassis (see Figure 7-20) to access the peripheral device power cables.

4. Label and disconnect the power cables from the PDU (see Figure 7-20).

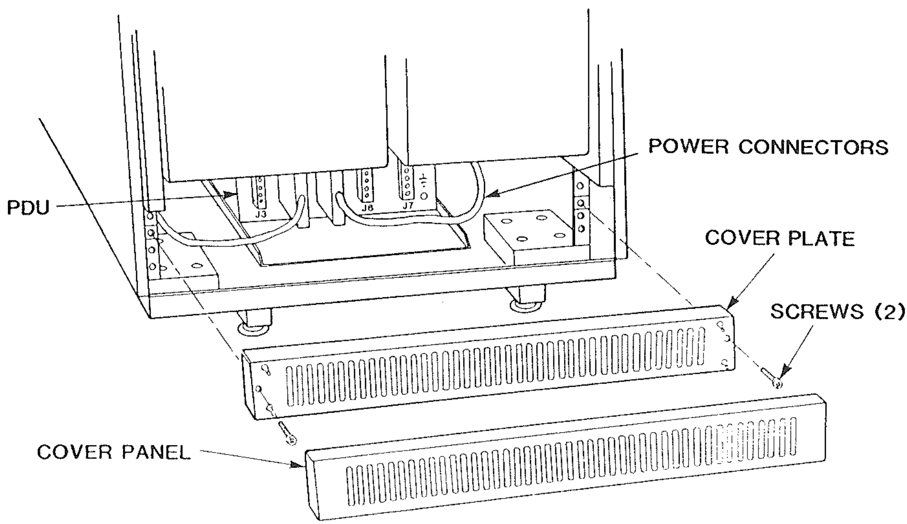
5. From the rear of the cabinet, label and disconnect all external PDU cables.

6. Remove the four screws that secure the PDU to the peripheral cabinet and set them aside (see Figure 7-20).

7. Slide the PDU from the chassis.



PDU (REAR VIEW)



PERIPHERAL CABINET (FRONT VIEW)

PDU (FRONT VIEW)

FIGURE 7-20: PERIPHERAL BAY PDU REMOVAL

7.15.4 REPLACING THE PERIPHERAL CABINET PDU

To replace the peripheral cabinet PDU, follow these steps.

1. Slide the PDU into the cabinet, then replace and tighten the four screws that secure the PDU to the chassis (see Figure 7-20).
2. Connect the external cables you removed in Step 5 of the removal procedure.
3. From the front of the cabinet, connect the device power cables you removed in Step 4 of the removal procedure.
4. Install the cover plate and cover panel (see Figure 7-20)
5. Install the ac power cable.

7.16 REMOVING AND REPLACING THE FLOPPY DISK DRIVES

The following subsections provide removal and replacement procedures for the twin floppy disk drives (see Figure 7-1).

7.16.1 REMOVING A FLOPPY DISK DRIVE

To remove a floppy disk drive, follow these steps:

NOTE

You can remove each floppy disk drive independently.

1. Power down the system (refer to System Power-Down in this chapter).
2. Open the floppy disk drive access door and remove the top and left side covers.
3. Label and disconnect the floppy drive control and power cables (see Figure 7-21).
4. Remove the three screws (one on the left and two on the right) that secure the floppy drives to the mounting bracket (see Figure 7-21).

   NOTE

   Do not remove the disk drive mounting bracket from the chassis.

5. Slide the floppy drive from the mounting bracket through the opening in the floppy drive access door (see Figure 7-21).

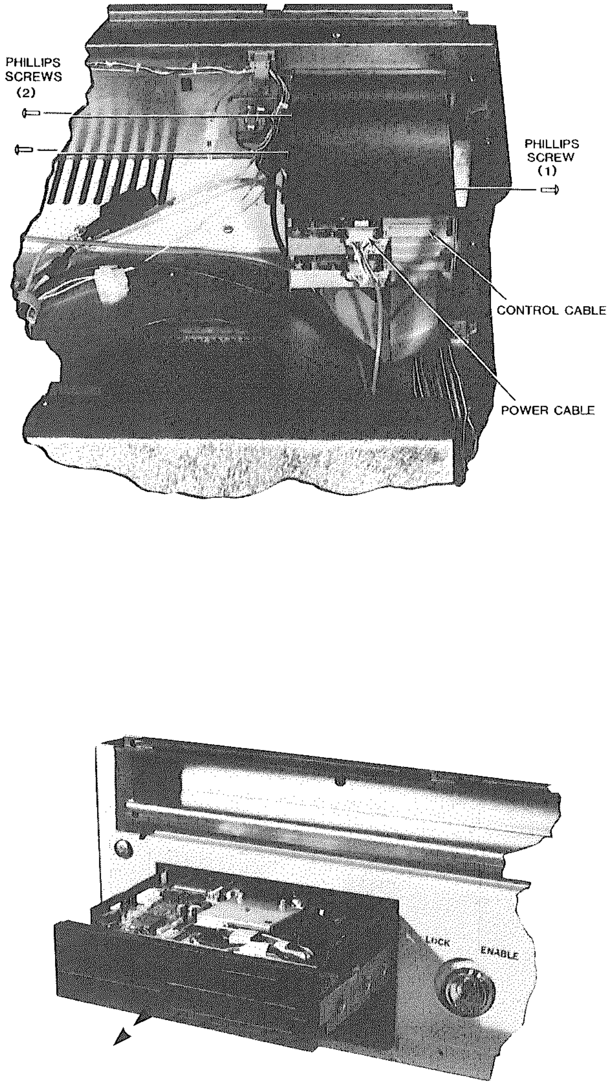


FIGURE 7-21: FLOPPY DISK DRIVE REMOVAL

7.16.2 REPLACING A FLOPPY DISK

To replace a floppy disk drive, follow these steps.

1. Slide the disk drive through the opening in the drive access door until the drive's front panel is flush with the access door panel and the three holes on the floppy drive mounting bracket (one on the left and two on the right) are aligned with their corresponding holes on the drive chassis.

2. Secure the drive to the mounting bracket with the three screws you removed in step 4 of the floppy drive removal procedure.

3. Connect the control and power cables you removed in step 3 of the floppy drive removal procedure.

4. Replace the top and left side covers, and close the floppy drive access door.

7.17 REMOVING AND REPLACING THE PRIMENET NODE CONTROLLER AND MJ-BOX

When the system is configured with the PNC-II option, a PNC Modular Junction Box is mounted on the bulkhead panel and a controller board is mounted in the system chassis.

Refer to Removing and Replacing System Boards and Removing and Replacing System Board Interface Cables in this chapter for PNC-II controller board and cable removal and replacement information.

CAUTION

> To avoid bringing down the network when removing the controller board or cable, be sure to switch the Disconnect Node control on the junction box to the DIS position.

Refer to the following subsections for modular junction box removal and replacement procedures.

7.17.1 REMOVING THE PNC MJ-BOX

To remove the PNC MJ-BOX, follow these steps:

NOTE

> If you are exchanging the existing MJ-BOX for another, you must bring the network down, then remove the twinax cables.

1. Power down the system (refer to System Power-Down in this chapter).

2. Switch the Disconnect Node control on the junction box to the DIS position, and label and disconnect the twinax input/output cables.

3. Remove the four screws securing the PNC MJ-Box to the bulkhead panel (see Figure 7-22).

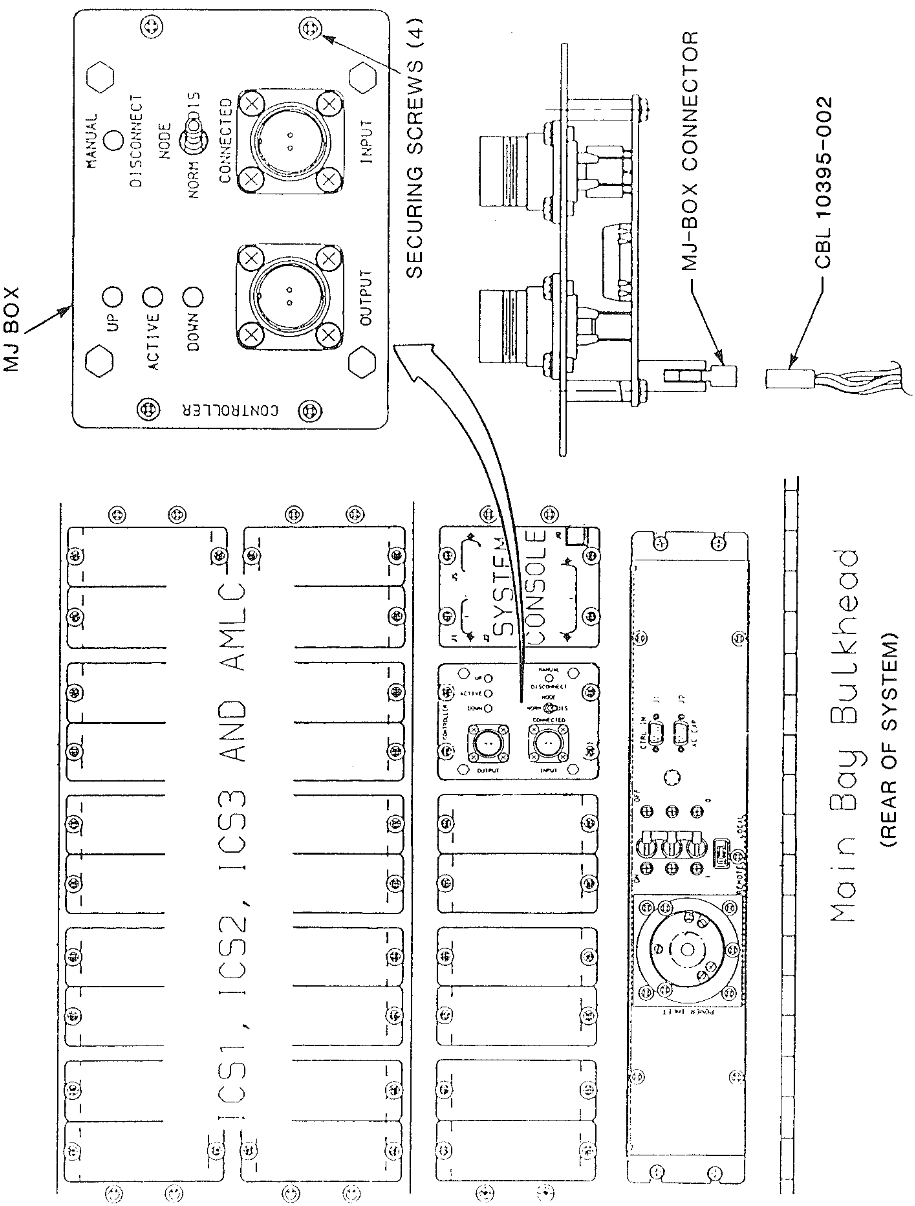


FIGURE 7-22: MJ BOX REMOVAL

4. Pull the box toward you until the assembly clears the system bulkhead.

5. Disconnect the controller cable.

7.17.2 REPLACING THE PNC MJ-BOX

To replace the PNC MJ-Box, follow these steps:

1. Connect the controller cable to the rear of the junction box.

2. Insert the junction box into the system bulkhead and secure the assembly with four screws (see Figure 2-22).

3. Connect the twinax input/output cables, and switch the Disconnect Node control on the junction box to the NORM position (see Figure 2-22).

7.18 REMOVING AND REPLACING THE ICS3

This section contains removal and replacement procedures for the following Intelligent Communications Controller Model 3 (ICS3) FRUs in the mainbay and peripheral cabinets:

- Controller Board
- Line Adapter Card
- Buffer Card
- LAC Backplane Assembly
- Power Supply
- Power Supply Fuse
- Fan Tray Assembly

7.18.1 REMOVING AND REPLACING THE ICS3 CONTROLLER BOARD

To remove or replace the ICS3 controller board, refer to Removing and Replacing System Boards in this chapter.

7.18.2 REMOVING AND REPLACING ICS3 LINE ADAPTER CARDS

This section provides procedures for removing and replacing the line adapter cards in the ICS3's 16-slot card cage. The LAC types and their part numbers are as follows:

- Asynchronous LAC assembly (ESA10063-001)
- Synchronous EIA LAC assembly (ESA10064-001)
- Synchronous DDS LAC assembly (ESA10065-001)

CAUTION

Power down the ICS before removing any LAC.

7.18.2.1 Removing an ICS3 LAC Card

To remove a line adapter card, follow these steps:

1. Power down the ICS3 by pressing the On/Off button on the ICS3 card cage. Verify the unit is shutdown by making sure the On/Off button is fully extended.

2. Label and disconnect all device cables attached to the line adapter card.

3. Loosen the top and bottom spring-loaded thumb screws on the line adapter card (see Figure 7-23) and remove the card from the card cage chassis.

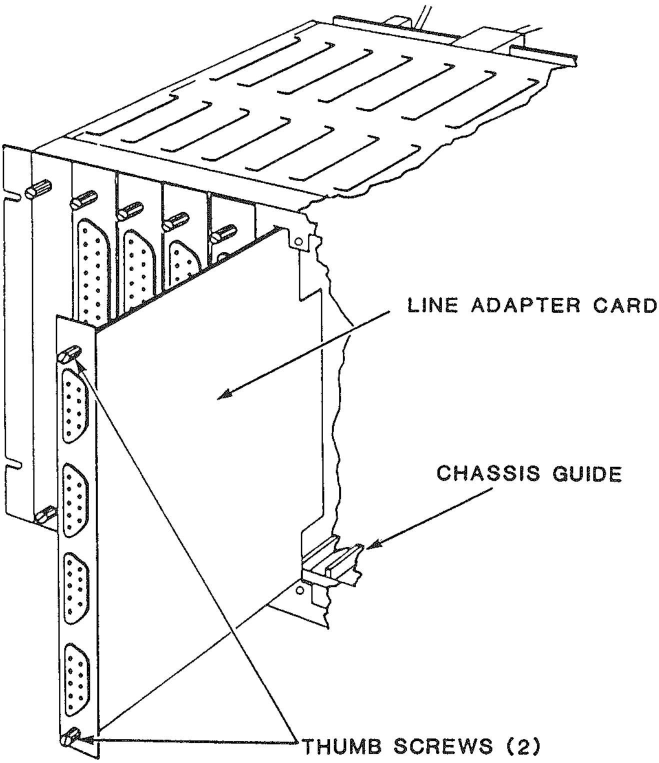


FIGURE 7-23: ICS3 LAC REMOVAL

7.18.2.2 Replacing an ICS3 LAC Card

To replace a line adapter card, follow these steps:

1. Hold the line adapter card vertically, components facing left.

2. Align the card with the top and bottom chassis guides. Push the card in (see Figure 7-23) until it contacts its backplane slot.

3. Seat the line adapter card (see Figure 7-23). Finger tighten the top and bottom spring-loaded thumb screws.

4. Connect all line adapter card device cables.

7.18.3 REMOVING AND REPLACING THE ICS3 BUFFER CARD

The following subsections provide ICS3 buffer card removal and replacement procedures.

7.18.3.1 Removing the ICS3 Buffer Card

To remove the ICS3's buffer card, follow these steps:

NOTE

> In mainbay installations, the ICS3 buffer card is accessible without removing the ICS3 card cage from the system bulkhead. In peripheral cabinet installations, you must remove the ICS3 cage cage from the cabinet to access the ICS3 buffer card.

1. Power down the system (refer to System Power-Down in this chapter).

2. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, unlock the two fasteners on both sides of the rear door and tilt the rear door. Proceed to step 3.

   B) If the ICS3 is installed in the peripheral cabinet, remove the rear panel. Note the exact location of the card cage against the mounting rail. Remove the four screws securing the 16-slot card cage to the mounting rail and withdraw the card cage from the cabinet. Place the card cage on the floor, taking care not to exert undue strain on the power and control cables. Proceed to step 3.

3. Unlock and disconnect the buffer card-to-internal bulkhead cable (CBL10137-001) from connector P01 (see Figure 7-24) located on the buffer card.

4. Disconnect the power supply cable (CBL10139-001) from connector J10 (see Figure 7-24) located on the LAC backplane.

5. Using a 5/16-inch nut driver, loosen and remove the two nuts and pressure washers (see Figure 7-24) securing the buffer card to the LAC backplane's standoffs.

6. Separate the connectors of the buffer card from the LAC backplane assembly (see Figure 7-24).

7.18.3.2 Replacing the ICS3 Buffer Card

To replace the ICS3's buffer card, follow these steps:

1. Make sure the buffer card is properly configured. Refer to Verifying ICS3 Configuration in Chapter 2 of this manual.

2. Position and press the buffer card onto the LAC backplane assembly's connector J09 (see Figure 7-24).

3. Using a 5/16-inch nut driver, tighten the two nuts and pressure washers (see Figure 7-24) securing the buffer card to the LAC backplane's standoffs.

4. Connect and lock the buffer card-to-internal bulkhead cable (CBL10137-001) to connector P01 (see Figure 7-24) located on the buffer card.

5. Connect the power supply cable (CBL10139-001) to connector J10 (see Figure 7-26) located on the LAC backplane assembly.

6. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, return the rear door to its full upright position and lock the two fasteners that secure the rear door to the chassis.

   B) If the ICS3 is installed in the peripheral cabinet, slide the 16-slot card cage into the cabinet and secure the card cage to the mounting rail with four screws. Replace the rear panel.

7.18.4 REMOVING AND REPLACING THE ICS3 LAC BACKPLANE ASSEMBLY

The following subsections provide ICS3 LAC backplane assembly removal and replacement procedures.

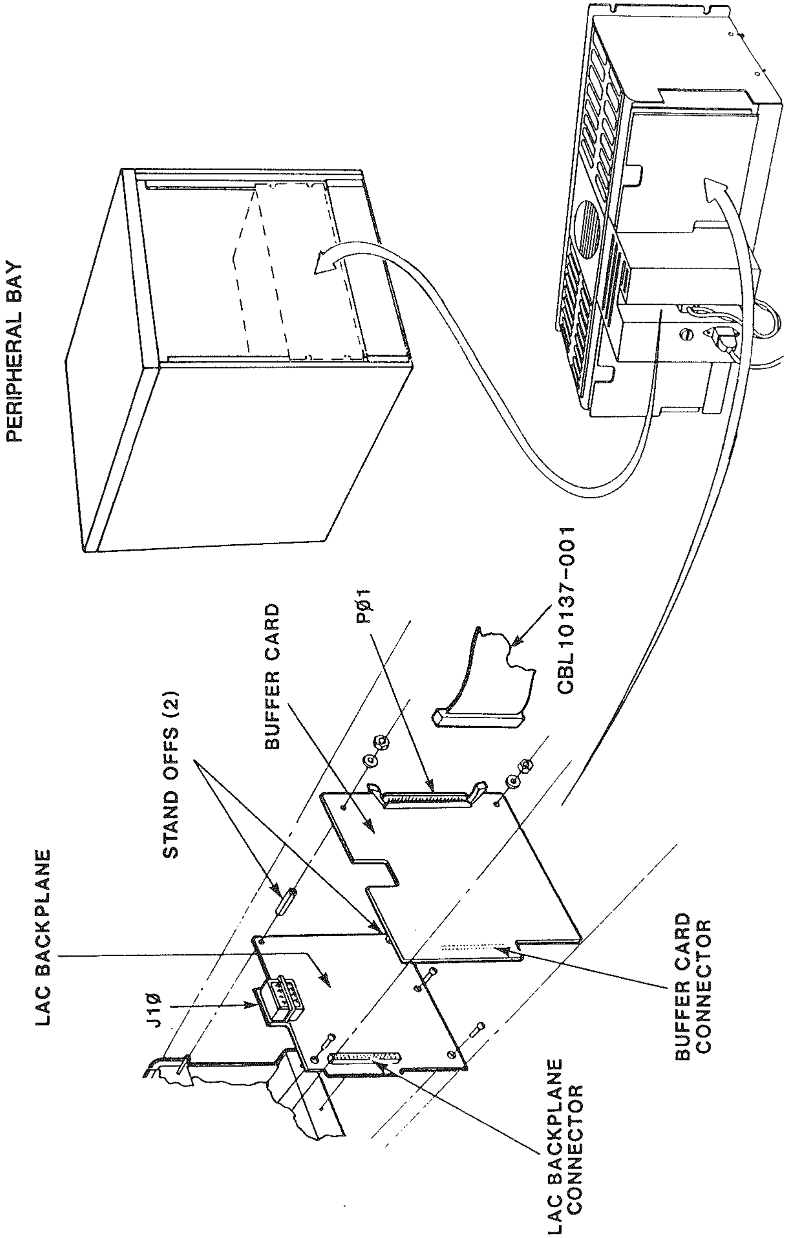


FIGURE 7-24: ICS3 BUFFER CARD/LAC BACKPLANE REMOVAL

7.18.4.1 Removing the LAC Backplane Assembly

NOTE

> In mainbay installations, the ICS3 LAC backplane is accessible without removing the ICS3 card cage from the system bulkhead. In peripheral cabinet installations, you must remove the ICS3 cage cage from the cabinet to access the ICS3 LAC backplane.

To remove the ICS3's LAC backplane assembly, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter) and complete the LAC card removal procedures described in the previous subsection.
2. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, unlock the two fasteners on both sides of the rear door and tilt the rear door. Proceed to step 3.

   B) If the ICS3 is installed in the peripheral cabinet, remove the rear panel. Note the location of the card cage against the mounting rail. Remove the four screws securing the 16-slot card cage to the mounting rail and withdraw the card cage from the cabinet. Place the card cage on the floor, taking care not to exert undue strain on the power and control cables. Proceed to step 3.
3. Unlock and disconnect the buffer card-to-internal bulkhead cable (CBL10137-001) from connector P01 (see Figure 7-24) located on the buffer card.
4. Disconnect the power supply cable (CBL10139-001) from connector J10 (see Figure 7-24) located on the LAC backplane.
5. Using a 5/16-inch nut driver, loosen and remove the two nuts and pressure washers (see Figure 7-24) securing the buffer card to the LAC backplane's standoffs.
6. Separate the connectors of the buffer card from the LAC backplane assembly (see Figure 7-24).
7. Loosen the top and bottom spring-loaded thumb screws on each line adapter card (see Figure 7-23). Back the cards out from the backplane about one inch.
8. Loosen and remove the two screws (see Figure 7-24) securing the left side of the LAC backplane assembly.
9. Loosen and remove the two standoffs (see Figure 7-24) securing the right side of the LAC backplane assembly. Remove the LAC backplane assembly.

7.18.4.2 Replacing the LAC Backplane Assembly

To replace the ICS3's LAC backplane assembly, follow these steps:

1. Position the LAC backplane assembly against the card cage. Insert and tighten the two screws (see Figure 7-24) securing the left side of the LAC backplane assembly to the card cage.

2. Insert and tighten the two standoffs (see Figure 7-24) securing the right side of the LAC backplane assembly.

3. Push in and seat each line adapter card (see Figure 7-23). Finger tighten the top and bottom spring-loaded thumb screws.

4. Position and press the buffer card onto connector J09 (see Figure 7-24) located on the LAC backplane assembly.

5. Using a 5/16-inch nut driver, tighten the two nuts and pressure washers (see Figure 7-24) securing the buffer card to the LAC backplane standoffs.

6. Connect the power supply cable (CBL10139-001) to connector J10 (see Figure 7-24) located on the LAC backplane.

7. Connect and lock the buffer card-to-internal bulkhead cable (CBL10137-001) to connector P01 (see Figure 7-24) located on the buffer card.

8. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, return the rear door to its full upright position and lock the two fasteners that secure rear door to the chassis.

   B) If the ICS3 is installed in the peripheral cabinet, slide the 16-slot card cage into cabinet and secure the card cage to the mounting rail place with four screws. Replace the rear panel.

7.18.5 REMOVING AND REPLACING THE ICS3 POWER SUPPLY

The following subsections provide ICS3 power supply removal and replacement procedures:

7.18.5.1 Removing the ICS3 Power Supply

To remove the ICS3 power supply, follow these steps:

NOTE

> In mainbay installations, the ICS3 power supply is accessible without removing the ICS3 card cage from the system bulkhead. In peripheral cabinet installations, you must remove the ICS3 cage cage from the cabinet to access the ICS3 power supply.

1. Power down the system (refer to System Power-Down in this chapter).

2. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, unlock the two fasteners on both sides of the rear door and tilt the rear door. Proceed to step 3.

   B) If the ICS3 is installed in the peripheral cabinet, remove the rear panel. Note the location of the card cage against the mounting rail. Remove the four screws securing the 16-slot card cage to the mounting rail and withdraw the card cage from the cabinet. Place the card cage on the floor, taking care not to exert undue strain on the power and control cables. Proceed to step 3.

3. Disconnect the following ac cables from the power supply (see Figure 7-25) located in the card cage assembly:

   - Fan tray assembly dc power cable (CBL10153-001) (peripheral bay only)

   - Source ac power cable (CBL10368-001) 60Hz or (CBL10371-001) 50Hz

   - LAC backplane power cable (CBL10139-001)

4. Loosen and remove the two screws securing the power supply to the card cage chassis.

5. Remove the power supply from the card cage chassis.

7.18.5.2 Replacing the ICS3 Power Supply

To replace the ICS3 power supply, follow these steps:

1. Slide the power supply into the ICS3 card cage chassis from the rear (see Figure 7-25).

2. Insert and tighten the two screws (see Figure 7-25) securing the unit to the card cage chassis.

3. Connect the following cables to the power supply (see Figure 7-25):

   - Fan tray assembly dc power cable (CBL10153-001) (peripheral bay only)

   - Source ac power cable (CBL10368-001) 60Hz or (CBL10371-001) 50Hz

   - LAC backplane power cable (CBL10139-001)

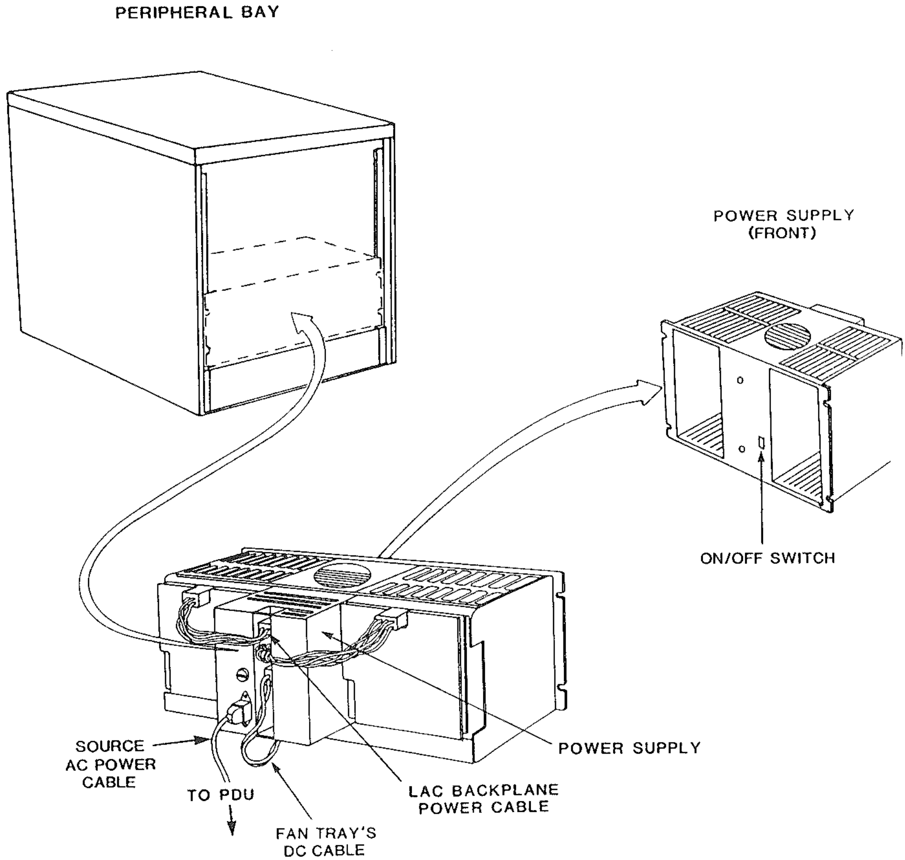


FIGURE 7-25: ICS3 POWER SUPPLY REMOVAL

4. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, return the rear door to its full upright position and lock the two fasteners that secure rear door to the chassis.

   B) If the ICS3 is installed in the peripheral cabinet, slide the 16-slot card cage into the cabinet and secure the card cage to the mounting rail with four screws. Replace the rear panel.

7.18.6 REMOVING AND REPLACING THE ICS3 FUSE

The ICS3 has a fuse that may require replacement. The fuse is located to the rear of the 16-slot card cage's power supply.

7.18.6.1 Removing the ICS3 Power Supply Fuse

To remove the power supply fuse, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, unlock the two fasteners on both sides of the rear door and tilt the rear door. Proceed to step 3.

   B) If the ICS3 is installed in the peripheral cabinet, remove the four screws securing the 16-slot card cage to the cabinet bulkhead and remove the card cage. Proceed to step 3.

3. Turn the fuse holder counter-clockwise until the spring-loaded holder releases (see Figure 7-26 for fuse location).

4. Remove the 5 amp, 250V glass fuse (see Figure 7-26) from the holder.

7.18.6.2 Replacing the ICS3 Power Supply Fuse

To replace the ICS3 16-slot card cage's power supply fuse, follow these steps:

1. Insert the 5 amp, 250V glass fuse (see Figure 7-26) into the plastic fuse holder.

2. Insert the fuse holder into the opening (see Figure 7-26) located to the rear of the 16-slot card cage's power supply.

3. Turn the fuse holder clockwise (see Figure 7-26) until it locks into position.

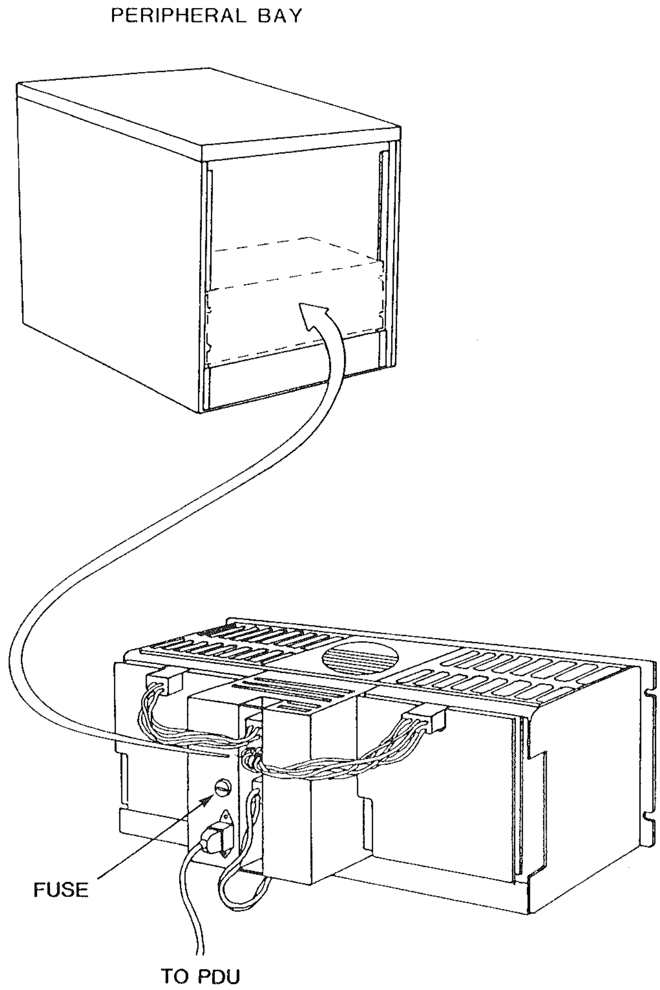


FIGURE 7-26: ICS3 POWER SUPPLY FUSE REMOVAL

4. Select the applicable action:

   A) If the ICS3 is installed in the mainbay, return the rear door to its full upright position and lock the two fasteners that secure rear door to the chassis.

   B) If the ICS3 is installed in the peripheral cabinet, slide the 16-slot card cage into its bulkhead panel opening and secure the card cage in place with four screws.

7.18.7 REMOVING AND REPLACING THE ICS3 FAN TRAY ASSEMBLY

The following subsections provide removal and replacement procedures for the ICS3 fan tray assembly (see Figure 7-27).

NOTE

ICS3 systems mounted in the mainbay are not equipped with a fan tray assembly.

7.18.7.1 Removing the ICS3 Fan Tray Assembly

To remove the fan tray assembly from the 16-slot card cage, follow these steps:

1. Power down the system (refer to System Power-Down in this chapter).

2. Remove the four screws securing the 16-slot card cage to the cabinet bulkhead and remove the card cage.

3. Disconnect the fan tray assembly's dc power cable (CBL10153-001) from the power supply (see Figure 7-27).

4. Remove the four screws (see Figure 7-27) securing the fan tray assembly to the card cage chassis.

5. Pull the tray assembly forward (see Figure 7-27) and remove it from the card cage chassis.

7.18.7.2 Replacing the ICS3 Fan Tray

To replace the fan tray assembly, follow these steps:

1. Slide the fan tray assembly (from the front) into the card cage chassis (see Figure 7-27).

2. Insert and tighten the four screws (see Figure 7-27) securing the fan tray assembly to the card cage chassis.

3. Connect the fan tray assembly's dc power cable (CBL10153-001) to the power supply (see Figure 7-27).

4. Slide the 16-slot card cage into its bulkhead panel opening and secure the card cage in place with four screws.

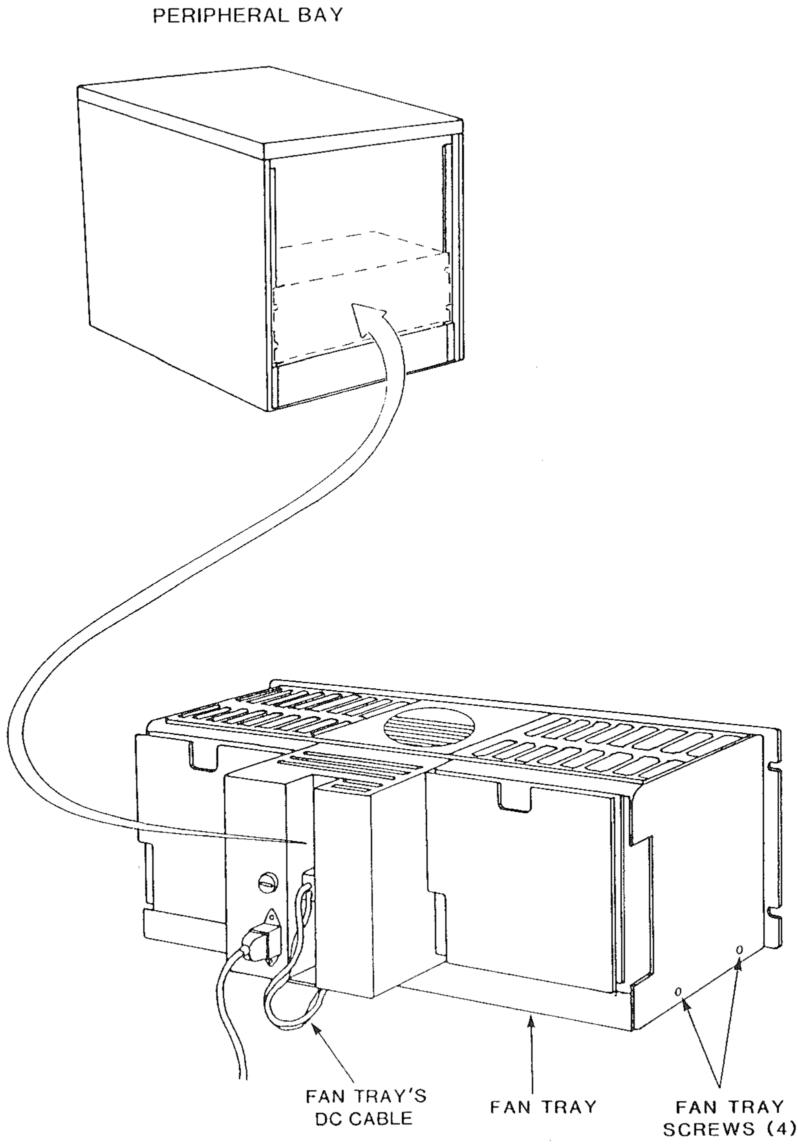


FIGURE 7-27: ICS3 FAN TRAY REMOVAL

7.19 REMOVING AND REPLACING THE MODEL 4587 TAPE DRIVE

Refer to Model 4587 Tape Drive Service Procedures Manual (SPM920) for tape drive removal and replacement procedures.

7.20 REMOVING AND REPLACING THE MODEL 4735 DISK DRIVE (496 MB)

Refer to 496MB Fixed Module Disk Subsystem Service Procedures Manual (SPM470) for disk drive removal and replacement procedures.

7.21 REMOVING AND REPLACING THE MODEL 4835 DISK DRIVE (770 MB)

Refer to 770MB Fixed Storage System Service Procedures Manual (SPM390) for disk drive removal and replacement procedures.

7.22 SYSTEM PART NUMBERS

Table 7-1 lists the part numbers associated with the Model 4050/4150 system. Table 7-2 lists Model 4050/4150 cable part numbers. Use these part numbers when ordering replacement components for the Model 4050/4150 system.

TABLE 7-1: MODEL 4050/4150 PART NUMBERS

DESCRIPTION	PART NUMBER
MODEL 4050 DISKETTES	
Functional Microcode	DSK7084-935
Microdiagnostic 1	DSK7084-936
Microdiagnostic 2	DSK7084-937
MODEL 4150 DISKETTES	
Functional Microcode	DSK7084-928
Microdiagnostic 1	DSK7084-929
Microdiagnostic 2	DSK7084-930
SYSTEM BOARDS	
4050 CPU Board Set	TLA10290-001
CPU CMI Board	TLA10288-001
CPU E Board	TLA10289-001
CPU IS Board	TLA10251-001

TABLE 7-1: MODEL 4050/4150 PART NUMBERS (CONT.)

DESCRIPTION	PART NUMBER
SYSTEM BOARDS (CONT.)	
4150 CPU Board Set	TLA10104-001
CPU CMI Board	TLA10253-001
CPU E Board	TLA10252-001
CPU IS Board	TLA10251-001
Memory, 8MB Array Board	TLA10088-001
VCP-V PCB Assembly	TLA10132-001
SYSTEM UNITS	
5 1/4" Disk Drive	MHD10012-001
Card Cage, 22-Slot	MEC10403-001*
Backplane, 22-Slot (Rev. 15)	MEC10231-001*
ID Board Assembly	ESA6481-913
PROM, Model 4150 ID	PRM10177-001
ID Board Assembly	ESA6481-916
PROM, Model 4050 ID	PRM10273-001
PDU Assembly 120/208Vac (Main Cabinet)	ESA10233-001
PDU Assembly 240Vac (Main Cabinet)	ESA10233-002
PDU Assembly 120Vac (Peripheral Bay)	ESA10296-001
PDU Assembly 240Vac (Peripheral Bay)	ESA10296-002
Status Panel Assembly	ESA10239-001
TLA10113 130 A 50 Hz/60 Hz Power Supply	TLA10113-001
20 A, 3AG Slow Blow Fuse	FUS0224-036
Fuse Holder	FUS8090-101
Battery Backup Unit, 120Vac	TLA10069-001
Battery Backup Unit, 240Vac	TLA10069-002
Battery Backup Unit Shield	MEC10495-001*

TABLE 7-1: MODEL 4050/4150 PART NUMBERS (CONT.)

DESCRIPTION	PART NUMBER
SYSTEM UNITS (CONT.)	
Power Shunt Board	ESA10252-001*
Blower Assembly	BWR10005-001
Sensor, Airflow	SWT10019-004
Switch, Blower Bypass	SWT10029-001
Filter, Air	HDW10078-001
CABINET PANELS & DOORS	
Front	MEC10385-001*
Right Side	MEC10387-001*
Left Side	MEC10388-001*
Top	MEC10386-001*
Side Rear Trim (2)	MEC10384-001*
Lower Rear Trim	MEC10382-001*
Lower Front Trim	MEC10383-001*
Rear Door Assembly	MSA10112-001*
COMMUNICATIONS DEVICES	
ICS3 Assembly	MSA10010-003
Exhaust Tray (ICS3 mainbay)	MEC10505-001*
Fan Tray (ICS3 peripheral bay)	ESA10299-001

* Not stocked by Logistics. These items require a special order.

TABLE 7-2: MODEL 4050/4150 CABLE PART NUMBERS

DESCRIPTION	FRU NUMBER
AC Power Cable, Mainbay (Domestic/208V)	CBL10898-001
AC Power Cable, Mainbay (Intl./240V)	CBL10598-001
AC Power Cable, Peripheral (Domestic/120V)	CBL10864-001
AC Power Cable, Peripheral (Intl./240V)	CBL10600-001
PDU to I/O 7778 Power Supply (Domestic)	CBL10648-001
PDU to CPU 7778 Power Supply (Domestic)	CBL10648-003
PDU to I/O 7778 Power Supply (International)	CBL10648-002
PDU to CPU 7778 Power Supply (International)	CBL10648-004
PDU to Battery Backup Unit (Domestic)	CBL10498-001
PDU to Battery Backup Unit (International)	CBL10498-002
Console Panel Assembly Cable	CBL10449-001*
Status Panel Harness	CBL10490-001
VCP-V/PDU/Status Panel/BBU	CBL10486-001
Air Flow Sensor to VCP-V	CBL10481-001
Air Flow Sensor to Connector	CBL10616-001
Floppy Drive to VCP-V	CBL10450-001
Floppy Drive Power	CBL10491-001
Disk Drive Power (120V)	CBL10662-001
Disk Drive Power (240V)	CBL10662-002
Keylock Switch Cable	CBL10529-001
PDU Sense	CBL10465-001
PDU Control Out (Mainbay)	CBL10464-001
PDU Control In (Mainbay)	CBL10464-001
PDU Contr. Out (Peripheral)	CBL10469-002
Modem Telephone Jack Cable	CBL10172-001

* Not stocked by Logistics. These items require a special order.

APPENDIX A
QUICK REFERENCE

The Quick Reference Guide provides system-specific information in table format. The information is extracted from procedures within the service manual and condensed for easy access. The following sections include:

- Memory Configurations
- Software/Hardware Dependencies
- I/O Configuration (Backplane Priority)
- Device Addresses
- Board Switch Settings
- VCP-V Diagnostic Processor Cabling
- Sample of MAKE Command
- Sample CONFIG File
- Sample PRIMOS.COMI File
- Control Panel Commands Sumary
- Booting Information
- Halt Locations
- Status Words
- Memory Decode Information
- Major Cabling Diagram

1.1 MEMORY CONFIGURATIONS

TABLE A-1: MEMORY CONFIGURATIONS FOR MODELS 4050 & 4150 SYSTEMS

SYSTEM MODEL	MEMORY MODEL #	MINIMUM MEMORY	MAXIMUM MEMORY	AVAILABLE SLOTS
4050	MMW3-8MB	8	32	4
4150	MMW3-8MB	8	32	4

1.2 SOFTWARE/HARDWARE DEPENDENCIES

TABLE A-2: MODEL 4050/4150 SOFTWARE REQUIREMENTS

MODEL	MINIMUM PRIMOS REV.
4050	20.2.6 or 21.0.2S
4150	20.2.5 or 21.0.2

NOTE

Both the Model 4050 and Model 4150 support all currently-marketed 50 Series controllers and peripheral devices. All system boards must be at their latest revision level. Minimum board revision requirements are listed in Table A-3.

TABLE A-3: MODEL 4050/4150 HARDWARE REQUIREMENTS

BOARD NAME	MODEL NUMBER	PART NUMBER	MINIMUM REVISION
IDC1	6580	7LA10019-001	R
MSTC	2382-003	7LA10234-001	R
MPC4	7010T	SPL91521-91	H
8MB MEMORY	MMW3-8MB	7LA10088-001	C
STSC	2301	2301-901	AA
ASYNC LAC	CLAC304	ESA10063-001	C
BMTC	2023	2023-901	N

1.3 I/O CONFIGURATION

TABLE A-4: MODELS 4050 & 4150 I/O CONTROLLER PRIORITY: BASIC ORDER

PRIORITY	I/O CONTROLLER
Lowest	Synchronous
●	Asynchronous
●	Disk
Highest (Rightmost slot)	Tape (see Note)

NOTE

Install the magnetic tape controller (MSTC) to the right of disk controllers.

1.4 DEVICE ADDRESSES

TABLE A-5: DEVICE ADDRESSES

DEVICE ADDRESS (OCTAL)	CONTROLLER MODEL	DESCRIPTION
00	----	-----
01	3000	Paper Tape Reader
02	3000	Paper Tape Punch
03	31XX/2294	URC #1 (Line Printer, Card Reader)
04	*	System Terminal
05	31XX/2294	URC #2 (Line Printer, Card Reader)
06	7000	IPC (Interprocessor Communications Board)
07	7040	PRIMENET Node Controller #1
10	2034/2036	ICS2 #1 or ICS1 (Intelligent Communication Subsystem) #3
11	2034/2036	ICS2 #2 or ICS1 #4
12	4300	Floppy Disk
13	4020/2295/ 2301/2081/ 2023/2270/ 2047/2382	Magnetic Tape Controller #2
14	4020/2295 2301/2081/ 2023/2270/ 2047/2382	Magnetic Tape Controller #1
15	5XXX/2036	AMLC/QAMLC #5 or ICS1 #8
16	5XXX/2036	AMLC/QAMLC #6 or ICS1 #7
17	5XXX/2036	AMLC/QAMLC #7 or ICS1 #6
20	*	Processor I/O Select (PIOS) Board SOC (System Option Controller)
21	4002	Disk Option B'
22	4005/6580/6590	Disk Controller #3

*Used by the VCP-V Diagnostic Processor

TABLE A-5: DEVICE ADDRESSES (CONT.)

DEVICE ADDRESS (OCTAL)	CONTROLLER MODEL	DESCRIPTION
23	4005/6580/6590	Disk Controller #4
24	6590	Disk Controller #5
25	6590	Disk Controller #6
26	4005/6580/6590	Disk Controller #1
27	4005/6580/6590	Disk Controller #2
30	3007	Buffered Parallel I/O Channel #1
31	3025	Buffered Parallel I/O Channel #2
32	5XXX/2036	AMLC/QAMLC #8 or ICS1 #5
33	3009/3008	VERSATEC/GOULD Printer Plotter
34	3009/3008	VERSATEC/GOULD Printer Plotter
35	5XXX/2036	AMLC/QAMLC #4 or ICS1
36	2034/2036	ICS1 #1 or ICS2 #3
37	2034/2036	ICS1 #2 or ICS2 #4
40	6000/6005	PRIMAD (AIS, Analog Input System)
41	6020	Digital Input #1 (DIS)
42	6020	Digital Input #2
43	6040	Digital Output #1 (DOS)
44	6040	Digital Output #2
45	6590	Disk Controller # 7
46	6590	Disk Controller # 8
47	7040	PRIMENET Node Controller #2
50	5300	HSSMLC #1 (High Speed Synchronous Multiline Controller) or MDLC
51	5300	HSSMLC #2 or MDLC
52	5XXX/2036	AMLC/QAMLC #3 or ICS1
53	5XXX	AMLC/QAMLC #2
54	5XXX	AMLC/QAMLC #1
55	5400	Multiple Autocall
56	5200	SMLC (Synchronous Multiline Controller)
	LHC300	LAN Controller
57	_____	_______________
60	7000	General Purpose Interface Board
61	7000	General Purpose Interface Board
62	7000	General Purpose Interface Board
63	7000	General Purpose Interface Board
64	7000	General Purpose Interface Board
65	7000	General Purpose Interface Board
66	7000	General Purpose Interface Board
67	7000	General Purpose Interface Board
70	----	Reserved for Specials
71	----	Reserved for Specials
72	----	Reserved for Specials
73	----	Reserved for Specials
74	----	Reserved for Specials
75	----	Reserved for Controllers Using T$GPPI
76	----	Reserved for Controllers Using T$GPPI
77	----	I/O Bus Tester

*Used by the VCP-V Diagnostic Processor

1.5 BOARD SWITCH SETTINGS

NOTE: DOWN = OFF UP = ON

TABLE A-6: DIAGNOSTIC PROCESSOR (VCP-V) OPTION SWITCH A SETTINGS

SWITCH SETTINGS			FUNCTION
S1	S2	S3	LOCAL1 SYSTEM CONSOLE BAUD RATE
OFF	OFF	OFF	300 BAUD
ON	OFF	OFF	600 BAUD
OFF	ON	OFF	1200 BAUD
ON	ON	OFF	2400 BAUD
OFF	OFF	ON	4800 BAUD
ON	OFF	ON	9600 BAUD
OFF	ON	ON	19200 BAUD (Not Supported)
ON	ON	ON	38400 BAUD
S4	S5		REMOTE SYSTEM CONSOLE BAUD RATE
OFF	OFF		300 BAUD
ON	OFF		1200 BAUD
OFF	ON		4800 BAUD (Not Supported)
ON	ON		9600 BAUD (Not Supported)
S6			BOOT DEVICE
ON			Attempt to use next logical device if current device fails during power up.
OFF			Use only the current device
S7			SELF-VERIFICATION EXECUTION
OFF			Run self-verification once
ON			Loop on failing test
S8			VCP-V CODE BOOT DEVICE
ON			Enable Diagnostic Tools Mode (In-house only)
OFF			Boot VCP-V code from Floppy Drive

TABLE A-7: VCP-V OPTION SWITCH B SETTINGS

SWITCH SETTINGS			FUNCTION
S9	S10	S11	LOCAL2 SYSTEM CONSOLE BAUD RATE
OFF	OFF	OFF	300 BAUD
ON	OFF	OFF	600 BAUD
OFF	ON	OFF	1200 BAUD
ON	ON	OFF	2400 BAUD
OFF	OFF	ON	4800 BAUD
ON	OFF	ON	9600 BAUD
OFF	ON	ON	19200 BAUD (Not Supported)
ON	ON	ON	38400 BAUD
S12			
OFF			Normal Operation
ON			If S8 is on, Virtual Floppy Automatically used.
S13			INTERNAL/EXTERNAL MODEM
OFF			External modem enabled
ON			Internal modem enabled
S14	S15	S16	USER MODE PORT BAUD RATE
OFF	OFF	OFF	300 BAUD
ON	OFF	OFF	600 BAUD
OFF	ON	OFF	1200 BAUD
ON	ON	OFF	2400 BAUD
OFF	OFF	ON	4800 BAUD
ON	OFF	ON	9600 BAUD
OFF	ON	ON	19200 BAUD (Not Supported)
ON	ON	ON	38400 BAUD

TABLE A-7A: VCP-V SWITCH OPTION 3 SETTINGS*

S17	
ON	Battery is disconnected from Real Time Clock Circuit
OFF	Battery is connected to Real Time Clock Circuit
S18 & S19	
ON	Disconnects 2nd PDA port from the Backplane
OFF	Connects 2nd PDA Port to the Backplane

*Switch 3 is unlabeled on the board.

TABLE A-7A: VCP-V OPTION SWITCH 3 SETTINGS (CONT.)

SWITCH SETTINGS	FUNCTION
S20 S21	
ON ON	Disconnects 1st PDA Port from the Backplane Connects 1st PDA Port to the Backplane
S22	
ON OFF	Does not supply Modem with -5 volts (used with a 1760) Supplies Modem with -5 volts (used with a 1770)
S23	Not Used
S24	Not Used

*Switch 3 is unlabeled on the board.

NOTE

The VCP-V is shipped to the customer site with the LOCAL1 and LOCAL2 ports set at 300 baud. Reset these baud rates to 9600 during system installation.

1.6 VCP-V DIAGNOSTIC PROCESSOR CONNECTORS

TABLE A-8: VCP-V EDGE CONNECTORS AND CABLES

CONNECTOR	CONNECTS VCP-V TO:	CABLE NUMBER
J01	Air Flow Switch	CBL10481-001
J03	ID Board/PROM	N/A
J05	Terminals/UPS/MBBU	CBL10449-001
J06	Floppy Disk Assembly	CBL10450-001
J07	Status Panel/PDU	CBL10486-001
J08	Modem Phone Jack	CBL10172-001

1.7 SAMPLE MAKE COMMAND

This section presents recommended MAKE options when installing a Model 4050/4150 System with a Model 4735 or Model 4784 disk drive.

The format for the command with recommended options is:

```
-DISK 1060 -PART COMDEV -DT MODEL_XXXX -NO_INIT -NEWDSK
```

TABLE A-9: RECOMMENDED MAKE COMMAND OPTIONS

OPTION	DESCRIPTION
-DISK_TYPE, (-DT disk-type)	Specifies what kind of disk.
-NO_INIT	Do not initialize the file system part of the disk. Unless this is specified, the records are initialized.
-BADSPOT_LEVEL, (-BADLEV bad-spot_checking_level)	Checking level can be from 0 to 4, inclusive. If level 0 is specified, no checking is done. The default for the Model 4735 and 4845 drives is 0.
-NEW_DISK, -NEWDSK	Suppresses the attempt to read the old badspot file. This command is necessary for a new disk.

TABLE A-10: MODELS 4735 and 4784 DISK DRIVES DESCRIPTION

MODEL #	DESCRIPTION	NUMBER DATA HEADS	MAKE COMMAND OPTIONS
Model 4735	496 Mb Fixed Media	24	-DT MODEL_4735
Model 4835	770 Mb Fixed Media	23	-DT MODEL_4845

NOTE

Use the -NO_INIT option, not the -FORMAT option, to MAKE the disk quickly.

1.8 SAMPLE CONFIG FILE

```
INPUT
ASRATE 3410          /* Set console rate to 9600 baud.
TYPOUT NO            /* Do not echo on screen.
ERASE ^210           /* Set erase character to BACKSPACE.
COMDEV 4060          /*
PAGDEV 100461        /*
NTUSR 11             /* Set number of terminal users + 1
NPUSR 5              /* Set number of phantom users.
MAXPAG 10000         /* For 32 Mb of memory (or remove directive).
LOUTQM 74            /* About one hour.
LOGMSG NO            /* Don't print user login/logout messages at
                     /* system console.
GO                   /* This must be last line of CONFIG file.
```

1.9 SAMPLE PRIMOS.COMI FILE

```
CONFIG -DATA CONFIG
AMLC TTY 0 2413              /*First terminal line
AMLC TTY 1 2413
AMLC TTY 2 2413
AMLC TTY 3 2413
AMLC TTY 4 2413
AMLC TTY 5 2413
AMLC TTY 6 2413
AMLC TTY 7 2413             /*Last terminal line
OPR1                           /* SHARE REQUIRES OPR 1
SHARE SYSTEM>ED2000 2000       /* SHARE the editor  -  ED
/*
SHARE SYSTEM>MP2122 2122 700        /* SHARE MIDASPLUS LIBRARY
SHARE SYSTEM>MP2123 2123 700
SHARE 2124 700
SHARE 2125 700
R SYSTEM>MP4000 1/2
SHARE 2122
R SYSTEM>IMIDASPLUS SYSTEM>MPLUS.CONFIG
/*
SHARE SYSTEM>F2021A 2021 700          /* SHARE FORMS LIBRARY
SHARE SYSTEM>F2021B 2021 700
R SYSTEM>F4000 1/4
SHARE 2021
SHARE SYSTEM>S$2167 2167              /* SHARE SPOOL LIBRARIES
R SYSTEM>S$4000 1/12
/* MAGLIB is a shared library as of Rev 19.2
SHARE SYSTEM>ML2222 2222              /* SHARE MAGLIB
R SYSTEM>ML4000 1/16
OPR 0
CO -END
PROP PRO -START                   /* START SPOOLER PHANTOM
CO SYSTEM>BASICV.SHARE.COMI 7     /* SHARE BASICV COMPILER
CO SYSTEM>COBOL.SHARE.COMI 7      /* SHARE COBOL COMPILER & LIBRARY
CO SYSTEM>ROAM.SHARE.COMI 7       /* SHARE ROAM before DBMS
CO SYSTEM>DBMS.SHARE.COMI 7       /* SHARE DBMS
CO SYSTEM>DPTX.SHARE.COMI 7       /* SHARE DPTX
CO SYSTEM>EMACS.SHARE.COMI 7      /* SHARE EMACS
CO SYSTEM>FED.SHARE.COMI 7        /* SHARE FED
CO SYSTEM>FORMS.SHARE.COMI 7      /* SHARE FORMS LIBRARY
CO SYSTEM>FTS.SHARE.COMI 7        /* SHARE FTS
CO SYSTEM>MIDASPLUS.SHARE.COMI 7    /* SHARE MIDASPLUS LIBRARY
CO SYSTEM>POWERPLUS.SHARE.COMI 7    /* SHARE POWERPLUS
CO SYSTEM>VRPG.SHARE.COMI 7         /* SHARE VRPG
CO SYSTEM>DISCOVER_DBMS.SHARE.COMI 7     /* SHARE DISCOVER_DBMS
CO SYSTEM>DISCOVER_PRISAM.SHARE.COMI 7  /* SHARE DISCOVER_PRISAM
CO SYSTEM>CC.SHARE.COMI 7               /* SHARE CC
CO SYSTEM>CBL.SHARE.COMI 7              /* SHARE CBL
CO SYSTEM>DBG.SHARE.COMI 7              /* SHARE DBG
CO SYSTEM>PRISAM.SHARE.COMI 7           /* SHARE PRISAM
CO SYSTEM>DSM.SHARE.COMI.7
CLOSE 7
/* SET THE DATE AND TIME **********
/* TYPE MAXUSR TO ALLOW USERS TO LOG IN
CO -END
```

1.10 SUMMARY OF CONTROL PANEL COMMANDS

Table A-11 provides a summary of all Control Panel commands. See Chapter 3 for a description of each command.

TABLE A-11: SUMMARY OF CONTROL PANEL COMMANDS

COMMANDS	
*:O,:H,:B,:D,:A,:0,:1,:2,:3,:4	Access <address> [:0 or :1]
Access <register> [:0 or :1]	BOOT [SS] [DS]
BOOTP [SS]	BOOTT [SS]
BREAKON	BREAKOFF
*CONFIG <table>	Copy <start> <end> <destination>
DARE	DIRectory [:0...:4]
DISABLE <:1 or :2 or :3>	DISPLAY <address> [:0 or :1]
DISPLAYC <address> [:0 or :1]	Dump <start> <end> [:0 or :1]
Dump <register> [:0 or :1]	ENABLE <:1 or :2 or :3> <-NOPASS>
FETCH	Fill <start> <end> <data> [:0 or :1]
*FREQHIGH	*FREQNORM
HALT	HELP [:0...:4]
HISTORY	*IOSYSOFF
*IOSYSON	LDNET [filename]
Lights	LightsC
listREV	*LMEMTST
LOADM <filename> [:0 or :1]	LOADTM <filename> [SS]
MARGIN <:0,:N,:H,:L> [0...8]	MODE <UNI or DUAL or DEGRADED> <A,B>
MO ABS	MO BRIEF
MO FULL	MO MAP
MO PDA [:0 or :1]	MO RFABS
MO RFCRS	MO RFH
MO RFL	MO ST
*MO TEST	MO USER
OVERRIDE [:0 or :1]	*PARTIAL_TAPdump <drive>
*PASSWORD	PRIVilege <:1,:2,:3>
RCP [address] [:0 or :1]	Run [address] [:0 or :1]
RUND <filename>	RUNDC <filename>
RUNTM <filename> [SS]	SCOPE
SD <data>	SEtime -<mmddyy> -<hhnnw> [-D]
SS <SS>	SSTEP [number]
STAT [-CLEAR]	STEPU <address>
STOP	STORE <data>
Sysclr [address]	*SYSON [:0 or :1]
*SYSOFF [address] [:0 or :1]	SYSOUT BUFF
SYSOUT IGN	SYSOUT INT
TAPEdump <drive>	TRACE [number]
*TSENS [1...9] [C]	VERIFYM <filename> [:0 or :1]
VFNET [filename]	VIRY
VPSD	*VSENS [1...8] [C]
WARMstart	

*New Control Panel command

1.11 BOOTING INFORMATION

1.11.1 SENSE SWITCH BOOT OPTIONS

The following boot options are defined at Rev. 20.2.3 of PRIMOS. Note that the value YYY represents the Boot Device Option, defined in detail in the next subsection.

'100YYY - Prompts the user for the values of COMDEV, PAGDEV, and NTUSR. Do not initialize the communications controllers (QAMLC, ICS1, ICS2, ICS3, SMLC, or PNC). Do not read the user's PRIMOS.COMI or CONFIG file. If this switch is not set, PRIMOS assumes that it is to use PRIMOS.COMI and CONFIG, and proceeds as usual.

'010YYY - Assumes that the program being booted is on the same device that BOOT was read from. If not set, BOOT prompts for 'Physical DEVICE=' for entry of a valid disk partition's Physical DEVice (PDEV) number, or a magtape unit in the form of MT0, MT1, MT2, ... or MT7.

'004YYY - AutoBoots PRIMOS. Assumes the pathname of the PRIMOS runfile is the same as used in the last successful boot of PRIMOS from this device. If the UFD MFD>BOOT_RUN_FILE_TREENAME does not exist, or does not contain a valid treename, it assumes PRIRUN>PRIMOS.SAVE. If PRIRUN>PRIMOS.SAVE does not exist, or if this switch is not set, BOOT prompts for 'RUN FILE TREENAME= '.

If this sense switch is not set the user is prompted for the pathname of the file to be booted. Examples are DOS>DOS.SAVE, CMDNC0>MAKE.SAVE, CMDNC0>COPY_DISK.SAVE, and PRIRUN_19>PRIMOS. Entering a carriage return in response to the prompt instructs BOOT to use the default treename, PRIRUN>PRIMOS.SAVE.

'002YYY - Halts immediately after loading the program to be booted, but before starting program execution, to allow the user to patch locations in memory or set sense switches. To execute the program depress the START switch (for Control Panel systems) or enter RUN from VCP mode. Do not SYSCLR before executing the program! This option is useful when running T&Ms. If this option is not set, the program is loaded then executed immediately.

'001YYY - Indicates do not run CPBOOT, or this machine, in Machine Check Mode. This option is useful when troubleshooting a system that is halting due to machine checks. If not set, the system runs with Machine Check Mode turned on.

'000040 - Halts immediately to allow the user to patch the system console baud rate to something other than the default of 300 baud. This option is valid only when booting from Magtape! Other baud rates are selected by patching locations '1004 through '1006.

To continue the boot, press the START switch (on Control Panel system), or enter RUN from VCP mode. Before continuing with the boot, you must set the sense switches back to their original values at the start of the boot.

1.11.2 BOOT DEVICES

The Rev. 20.2.3 BOOT program allows PRIMOS and standalone programs (MAKE.SAVE, COPY_DISK.SAVE, etc.) to boot from disk drives attached to controller addresses '22 and '23, and from Magtape units other than MT0. Table A-12 lists the boot devices supported at Rev. 20.2.3 of PRIMOS. The value XXX represents the Sense Switch Boot Options described in the previous section.

TABLE A-12: SENSE SWITCH BOOT DEVICE OPTIONS

OPTION	DEVICE
XXX114	Disk drive 0, disk controller 0 (dev addr '26)
XXX314	Disk drive 1, disk controller 0 (dev addr '26)
XXX514	Disk drive 2, disk controller 0 (dev addr '26)
XXX714	Disk drive 3, disk controller 0 (dev addr '26)
XXX134	Disk drive 0, disk controller 1 (dev addr '27)
XXX334	Disk drive 1, disk controller 1 (dev addr '27)
XXX534	Disk drive 2, disk controller 1 (dev addr '27)
XXX734	Disk drive 3, disk controller 1 (dev addr '27)
XXX154	Disk drive 0, disk controller 2 (dev addr '22)
XXX354	Disk drive 1, disk controller 2 (dev addr '22)
XXX554	Disk drive 2, disk controller 2 (dev addr '22)
XXX754	Disk drive 3, disk controller 2 (dev addr '22)
XXX174	Disk drive 0, disk controller 3 (dev addr '23)
XXX374	Disk drive 1, disk controller 3 (dev addr '23)
XXX574	Disk drive 2, disk controller 3 (dev addr '23)
XXX774	Disk drive 3, disk controller 3 (dev addr '23)
XXX005	Tape drive 0, tape controller 0 (dev addr '14)
XXX205	Tape drive 1, tape controller 0 (dev addr '14)
XXX405	Tape drive 2, tape controller 0 (dev addr '14)
XXX605	Tape drive 3, tape controller 0 (dev addr '14)
XXX025	Tape drive 0, tape controller 1 (dev addr '13)
XXX225	Tape drive 1, tape controller 1 (dev addr '13)
XXX425	Tape drive 2, tape controller 1 (dev addr '13)
XXX625	Tape drive 3, tape controller 1 (dev addr '13)

1.11.3 DATA SWITCH BOOT OPTIONS

The following data switch options are defined at Rev. 20.2.3 of PRIMOS.

'040000 - Forces the system to halt after an error has been displayed with Force Error Display set (Data Switch '004000).

'020000 - Inhibits PIO time outs.

'010000 - Bypasses the CPBOOT diagnostic routines.

'004000 - Forces error display.

'002000 - Displays informative messages while executing CPBOOT.

'000002 - Boots from a Pre-REV20 tape.

1.11.4 BOOT OPTION WORDS

TABLE A-13: COMMONLY-USED BOOT OPTION WORDS

BOOT VALUE	CONTROLLER ADDRESS	DRIVE UNIT	PARTITION WITH BOOT FILE	PRIMOS RUNFILE
14114	'26	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
10114	'26	0	First	Prompts for filename
114	'26	0	Prompts for pdev	Prompts for filename
114114	'26	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE Do not use configuration and startup files.
100114	'26	0	Prompts for pdev	Prompts for filename. Do not use configuration and startup files.
14314	'26	1	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14514	'26	2	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14134	'27	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14154	'22	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
14174	'23	0	First	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE
10005	'14	MTO	-	In BOOT_RUN_FILE_TREENAME or use PRIRUN>PRIMOS.SAVE

1.12 HALT LOCATIONS

TABLE A-14: PRIMOS SYSTEM HALTS

HALT	LOCATION	DEFINITION
AMLCI_	*	Spurious AMLC interrupt.
BOOT0_	*	SHUTDN ALL stops here.**
DKSEM_	*	Disk semaphore not free when it should be.
DSTWO_	*	Illegal recursive call to disk I/O.
DSKNW_	*	No I/O windows for disk I/O.
IFLTB_	*	Bad fault in interrupt process.
INTRT_	*	Too many returns in interrupt process.**
IPAGF_	*	Page fault in interrupt process.**
MCHK_	4/305	Machine check.
MEMH2_	*	Halt after auto mapping out page.
MEMPA_	4/276	Memory parity halt (non-ECCC).
MMOD_	4/315	Missing memory check.
PAGFB_	*	Illegal block of page faults.**
PAGFI_	*	Illegal inhibit of page faults.**
PAGES_	*	Error handling fault on stack.**
PWRFL_	4/204	Power failure.
REFLO_	*	Flex, UII or PSU when not allowed.
RCMF0_	*	Restrict mode fault when not allowed.
SVCF4_	*	SVC when not allowed.
XRNG0_	*	Illegal ring number in supervisor.

* Those halt locations marked with an asterisk (*) change between revisions of PRIMOS. Halt locations for the revision of PRIMOS being used on your system can be found in the RINGO map (PRIRUN>RINGO.MAP) for that revision. Use ED to examine the map.

**Slow halts as of REV. 20.2

1.13 STATUS WORDS

TABLE A-15: FORMAT OF DSWPARITY REGISTER: HIGH SIDE

BITS	NAME	DESCRIPTION
1	I/O Parity	If 1, the CMI reported an I/O parity error. Sets bits 2 to 5 to represent BPD or BD errors: Bit 2: BDH, left byte Bit 3: BDH, right byte Bit 4: BDL, left byte Bit 5: BDL, right byte Bit 6: Not used Bit 7: Not used
8 to 10	RCC Parity Error Code	If DSWSTAT bit 2 is set to 1, these three bits contain the RCC parity error code: ERROR CODES 000: NO ERROR 001: FRCCPE1 010: FRCCPE2 011: FRCCPE3 100: FRCCPE4 101: FRCCPE5 110: FRCCPE6 111: FRCCPE7
11	Not Used	
12 to 13	RCC/Decode Parity Error	Describes CMI unit parity error status: ERROR CODES 00: no error 01: FRCCPE8 10: DNETPE1 11: DNETPE2
14 to 16	E Unit parity Error Code	Describes the E unit parity error status: ERROR CODES 000: no error 001: BBH left parity error 010: BBH right parity error 011: BBL left parity error 100: BBL right parity error 101: BAH parity error 110: BAL parity error 111: BAE parity error

TABLE A-16: FORMAT OF DSWPARITY REGISTER: LOW SIDE

BITS	NAME	DESCRIPTION
1	Not Used	
2	Memory Address Shift Control	Specifies the address size of a slot in the memory backplane: 0: 8-megabyte slot decode 1: 16-megabyte slot decode
3	Memory Array	Memory array number 1 reported error
4	Memory Array	Memory array number 2 reported error
5	Memory Array	Memory array number 3 reported error
6	Memory Array	Memory array number 4 reported error
7	Not Used	
8	Not Used	
9	Not Used	
10	Not Used	
11	Not Used	
12	Not Used	
13	Parity Error	CMI reported a write buffer data high left parity error
14	Parity Error	CMI reported a write buffer data high right parity error
15	Parity Error	CMI reported a write buffer data low left parity error
16	Parity Error	CMI reported a write buffer data low right parity error

TABLE A-17: FORMAT OF DSWPARITY2 REGISTER: HIGH SIDE

BITS	NAME	DESCRIPTION
1 to 4	IS Unit Reports Memory Errors	A 1 in any of these bits specifies the error reported by the IS unit: Bit 1: BDH left parity error Bit 2: BDH right parity error Bit 3: BDL left parity error Bit 4: BDL right parity error
5	IS reported a Base register file parity error, high	
6	IS reported a Base register file parity error, low	
7	IS reported a Index register file parity error	
8 to 9	Not Used	
10	Branch Cache Recoverable Error	If 1, the microcode reported a branch cache recoverable error.
11 to 16	IS Unit Reports Cache parity Errors	A 1 in any of these bits specifies the cache parity error reported by the IS unit: Bit 11: Cache data parity error on Element B even data low byte Bit 12: Cache data parity error on Element B odd data low byte Bit 13: Cache data parity error on Element A even data low byte Bit 14: Cache data parity error on Element A odd data low byte Bit 15: Cache index parity error on Element B low byte Bit 16: Cache index parity error on Element B high byte

TABLE A-18: FORMAT OF DSWPARITY2 REGISTER: LOW SIDE

BITS	NAME	DESCRIPTION
1 to 16	IS Unit Reports Cache or STLB Errors	A 1 in any of these bits specifies the cache or STLB parity error reported by the IS unit: Bit 1: Cache data parity error on Element A even data high byte Bit 2: Cache data parity error on Element A odd data high byte Bit 3: Cache data parity error on Element B even data high byte Bit 4: Cache data parity error on Element B odd data high byte Bit 5: Cache index parity error on Element A high byte Bit 6: Cache index parity error on Element A low byte Bit 7: STLB parity error on Element B physical address low byte Bit 8: STLB parity error on Element A physical address low byte Bit 9: STLB parity error on Element B access bits Bit 10: STLB parity error on Element B process ID Bit 11: STLB parity error on Element B virtual address tag Bit 12: STLB parity error on Element A physical address high byte Bit 13: STLB parity error on Element B physical address high byte Bit 14: STLB parity error on Element A access bits Bit 15: STLB parity error on Element A process ID Bit 16: STLB parity error on Element A virtual address tag

TABLE A-19: FORMAT OF DSWSTAT REGISTER: HIGH SIDE

BITS	NAME	DESCRIPTION
1	Check Immediate	If 1, the check was taken immediately.
2	Machine Check	If 1, a machine check occurred.
3	Memory Parity	If 1, a memory parity error occurred.
4	Missing Memory Module	If 1, a missing memory module caused the check.
5	E Unit	If 1, the E unit reported a parity error.
6	IS Unit	If 1, the IS unit reported a parity error.
7	CMI Unit	If 1, the control store, memory controller I/O unit reported a parity error.
8	Not Used	
9	ECCU	If bits 3 and 9 are both 1, the memory ECC error was uncorrectable.
10	ECCC	If bits 3 and 10 are both 1, the memory ECC error was correctable.
11	Not Used	
12	RCM Parity	If 1, an RCM parity error was detected by the control store board.
13 to 14	RPBU	Specifies the RP backup count at the time of the error.
15	DMx Operation	If 1, a DMx transfer was in progress when the error occurred.
16	I/O Operation	If 1, an I/O operation was in progress when the error occurred.

TABLE A-20: FORMAT OF DSWSTAT REGISTER: LOW SIDE

BITS	NAME	DESCRIPTION
1 to 7	ECC Syndrome Bits	If a correctable memory parity error occurred, it is encoded in these bits.
8	Memory Module Number	If a memory error occurred, this bit identifies the interleaved memory module with the error (bit 15 of address).
9	RMA Invalid	If 1, the contents of DSWRMA are invalid.
10	Recoverable Parity Error	If 1, a recoverable parity error occurred in the cache, STLB, or branch cache.
11	Hard Error	If bit 10 is 1 and this bit is also 1, a recoverable hard parity error occurred. There is a permanent error in hardware.
12	Not used	
13	Internal Error	If 1, the microcode detected an internal error. DSWRMA has a code that indicates the failing microcode algorithm.
14	Not Used	
15	Not Used	
16	Not Used	

1.14 MEMORY DECODE INFORMATION

TABLE A-21: MMW3 BIT IN ERROR DECODE TABLE

DSWSTATL MSBs	BIT IN ERROR
0001010	1
0001111	2
0010010	3
0010100	4
0010111	5
0011000	6
0011011	7
0011101	8
0100010	25
0100100	26
0100111	27
0101000	28
0101011	29
0101101	30
0110000	32
0110101	31
0111111	CB0
1001011	17
1001110	18
1010011	19
1010101	20
1010110	21
1011001	22
1011010	23
1011100	24
1011111	CB1
1100011	9
1100101	10
1100110	11
1101001	12
1101010	13
1101100	14
1101111	CB2
1110001	16
1110100	15
1110111	CB3
1111011	CB4
1111101	CB5
1111110	CB6
1111111	No Error

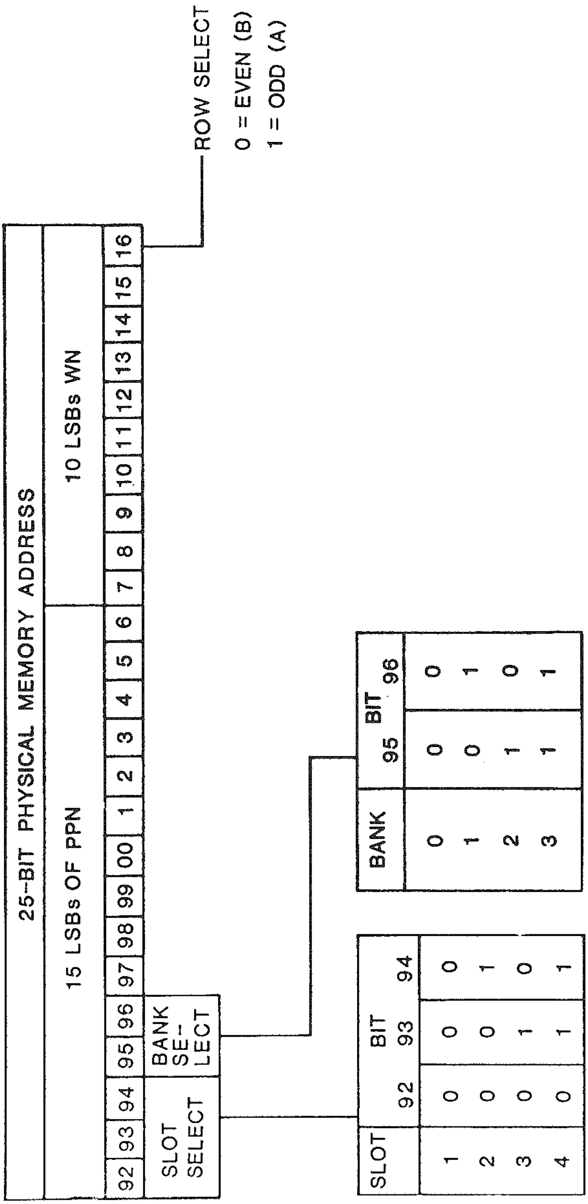


FIGURE A-1: MMW3 DECODE CHART

HANDLE END OF BOARD

LEFT SIDE OF BOARD

A ODD
B EVEN

	A	B	A	B	A	B	A	B	A	B	A	B
BANK 3	32	32	29	29	26	26	23	23	20	20	17	17
	31	31	28	28	25	25	22	22	19	19	16	16
	30	30	27	27	24	24	21	21	18	18	15	15
BANK 2	30	30	27	27	24	24	21	21	18	18	15	15
	31	31	28	28	25	25	22	22	19	19	16	16
	32	32	29	29	26	26	23	23	20	20	17	17
BANK 1	32	32	29	29	26	26	23	23	20	20	17	17
	31	31	28	28	25	25	22	22	19	19	16	16
	30	30	27	27	24	24	21	21	18	18	15	15
BANK 0	30	30	27	27	24	24	21	21	18	18	15	15
	31	31	28	28	25	25	22	22	19	19	16	16
	32	32	29	29	26	26	23	23	20	20	17	17

DRIVERS

RIGHT SIDE OF BOARD

A	B	A	B	A	B	A	B	A	B	A	B	A	B
14	14	12	12	10	10	8	8	6	6	4	4	2	2
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
14	14	12	12	10	10	8	8	6	6	4	4	2	2
14	14	12	12	10	10	8	8	6	6	4	4	2	2
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
13	13	11	11	9	9	7	7	5	5	3	3	1	1
C0	C0	C1	C1	C2	C2	C3	C3	C4	C4	C5	C5	C6	C6
14	14	12	12	10	10	8	8	6	6	4	4	2	2

CONNECTOR END OF BOARD

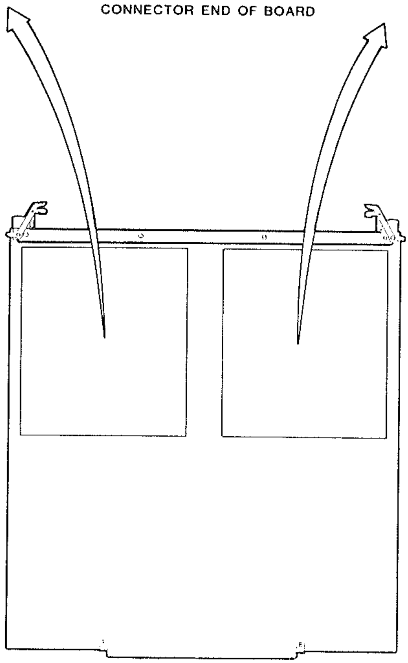
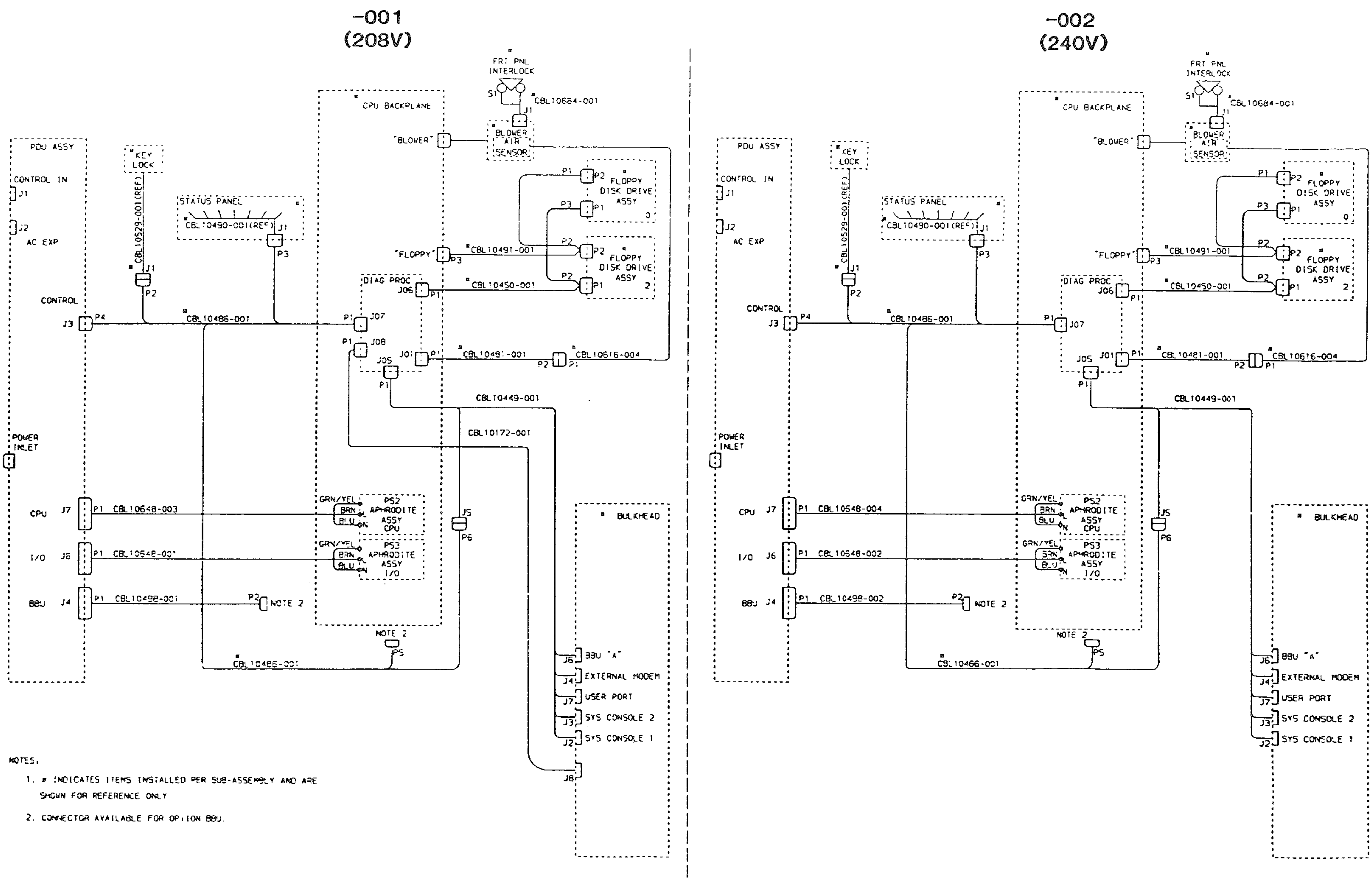


FIGURE A-2: MMW3 BIT MAP

MODEL 4050/4150 INTERCONNECTION DIAGRAM



NOTES:

1. * INDICATES ITEMS INSTALLED PER SUB-ASSEMBLY AND ARE SHOWN FOR REFERENCE ONLY
2. CONNECTOR AVAILABLE FOR OPTION BBU.

FIGURE A-3: WIRING DIAGRAM